Flight Computer

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SPACE PHYSICS RESEARCH LABORATORY

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Requirements Summary

- **Spacecraft Requirements**
  - MIL-STD-1553B Interface
  - Radiation Hardened, Qualified Components
- **Instrument Requirements**
  - Boot PROM
  - Data and Program RAM
  - EEPROM for Code and Data Storage
  - Watchdog Timer
  - Power-On Reset
  - Discrete Digital Output
  - Bus Interface for Control of Other Decks
  - Bench Test Features (Reset, Watchdog Disable)

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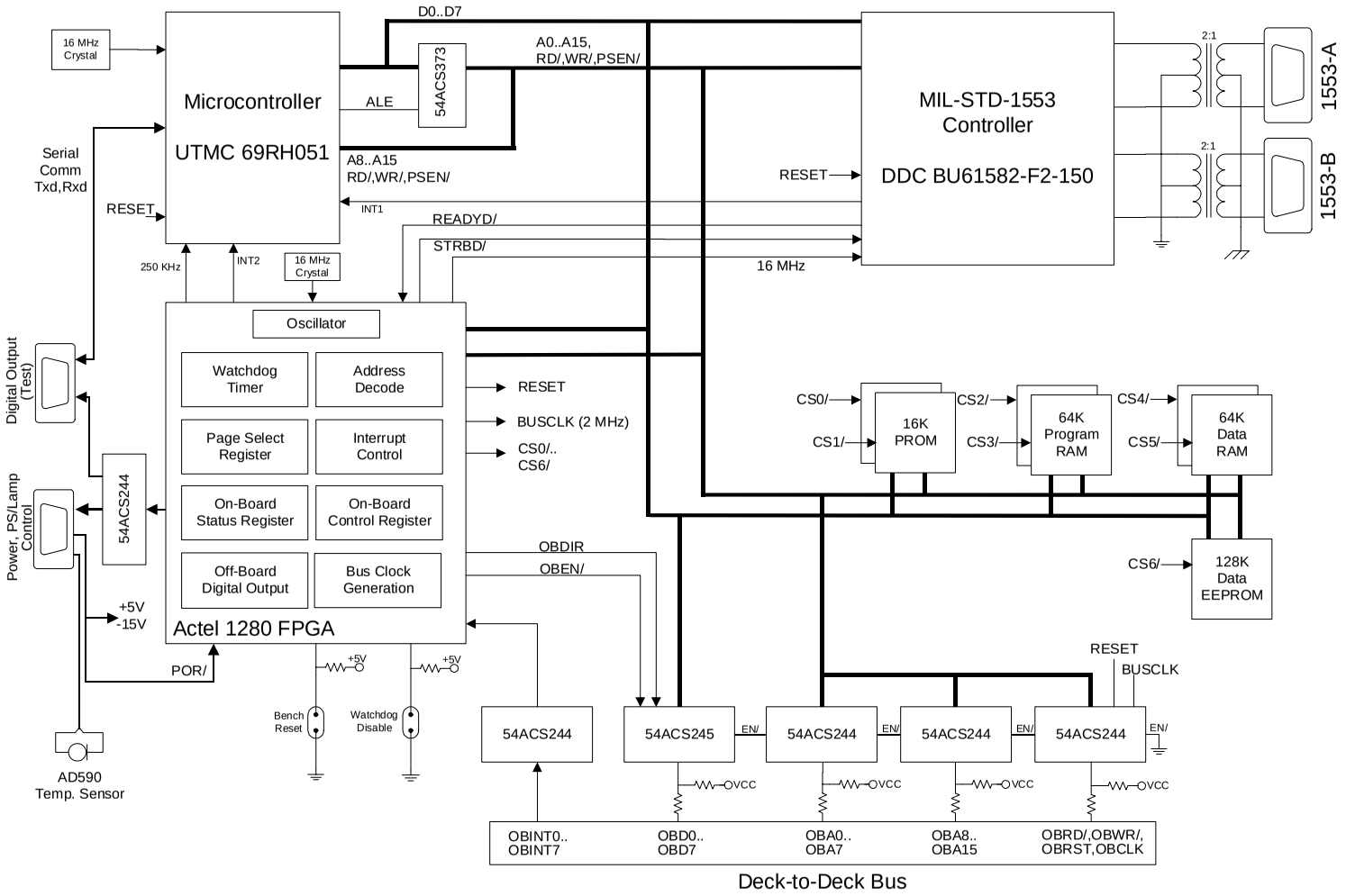
Subsystem Overview

- **CPU**
  - UTMC 69RH051 (Rad-Hard 80C51)
  - 16 MHz Clock
- **Memory**
  - 16K Boot PROM
  - 64K Program RAM
  - 64K Data RAM
  - 128K EEPROM
- **Spacecraft Interface**
  - MIL-STD-1553B (Transformer Coupled)
  - DDC BU61582

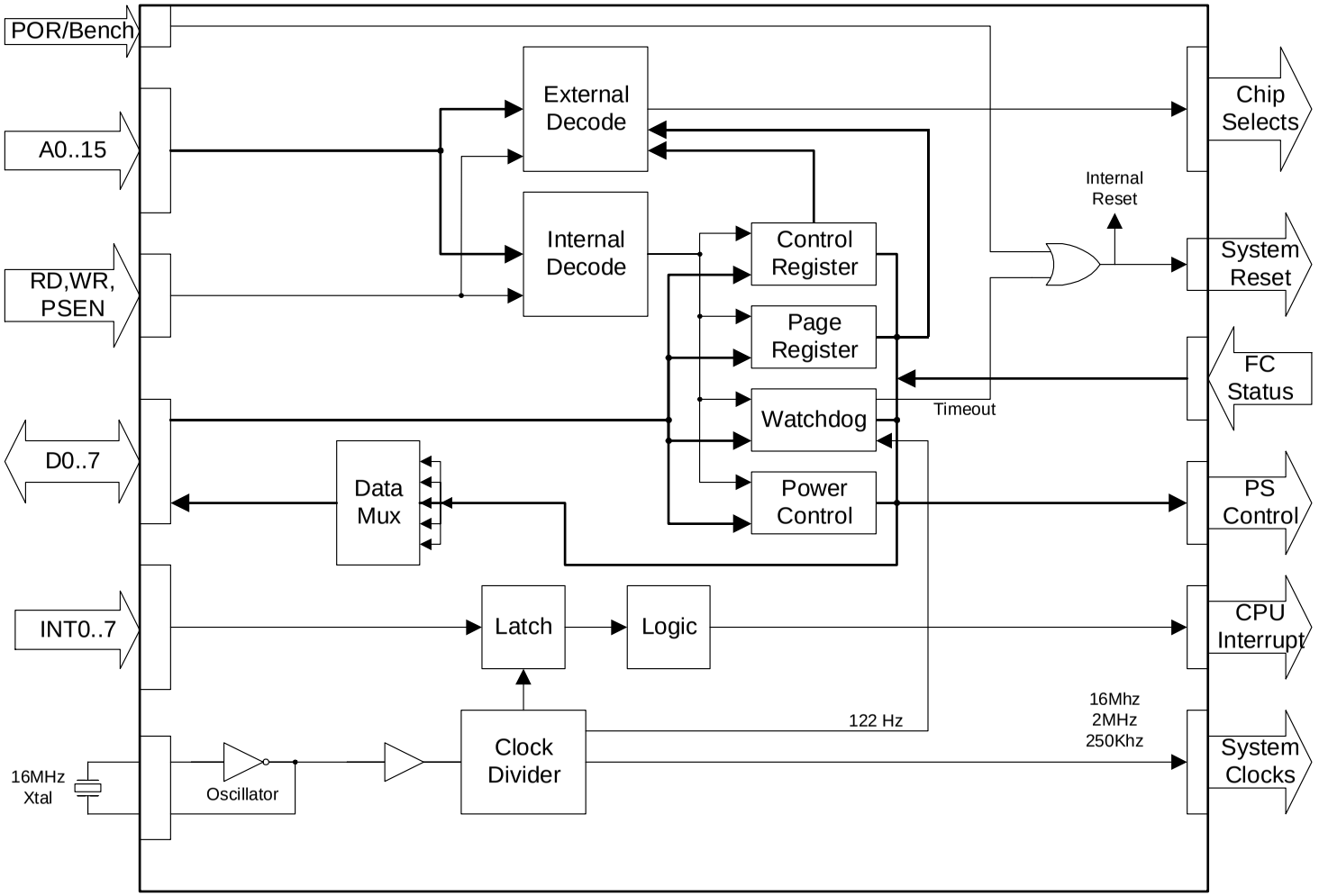
Subsystem Overview (cont.)

- **Instrument Control Bus**
  - **16-bit Address**
  - **8-bit Data**
  - **Read, Write, Reset, 8 Interrupts, 2 MHz Bus Clock**
- **General**
  - **Paged Memory**
  - **Watchdog Timer**
  - **Cal Lamp Control, Cal & Servo Power Supply Control**
  - **Bench Test (Reset, Watchdog Disable)**

Block Diagram



FPGA Block Diagram



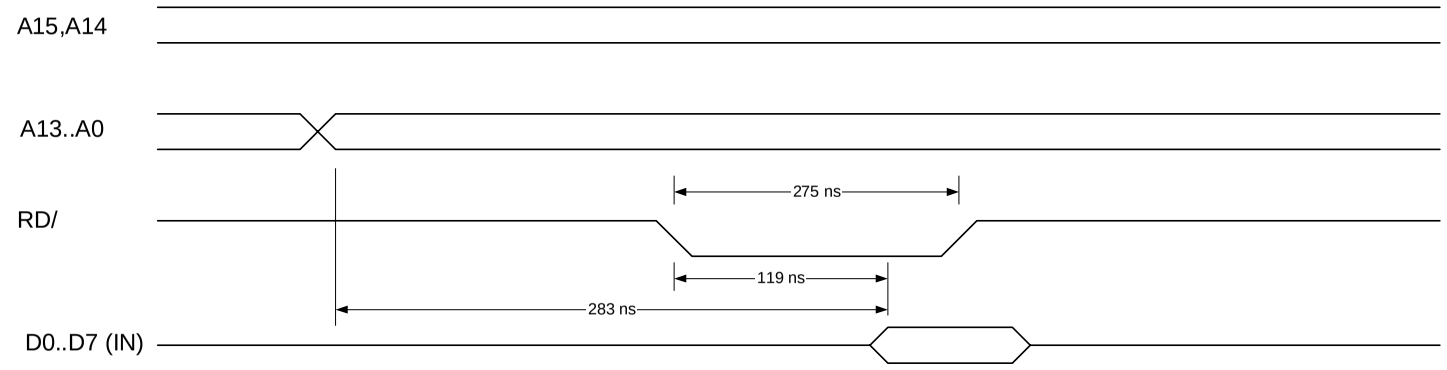
Operational Description

- **8051 Memory Space**
  - 64K Data Space
  - 64K Program Space
- **Memory Paging**
  - Allows More than 64K For Data Access
  - 16K Window in Data RAM
  - Page Register Controls Actual Memory Accessed via 16K Window
- **Bootup**
  - 16K PROM Available for Program Execution
  - 48K Program RAM Available for Program Execution
  - All Program RAM (64K) is Read/Write via Page Register

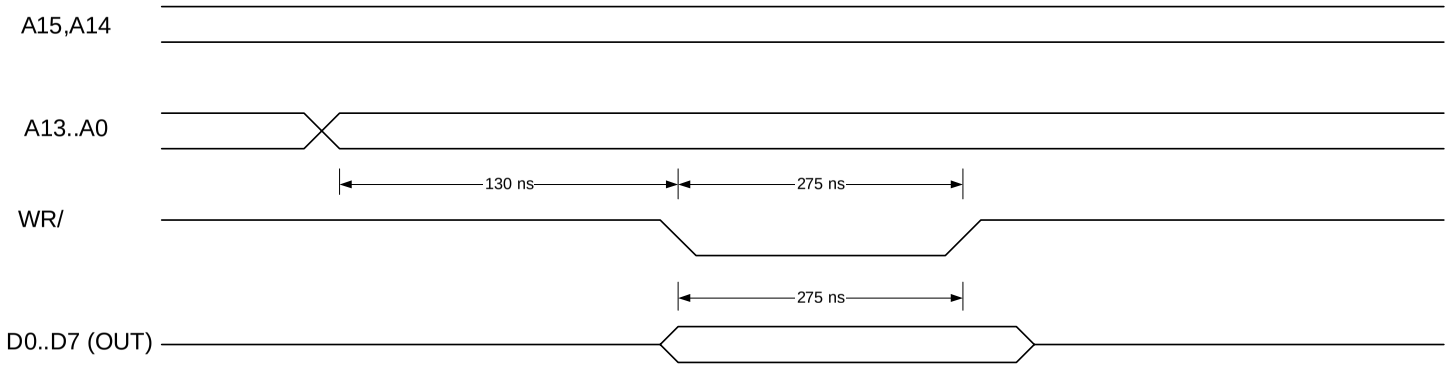
Operational Description (cont.)

- **Control Register**
  - **Disable PROM**
  - **Enable Read/Write access to Program RAM**
- **Watchdog Timer**
  - **FPGA State Machine**
  - **No Sequential Modules**
  - **2.09 Second Timeout**
  - **Generates 131ms Reset Pulse**

Bus Timing Diagrams



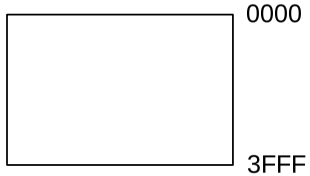
External Bus Read Cycle (16 MHz)



External Bus Write Cycle (16 MHz)

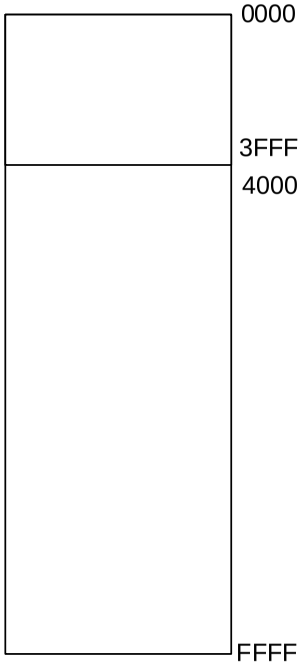
Memory Map

16K PROM



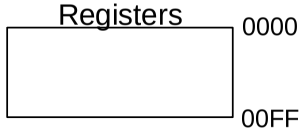
PROM is decodable after Reset. Can be disabled by CPU using Control Register.

64K Program RAM



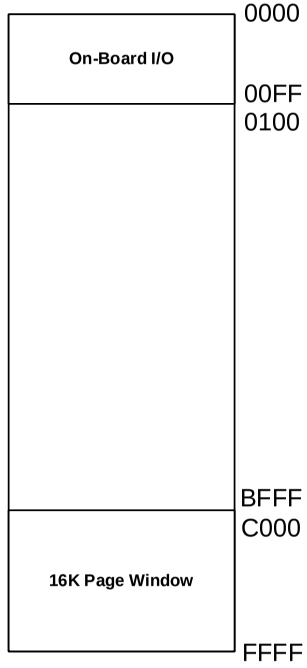
Program RAM above 0x4000 is decodable after Reset. Page Window access can be enabled by CPU using Control Register

Internal RAM/ Registers



Internal RAM/Registers are always accessible using appropriate 8051 addressing modes.

64K Data RAM



Actual memory space accessed using Data RAM addresses C000..FFFF is dependent on value of Page Register

On-Board Register List

On-Board Address (Hex)	On-Board Device	Register Size
0000..003F	1553 Registers	16 bits
80	Page Register	8 bits
81	Control Register	8 bits
82	Status Register	8 bits
83	Watchdog Reset	8 bits
84	Interrupt Register	8 bits
85	Digital Output	8 bits

Page Register Definitions

Page Register Value (Hex)	Device Accessed	Device Address (Hex)
00	Data RAM	C000..FFFF
01	Program RAM	0000..3FFF
02	Program RAM	4000..7FFF
03	Program RAM	8000..BFFF
04	Program RAM	C000..FFFF
05	Data EEPROM	0000..3FFF
06	Data EEPROM	4000..7FFF
07	Data EEPROM	8000..BFFF
08	Data EEPROM	C000..FFFF
09	Data EEPROM	10000..13FFF
0A	Data EEPROM	14000..17FFF
0B	Data EEPROM	18000..1BFFF
0C	Data EEPROM	1C000..1FFFF
0D	1553 RAM	0000..3FFF
0E	1553 RAM	4000..7FFF
0F	Boot PROM	0000.3FFF
80	CCD Controller Deck	(Bus) 0000..3FFF
81	Motor/Heater Deck	(Bus) 4000..7FFF
82	ADC Deck	(Bus) 8000..BFFF
83	Servo Deck	(Bus) C000..FFFF

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Design Status

- **Changes Since PDR**
  - **No significant changes**
- **Design Complete**
- **Engineering Model**
  - **PCB Assembled**
  - **Partially Tested**
    - **Memory Decoding**
    - **Memory Paging**
    - **On-Board Registers, 1553 Registers**
    - **Clocks**
    - **Program Execution**

Design Status (cont.)

- **Remaining Testing**
  - **1553 Interface**
    - **Interconnection with Spacecraft Simulator**
    - **Message Transfer**
    - **Electrical Verification of Interface to MIL-STD-1553**
  - **External Deck to Deck Bus**
    - **Addressing**
    - **Timing**
  - **Timing Verification**
    - **Decoder Performance**
    - **Memory Access Timing Margins**
  - **Temperature Test**
    - **Full Functional Test with PROMs (EEPROMs)**

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Planned Milestones

• Complete Engineering Model Tests	Early May
• Release Flight Computer to S/W Dev.	Mid May
• Incorporate Design Changes	Mid May
• Procure Flight PCB	Late May
• Assemble Flight PCB	Early June
• Test Flight PCB	Mid June