CCD Imaging System

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Requirements Summary

- CCD
  - 15 micron Pixels
  - Backside Illuminated
  - Low Noise
  - Flight Heritage
  - At Least 600 x 50 Pixels
- Subsystem
  - Selectable Image Region
  - Fixed Vertical Binning
  - Variable Horizontal (Wavelength) Binning
  - Adjustable Gain
  - Adjustable Erase and Expose Times
  - Provide Adjustable Clocking Rates to CCD
  - Provide Adjustable Drive Levels for CCD Clocks
  - Provide Test Interface for Image
  - Interface with DA Deck for Image Storage
  - Provide Power Supply and Heater Synchronization

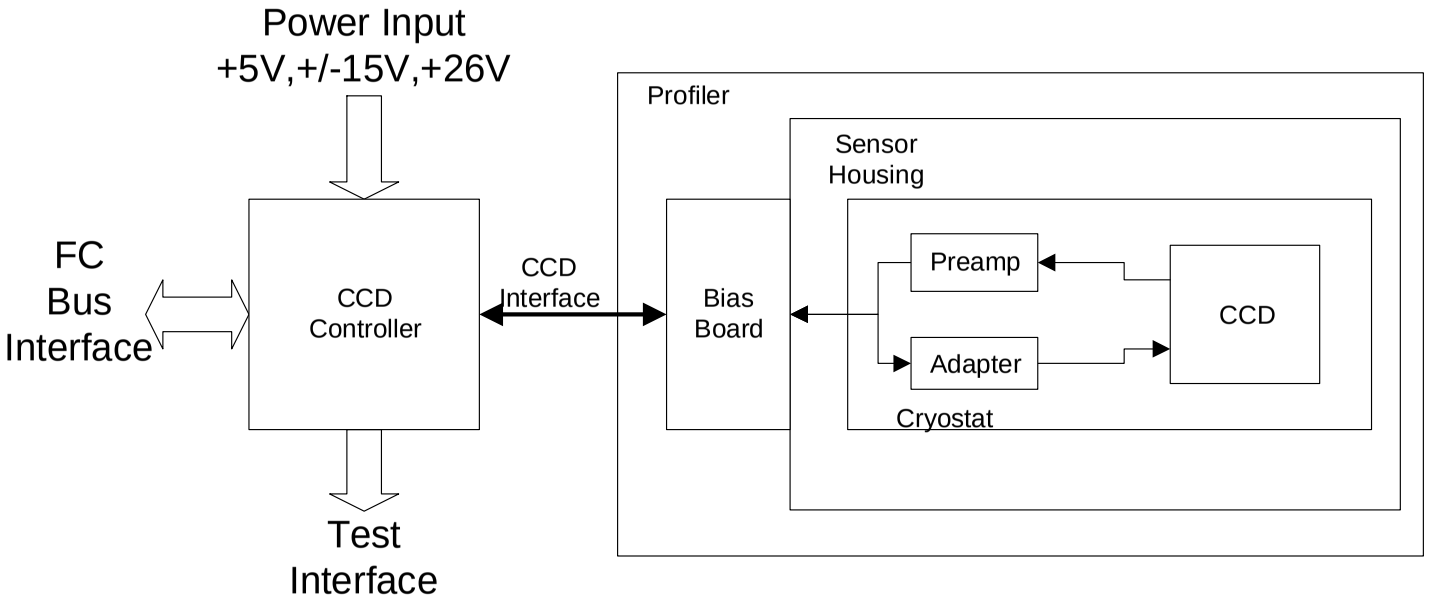
Subsystem Overview

- **CCD Controller**
  - Flight Computer Bus Interface
  - CCD Clock Rates
  - CCD Clock Levels
  - Post-Amp/Dual Slope Integrator
  - A/D Conversion
  - DA Deck Image Interface
  - Test Interface
- **Bias Board**
  - CCD Output Drain Voltage
  - Diode Temperature Sensor Interface
  - Signal Buffering/Bypassing

Subsystem Overview (cont.)

- **Preamp**
  - **CCD Output Preamplifier**
  - **Profiler Survival Heater**
- **Adapter**
  - **Interconnection from Cold to Hot**
- **CCD**
  - **SITe ST005A**

Subsystem Block Diagram



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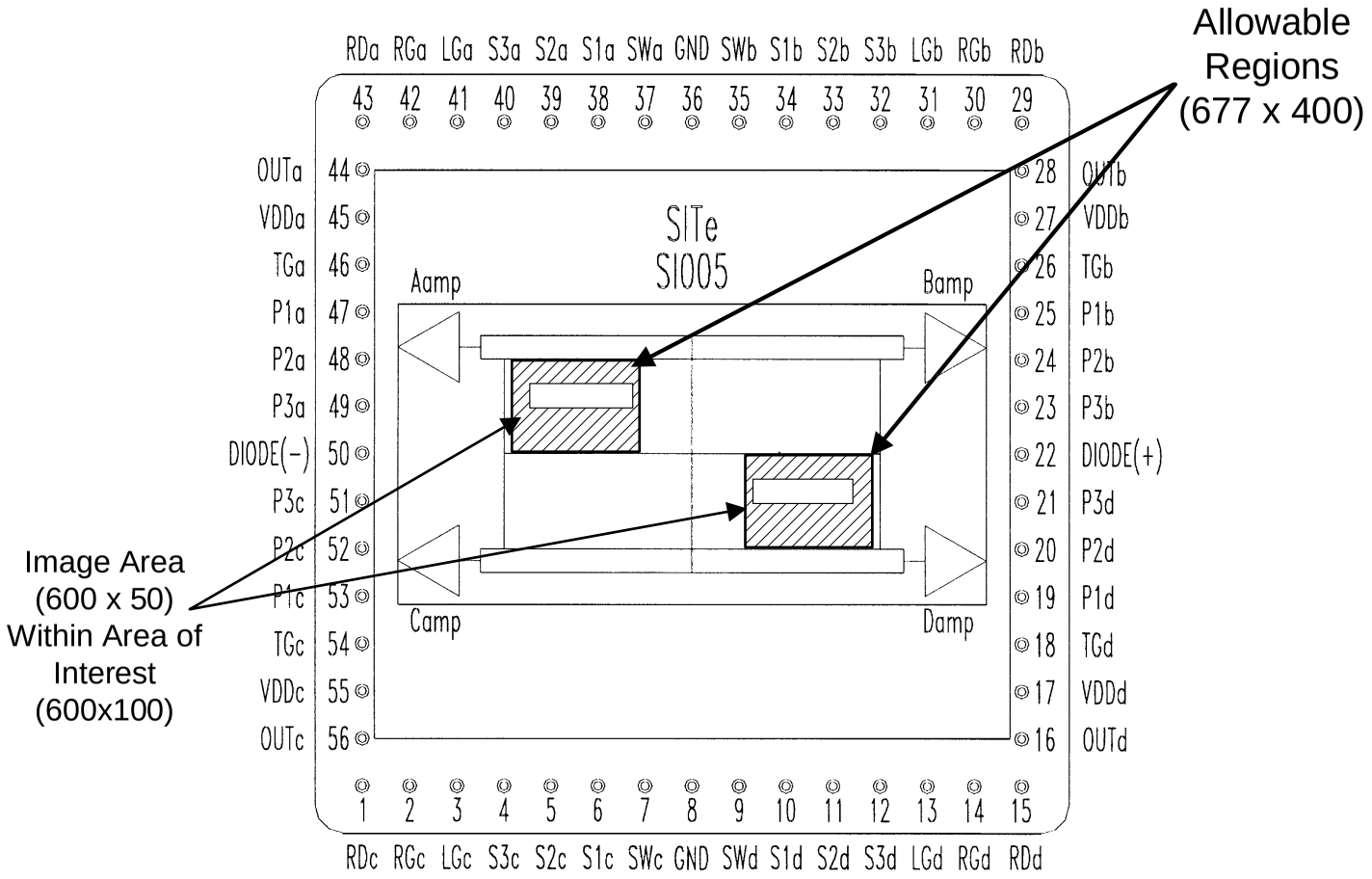
CCD Overview

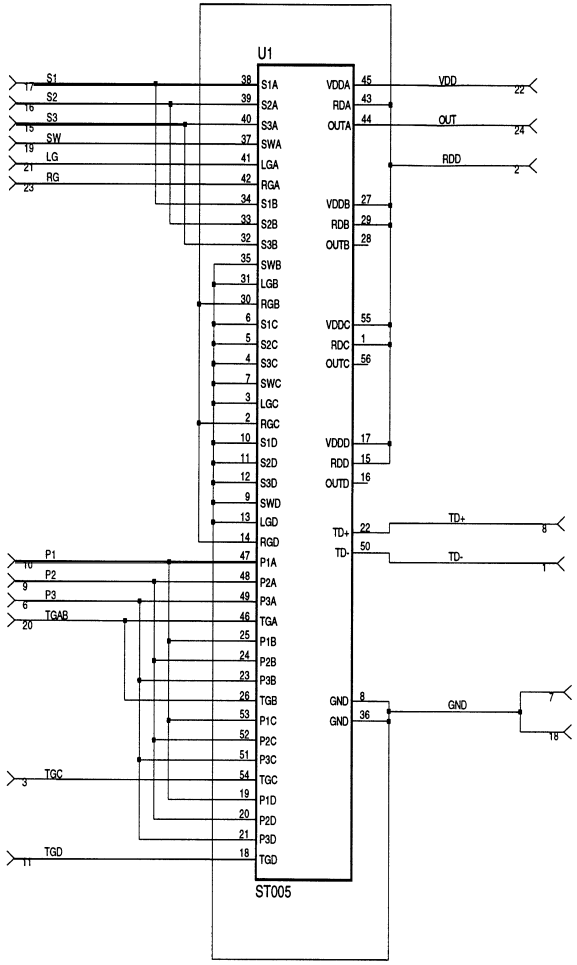
- SITe ST-005A
- 2000 x 800 Pixels
- Backside Illuminated
- 15 µm Pixels
- QE Stability
  - 53% @ 500nm
  - 63% @ 600nm
  - 35% @ 900nm
  - ±0.2% Pixel to Pixel Relative
  - ±2.0% Absolute
- CTE
  - 0.99999 at 40k Electrons/pixel
  - 0.99995 at 1620 Electrons/pixel
- Full Well
  - 60k Electrons, MPP Mode
  - 600k Electrons in Serial Register
- Area of Interest
  - 600 x 100 Pixels
  - No Hot or Dark Pixels
  - Single Quadrant
  - QE within ±15% of Average
- Output Amplifiers
  - Greater than 1µV/electron
  - 30mW Power Dissipation Max.
- Readout Noise ≤ 8 electrons

CCD Region of Interest



CCD Schematic

- Package Can Be Rotated 180°
- Output A or D
- All Parallel Clocks Common
- One Serial Register Used



CCD Statement of Work

- Updated to Revision 055-3479A
- Mostly Minor Changes to Facilitate Testing at SITe
- More Detailed Testing Specifications
- Area of Interest Increased to 600x100 (was 600x50)
- Diode Temperature Sensor (was Resistive)

CCD Procurement Status

- **Engineering Grade Devices**
  - Due to Equipment Problems at SITe:
    2 of 5 Engineering Grade Devices are not from Flight Lot
    Delivery Delayed from April 1, but In-House Now
    Diode Temperature Sensor Included
  - 3 of 5 Accelerated Life Test Devices From Flight Lot
    1000 Hour Tests Completed After Flight Delivery
- **Grade 2 Devices**
  - 2 Devices with Good Specs
  - Due In-House Now
- **Flight Grade Devices**
  - Delivery in October/November

Flight CCD Qualification

- **SITe Accelerated Test Program**
  - **Lots out of Fab** **5/20/98**
  - **Wafer and Package Test Complete** **6/15/98**
  - **Mechanical Testing Complete (2 Devices)** **7/2/98**
  - **Screen Testing Complete** **7/8/98**
  - **Flight Testing Complete** **7/17/98**
  - **3 Flight Units Shipped to U of M** **7/21/98**

  - **1000 Hour Life Test Complete (3 Devices)** **8/5/98**

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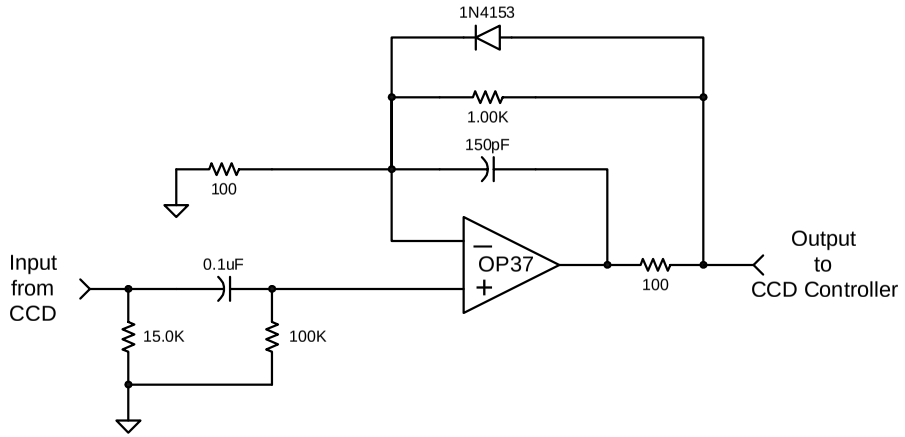
Preamp/Bias Overview

- **Preamp**
  - CCD Output Amplification
  - CCD Signal Bypassing, Conditioning
  - Interfaces Hot Side to Cold Side
- **Bias**
  - CCD Temperature Diode Conditioning
  - CCD Signal Bypassing, Conditioning

Preamp Schematic

- **15K Load R for CCD Output**
- **AC Coupled**
- **Gain of 11**
- **OP37 Op-Amp**



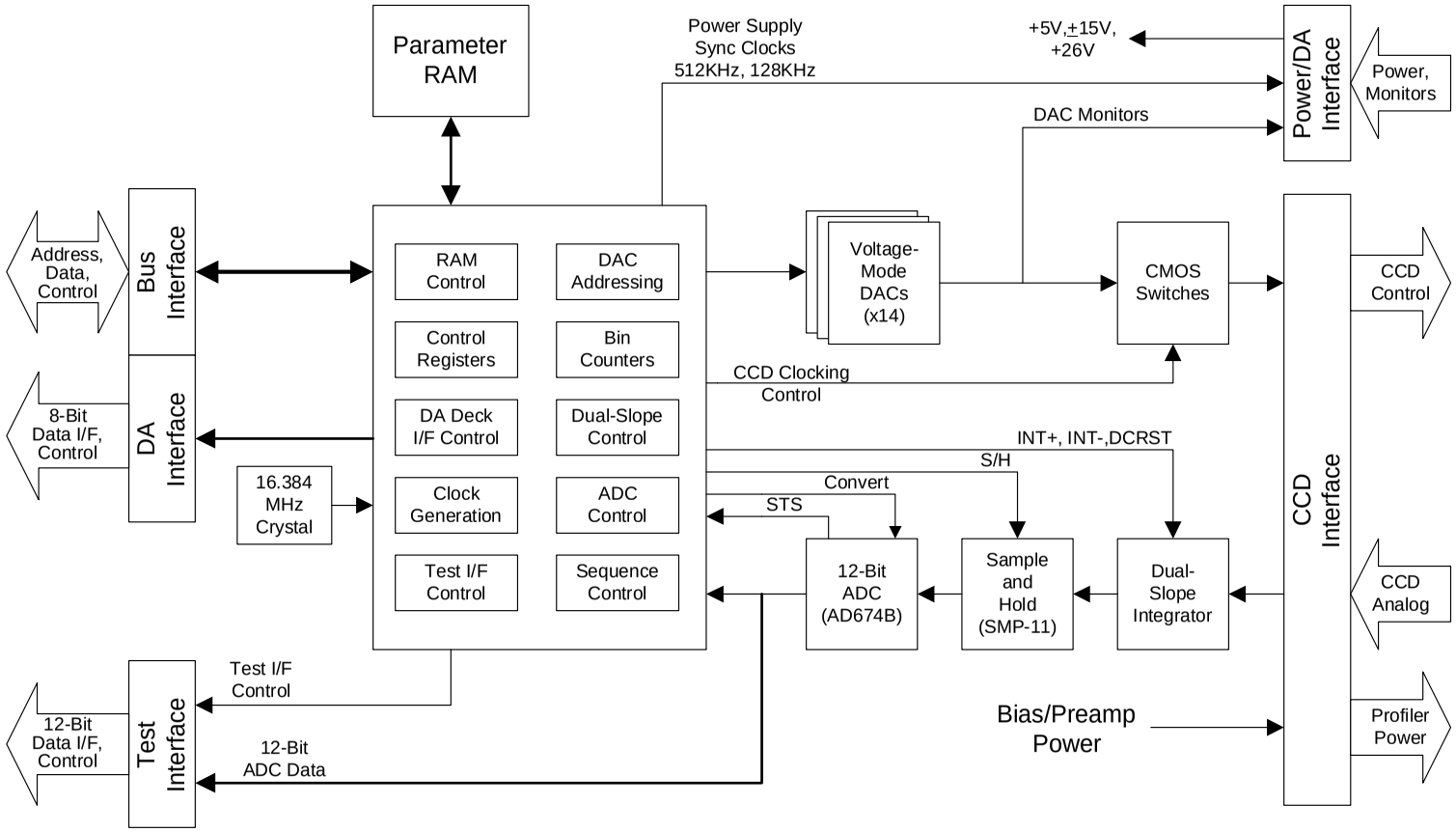
CCD Controller Overview

- **Flight Computer Bus Interface**
- **FPGA**
  - **Provides all Timing and Control Functions**
- **D/A Converters**
  - **High and Low Voltages for CCD Clocks**
  - **Bias Voltages**
- **Dual-Slope Integrator**
  - **Eliminates Reset Noise**
  - **Provides Post-Amp Gain**

CCD Controller Overview (cont.)

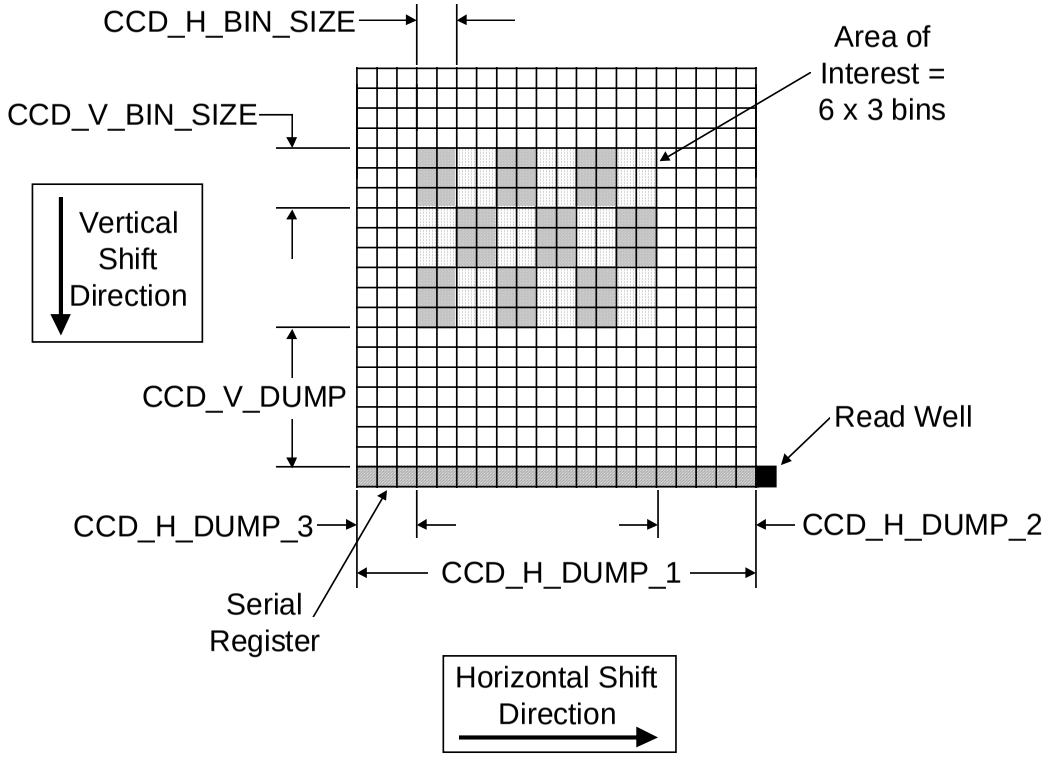
- **A/D Converter**
  - 12-Bit AD674B
  - 15usec Max. Conversion Time
- **CCD Interface**
  - CMOS Switches Controlled by FPGA Create Clocks
  - DACs Provide Inputs to Switches
- **DA Deck Interface**
  - 8-bit Interface to Image Memory
  - 12-bit Words Split into 4/8-bit Transfers

CCD Controller Block Diagram



CCD Controller FPGA Overview

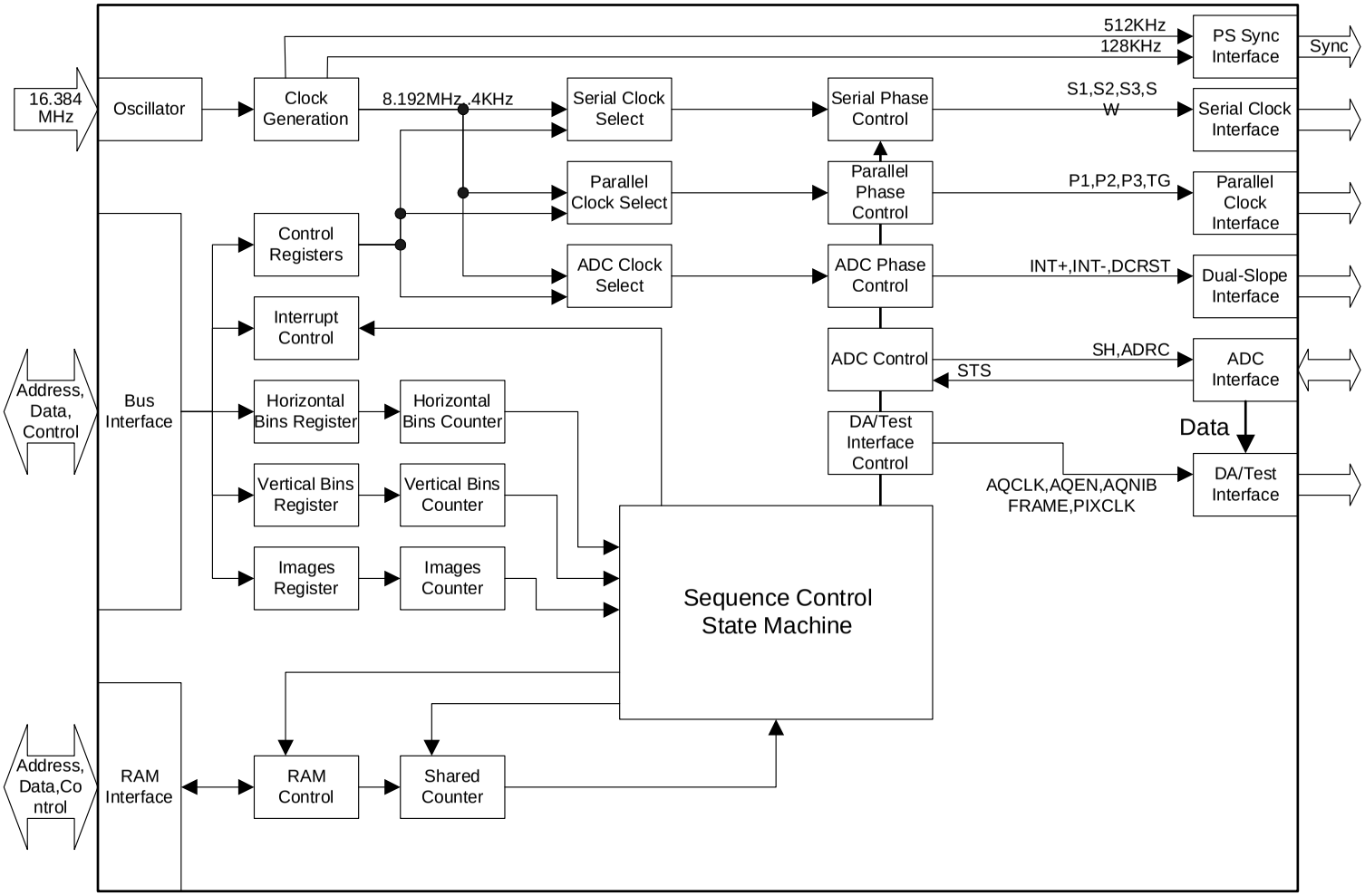
- **Sequence Control**
  - **Erase**
  - **Expose**
  - **Vertical Dump**
  - **Serial Register Dump**
  - **Vertical Binning**
  - **Horizontal Dump**
  - **Horizontal Binning**
  - **Conversion**
- **Binning**
  - **Fixed**
  - **Variable (Horizontal)**



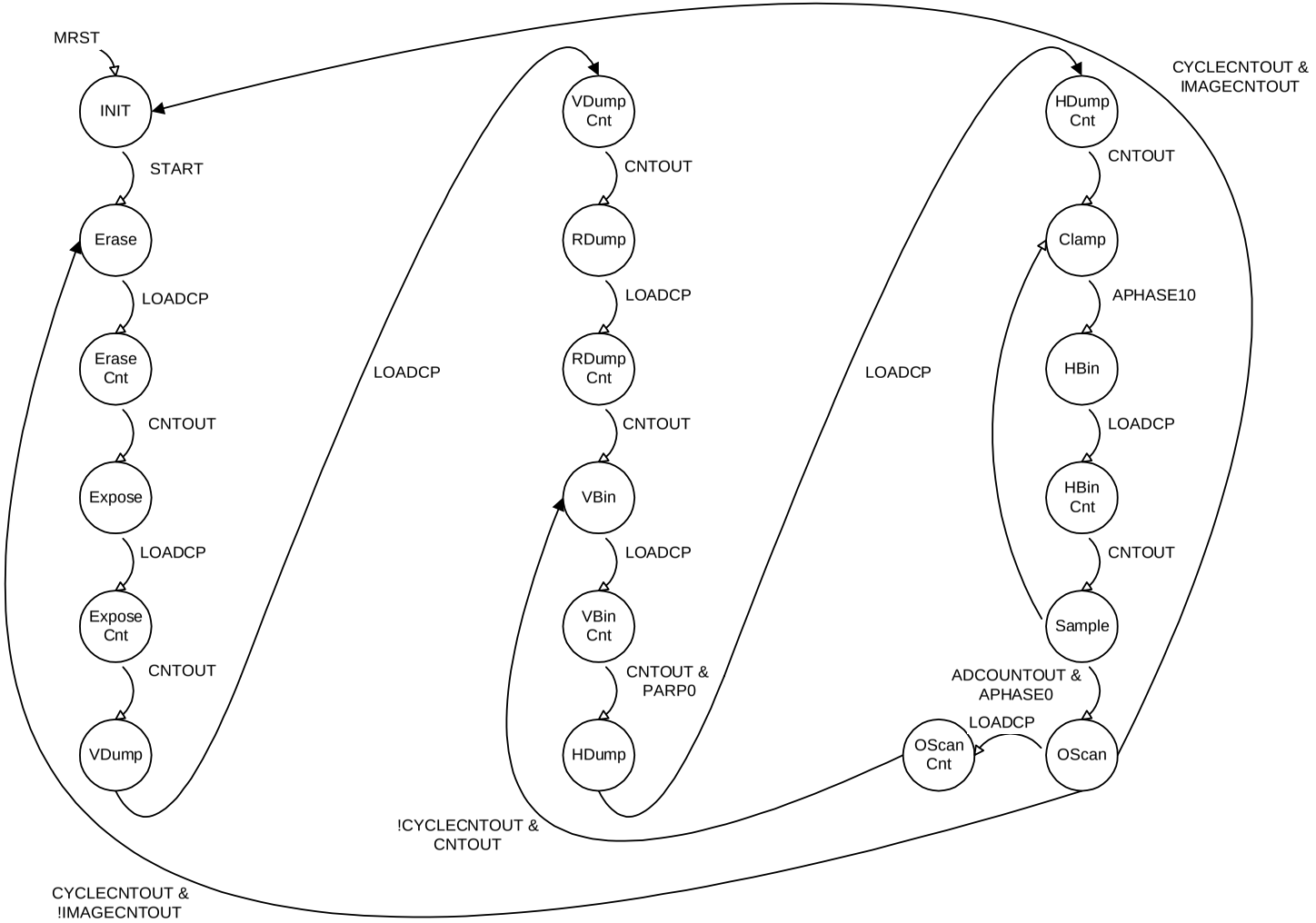
CCD Controller FPGA Overview (cont.)

- **Gain Control**
  - 2 Gain States for Dual-Slope Integrator
  - Fixed or Variable (Horizontal/Wavelength)
- **Conversion/Shifting Rates**
  - 7 Serial Clock Rates
  - 7 Parallel Clock Rates
  - 7 A/D Conversion Rates
- **Image Memory Interface**
  - DA Deck 8-Bit Interface
  - 2 Transfers for Each Pixel
- **Test Interface**
  - 12-Bit Interface
  - Spectral Images PCI Board (PC)

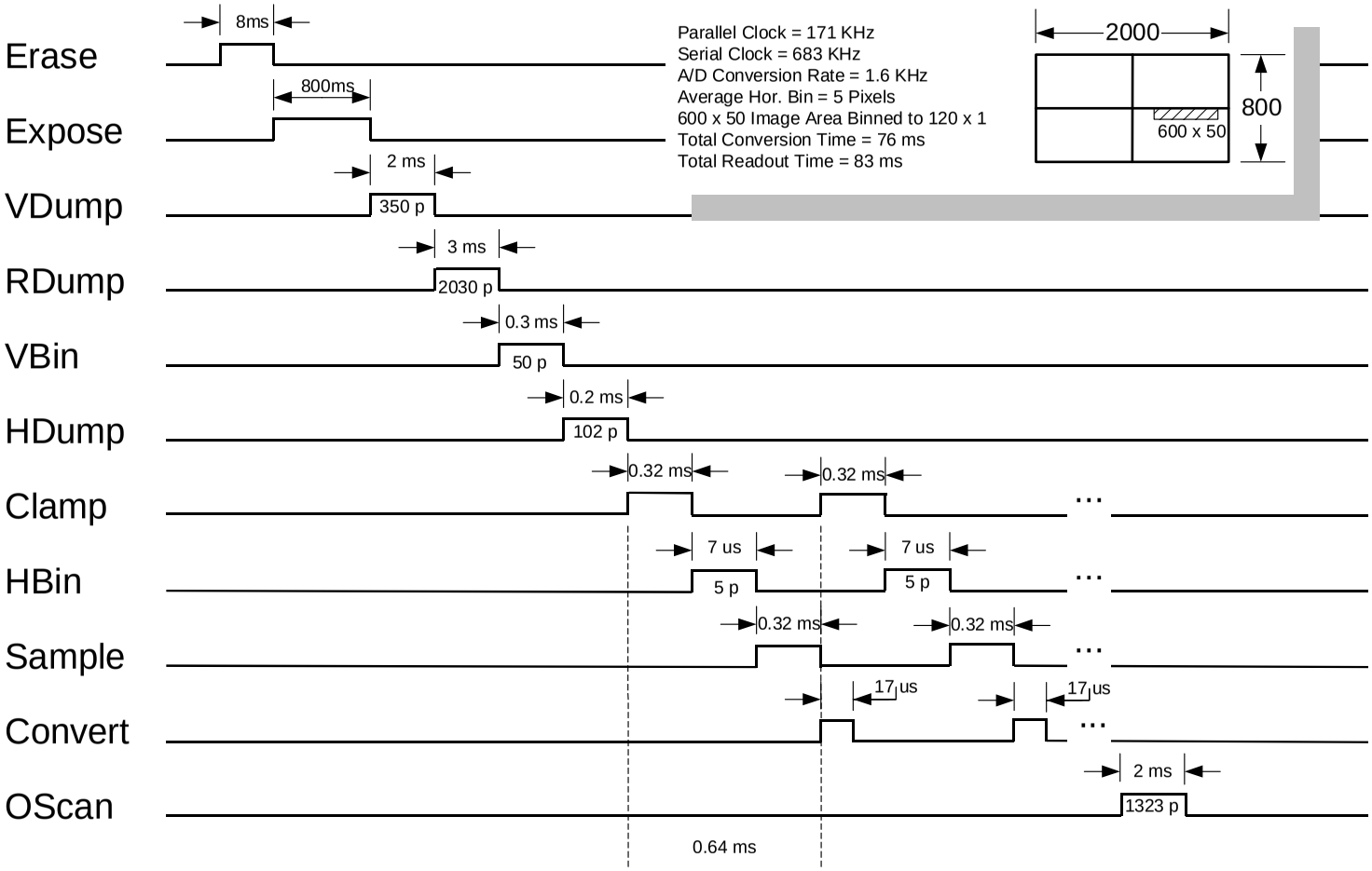
CCD FPGA Block Diagram



CCD FPGA Main State Machine



Timing - Image Cycle



Subsystem Performance

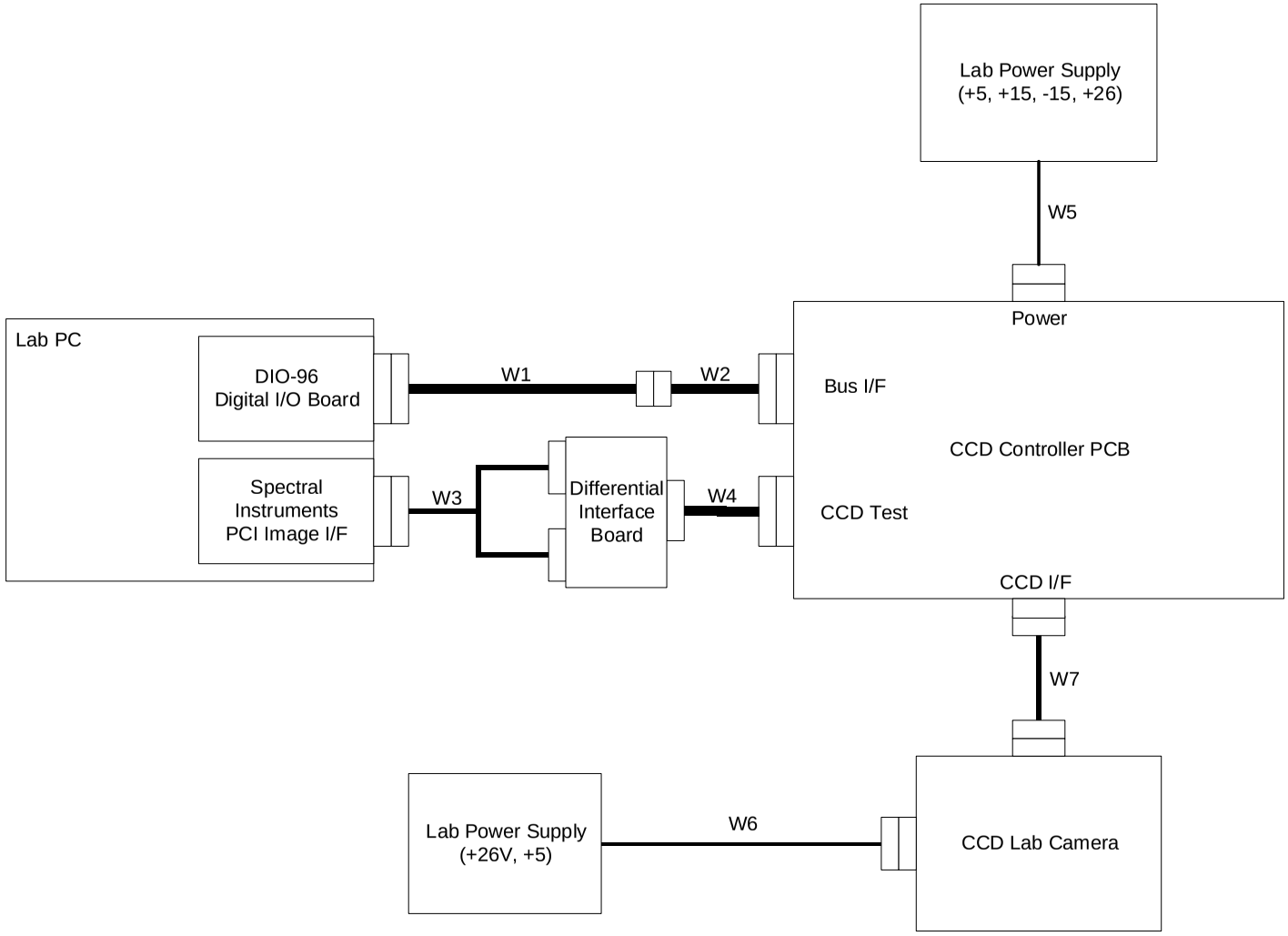
- **CCD Gain:** 1.5μV/electron
- **CCD MOSFET 1/F Noise:** 8 electrons
- **Preamp Noise:** 3 electrons
- **Total Noise (RSS):** 8.5 electrons
- **ADC Performance:**

A/D Rate	Counts/e-	Readout Time (120 x 1 Image)
1.6 KHz	1.1	75 ms
3.2 KHz	0.55	37.5 ms
6.4 KHz	0.28	18.8 ms
12.8 KHz	0.14	9.4 ms

Test Flow

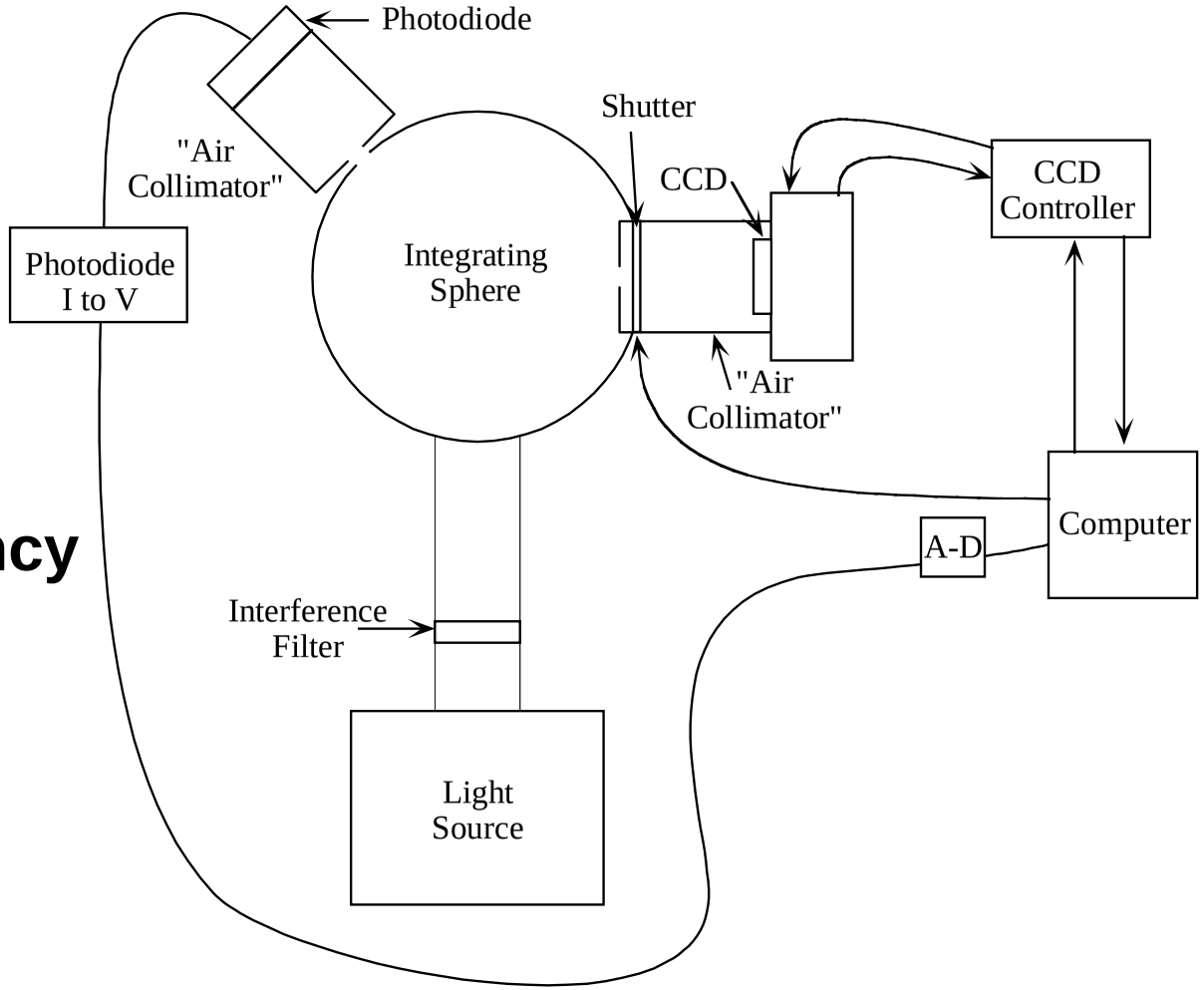
- **Engineering Model CCD Controller Standalone Testing**
- **Integration with Test Camera Head**
  - **Prototype Bias**
  - **Prototype Preamp**
  - **Engineering Grade CCD**
  - **Shutter/Shutter Control**
- **Development of Characterization Procedures**
- **Integration with Engineering Electronics Stack**
- **Characterization of Flight CCDs**

Test Setups - Functional Testing
Standalone CCD Controller



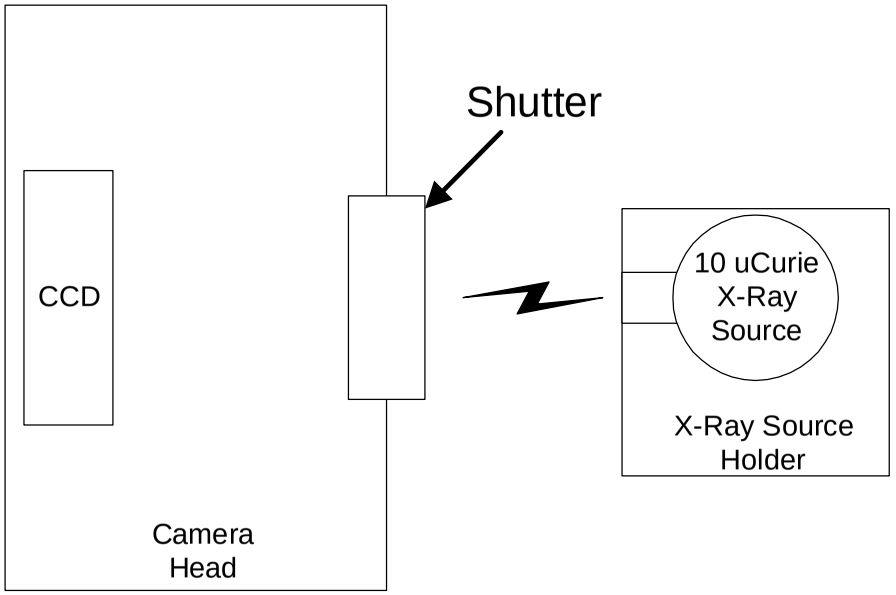
CCD Characterization

- **Bias**
  - **Read Noise**
  - **Electronics Noise**
- **Dark Counts**
- **Photon Transfer**
- **Flat Field**
- **Quantum Efficiency**
- **QE Stability**



CCD Characterization

- **X-Ray CTE**



TIDI Engineering Model Status

- **CCD Controller Status**
  - Assembled
  - Bus Interface Verified
  - Clocking Verified
  - RAM Access Verified
  - Basic Sequencing Verified
  - ADC Control Verified
  - ADC Trimmed for 0 to 10V Operation
  - DAC Operation Verified
  - Test Interface Operation Verified
- **CCD Controller EM Checkout Remaining**
  - Verify CCD Clock Timing
  - Test Dual-Slope Integrator

Engineering Model Status (cont.)

- **Lab Camera Status**
  - PCB in Manufacturing
  - Camera Head Assembled
  - Engineering CCDs In-House
- **Lab Camera Checkout Remaining**
  - Verify Preamp/Bias Operation
  - Verify Connections to CCD
  - Verify Shutter Operation
  - Integrate and Test CCD

Engineering Model Status (cont.)

- **Image Processing Software Status**
  - Basic User Interface Complete
  - CCD Controller Setup Complete
  - Basic Image Acquistion (via Test Interface) Complete
- **Image Processing Software Tasks Remaining**
  - “Image Manager” Interface
  - Support for Multiple Images
  - User Settable Region of Interest with Statistics
  - Automatic Flat-Fielding Support

Planned Milestones

• EM Controller Checkout Complete	Mid May
• EM Preamp/Bias Checkout	Late May
• Image Processing Software	Late May
• Engineering CCD Test Complete	Mid June
• Incorporate Design Changes	Late June
• Manufacture Flight PCBs	Mid July
• Assemble Flight PCBs	Early August
• Begin Testing Flight Components	Early August

ADC Calculations

$$\frac{\text{Counts}}{\text{electron}} := \left(\frac{4096}{10\ \text{V}}\right) \cdot \frac{G_{ccd} \cdot G_{Preamp}}{R \cdot C} \cdot \int_0^T 1 \, dt$$

Where:

$$G_{ccd} := 1.5 \cdot \frac{uV}{e}$$

$$G_{Preamp} := 11$$

$$R := 500\Omega$$

$$C := 2700pF$$