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TIMED

Thermosphere - Ionosphere - Mesosphere - Energetics - Dynamics

Software - Hardware Interfaces
for the
GPS Navigation Subsystem

The Johns Hopkins University
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GPS Navigation Subsystem

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1.0 INTRODUCTION

1.1 Overview

The TIMED program is an atmospheric remote sensing mission to study the interaction of the Sun and the Earth's atmosphere. The spacecraft will serve as a platform for four instruments that measure the basic state parameters and energy balance of the Mesospheric, Lower Thermospheric, and Ionospheric region of the atmosphere. These instruments require precise knowledge of the position and velocity of the spacecraft to perform their mission. The GPS Navigation Subsystem is the spacecraft's autonomous navigation and timekeeping subsystem. It will provide not only position, velocity, time and earth-sun vector information in realtime, but it will also provide notification of defined orbital events such as terminator crossings and predictions of events such as ground station contacts. In addition, it will generate orbital elements sets which will be downlinked for use by ground station antenna pointing systems. The GNS contains two computers, namely, the tracking processor and the navigation processor (see Figure 1). The tracking processor is responsible for the low-level GPS hardware interaction and control, and the navigation processor is responsible for the command/telemetry handling, navigation and the associated data product generation.

1.2 Purpose

The purpose of this document is to specify the software-hardware interfaces for the TIMED spacecraft's GPS Navigation Subsystem (GNS). The GNS software requirements and design are specified within other documents. The understanding of GPS specific terminology used in this document is assumed.

1.3 Acronyms

AIC	Accumulator Interval Clock
ASIC	Application Specific Integrated Circuit
C&DH	Command and Data Handling Subsystem
DRAM	Dynamic Random Access Memory
GNS	GPS Navigation Subsystem
GPS	Global Positioning System
GSE	Ground Support Electronics
GTA	GPS Tracking ASIC
H/W	Hardware
IEM	Integrated Electronics Module
MIC	Measurement Interval Clock
NP	Navigation Processor
NP/TP	Navigation Processor to Tracking Processor interface
PCI	Peripheral Component Interconnect
PPS	Pulse Per Second
RAM	Random Access Memory
SRAM	Static Random Access Memory
S/C	Spacecraft
S/W	Software
TBD	To Be Determined
TIMED	Thermosphere - Ionosphere - Mesosphere - Energetics - Dynamics
TP	Tracking Processor
UART	Universal Asynchronous Receiver Transmitter

1.4 Applicable Documents

1. TIMED GPS Navigation System (GNS) Software Requirements Specification, A. Chacos, 7363-9333, 24 Sep 97
2. TIMED GPS Navigation System (GNS) Requirements, R. J. Heins, 7363-9336, (Draft)
3. TIMED GPS Navigation System (GNS) Software Development Plan, A. A. Chacos, 7363-9331, 13 Mar 97
4. TIMED Command & Data Handling Computer, SRS, S. P. Williams, (Draft)
5. Synova Processor User's Manual, Rev 1.1, 7/10/97
6. GPS Tracker ASIC (GTA) Requirements Document, 7/25/97, (Preliminary)

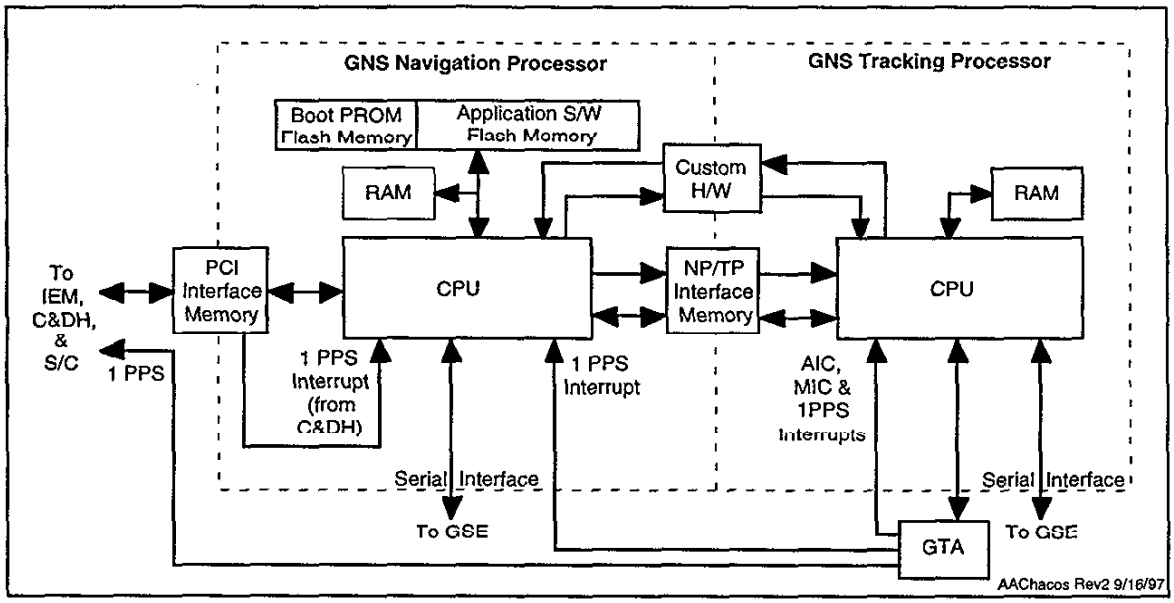

Figure 1 : Simplified GNS Hardware Layout

2.0 SOFTWARE - HARDWARE INTERFACES

2.1 Navigation Processor

2.1.1 Resets

Any cause of a navigation processor reset will, by software, force a reset of the tracking processor. This will be accomplished by the navigation processor asserting an I/O line in the Reset Actel which in turn will reset the tracking processor. The reset exception vector for the Mongoose V processor is 0xBFC0.0000.

2.1.1.1 Externally Initiated Resets

2.1.1.1.1 IEM Master Reset

This reset is applied to the entire IEM including the GNS navigation processor.

2.1.1.1.2 GNS Reset

This reset is applied to the GNS navigation processor by the C&DH subsystem upon initiation by ground command.

2.1.1.1.3 Console Reset

This reset is applied to the navigation processor by a hardwired connection to the GNS GSE, and thus is used only during pre-launch testing and operations.

2.1.1.2 Internally Initiated Resets

2.1.1.2.1 Watchdog Timer Reset

This reset is asserted if the navigation processor fails to write at a specified rate to the watchdog timer register address 0x1C10.794C. The data written is ignored.

2.1.1.2.2 EDAC Unrecoverable Double-Error Reset

This reset is asserted if the navigation processor EDAC circuit detects that the last memory access has two or more bit errors which is a non-recoverable condition.

2.1.1.2.3 Invalid DRAM Address Space Access Reset

This reset is asserted if the navigation processor attempts to access memory in the address range of 0x0000.0000 to 0x0FFF.FFFF. These addresses are reserved for DRAM which does not exist in the navigation processor hardware.

2.1.1.2.4 Navigation Processor Initiated Reset

This reset is asserted by the navigation processor software. It normally will be used for test purposes only, by writing to the Reset Actel address 0x1C10.B466 (see Appendix C). The data written is ignored.

2.1.2 Interrupts

There are 6 primary interrupts; namely, INT[0] thru INT[5] which are prioritized, INT[0] having the highest priority and INT[5] having the lowest priority. There are 32 expansion interrupts; namely, INT[5-0] thru INT[5-31] which are not prioritized and which are 'funneled' thru INT[5]. INT[5-0] thru INT[5-9] are user-defined interrupts and INT[5-10] thru INT[5-31] are used for internal functions.

2.1.2.1 Peripheral Interrupts

2.1.2.1.1 GTA Steered 1PPS Interrupt

This interrupt, INT[2], is asserted by the steered 1PPS signal generated by the GTA hardware at a 1 per second rate. This interrupt is acknowledged by writing to the PCI Actel address 0x1C18.0008. The data written is ignored.

2.1.2.1.2 GTA I/O Disabled Interrupt

This interrupt, INT[4], is asserted by the Reset Actel whenever the tracking processor GTA I/O access is disabled. There is no acknowledgment for this interrupt. After the interrupt occurs it can be masked, the cause can be read from the Reset Actel's Reset Cause Register, the navigation processor can re-enable the GTA I/O access (which would de-assert the interrupt), and then the interrupt could be unmasked.

2.1.2.1.3 PCI Data Write to Buffer Address 0x0FFF Interrupt

This interrupt, INT[5-2], is asserted by the PCI hardware when a word is written to the PCI buffer address 0x0FFF by the C&DH at a 1 per second rate. This occurs within 15 milliseconds of the GNS 1PPS signal output to the C&DH, and it is used as the starting time mark for the read/write access timing to the PCI buffer (see Figure 2). This interrupt is acknowledged by writing to the PCI Actel address 0x1C18.000A. The data written is ignored.

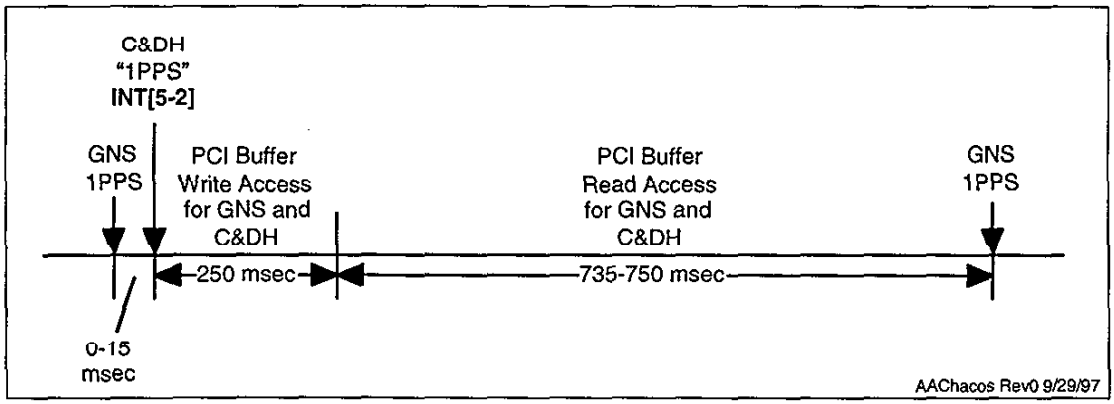

Figure 2 : PCI Buffer Access Timing

2.1.2.1.4 MIC-Delayed Interrupt

This interrupt, INT[5-7], is asserted by the tracking processor software to alert the navigation processor that it has received a MIC interrupt and has written the raw tracking data to the NP/TP interface buffer. This interrupt occurs at a rate corresponding to the MIC interrupt rate which nominally is 1 per second, but can be increased or decreased for testing purposes. The interrupt is acknowledged by writing to the Reset Actel address 0x1C10.B46A (see Appendix C).

2.1.2.1.5 Flash Memory Interrupt

This interrupt, INT[5-8], is asserted by the Reset Actel when a Flash memory erase or programming operation has completed. There is no acknowledgment for this interrupt (the interrupt will be de-asserted when the next erase/programming operation is initiated) and it should be masked-off when not erasing or programming the Flash memory.

2.1.2.2 Mongoose V Interrupts

The descriptions below only indicate which interrupts are asserted by the Mongoose V processor functions. See Applicable Document #5 (Section 1.4) for additional information.

2.1.2.2.1 Timer 1 Interrupt
This asserts INT[0].

2.1.2.2.2 Timer 2 Interrupt
This asserts INT[1].

2.1.2.2.3 Floating Point Unit Interrupt
This asserts INT[3].

2.1.2.2.4 UART 0 Interrupts
This asserts INT[5-11 thru 5-15].

2.1.2.2.5 UART 1 Interrupts
This asserts INT[5-17 thru 5-21].

2.1.2.2.6 Memory R/W Access Violation Interrupts
This asserts INT[5-22 and 5-23].

2.1.2.2.7 EDAC Error Interrupts
This asserts INT[5-30 and 5-31].

2.1.3 Memory Access
The most significant three bits of the 32-bit addresses are used at a system level to define user vs. kernel mode and cacheable vs. non-cacheable address space. The state of these three bits has been ignored for defining the address spaces in the sections below.

2.1.3.1 Flash Memory
2.1.3.1.1 Memory Size
The size of the navigation processor Flash memory is 4MB.

2.1.3.1.2 Access Data Width
The data is accessed as 32-bit words, thus the least-significant two address bits must be zero.

2.1.3.1.3 Address Space
The decoded address space for the navigation processor Flash memory is 0x1F00.0000 to 0x1F3F.FFFF. Note that bits b22-b23 are not decoded for this address space and, if used, will cause rollover into the decoded address space.

2.1.3.2 Static RAM
2.1.3.2.1 Memory Size
The size of the navigation processor SRAM is 2MB.

2.1.3.2.2 Access Data Width
The data is accessed as 32-bit words, thus the least-significant two address bits must be zero.

2.1.3.2.3 Address Space
The decoded address space for the navigation processor SRAM is 0x1000.0000 to 0x101F.FFFF. Note that bits b21 b26 are not decoded for this address space and, if used, will cause rollover into the decoded address space.

2.1.4 Reset Actel Registers

See Appendix C for a memory map and a complete list of all discrete I/O in the Reset Actel.

2.1.4.1 Number of Registers

There is one register accessible to the navigation processor; namely, the Reset Cause Register which can be read at address 0x1C10.0000. It is divided into three sections; namely, the navigation processor section (bits [6:0]) which can be cleared by writing to the Reset Actel address 0x1C10.B464, the tracking processor section (bits [11:7]) which can be cleared by writing to the Reset Actel address 0x1C10.B46E, and a miscellaneous section (bits [15:12]) (see Appendix C). The data written is ignored.

2.1.4.1.1 Reg 0x0 - Reset Cause Register

2.1.4.1.1.1 Bit 0 - DRAM Error Reset

This flag is used to indicate that the navigation processor was reset due to a navigation processor DRAM memory access error.
0 = Not-Asserted; 1 = Asserted.

2.1.4.1.1.2 Bit 1 - GNS Reset

This flag is used to indicate that the navigation processor was reset due to a GNS reset.
0 = Not-Asserted; 1 = Asserted.

2.1.4.1.1.3 Bit 2 - Watchdog Reset

This flag is used to indicate that the navigation processor was reset due to a watchdog time-out.
0 = Not-Asserted; 1 = Asserted.

2.1.4.1.1.4 Bit 3 - NP Initiated Reset

This flag is used to indicate that the navigation processor was reset due to a navigation processor initiated reset.
0 = Not-Asserted; 1 = Asserted.

2.1.4.1.1.5 Bit 4 - Master Reset

This flag is used to indicate that the navigation processor was reset by an IEM master reset.
0 = Not-Asserted; 1 = Asserted.

2.1.4.1.1.6 Bit 5 - EDAC Error Reset

This flag is used to indicate that the navigation processor was reset due to a navigation processor EDAC double-error.
0 = Not-Asserted; 1 = Asserted.

2.1.4.1.1.7 Bit 6 - Console Reset

This flag is used to indicate that the navigation processor was reset due to a console reset.
0 = Not-Asserted; 1 = Asserted.

2.1.4.1.1.8 Bit 7 - Master Reset GTA Disable

This flag is used to indicate that the GTA I/O access was disabled due to an IEM master reset.
0 = Not-Asserted; 1 = Asserted.

2.1.4.1.1.9 Bit 8 - Trk. Processor GTA I/O Disable

This flag is used to indicate that the GTA I/O access was disabled by tracking processor software.
0 = Not-Asserted; 1 = Asserted.

2.1.4.1.1.10 Bit 9 - Nav. Processor GTA I/O Disable

This flag is used to indicate that the GTA I/O access was disabled by navigation processor software.
0 = Not-Asserted; 1 = Asserted.

2.1.4.1.1.11 Bit 10 - DRAM Error GTA Disable

This flag is used to indicate that the GTA I/O access was disabled due to a tracking processor DRAM access error.
0 = Not-Asserted; 1 = Asserted.

2.1.4.1.1.12 Bit 11 - EDAC Error GTA Disable

This flag is used to indicate that the GTA I/O access was disabled due to a tracking processor EDAC double-error.
0 = Not-Asserted; 1 = Asserted.

2.1.4.1.1.13 Bit 12 - Reserved

Not used.

2.1.4.1.1.14 Bit 13 - Nav. Processor Reset Asserted

This flag is used to determine if the navigation processor is being held in reset.
0 = Not-Asserted; 1 = Asserted.

2.1.4.1.1.15 Bit 14 - Console Enabled Input

This flag is used to indicate if the GNS GSE is connected and enabled.
0 = Not-Asserted; 1 = Asserted.

2.1.4.1.1.16 Bit 15 - Reserved

Not used.

2.1.4.2 Access Data Width

The data is accessed as 16-bit words, thus the least-significant address bit must be zero.

2.1.4.3 Address Space

The decoded address space for the Actel is 0x1C10.0000 to 0x1C10.FFFF. Note that bits b24-b25 are utilized to select 1 of 4 I/O address segments, each of which have wait-state values which can be set independently. These bits are defined as b24=0 and b25=0 to select the SPEC3 segment.

2.1.4.4 Discrete Outputs

See Appendix C for a complete list of all navigation processor discrete outputs.

2.1.5 PCI Actel Registers

2.1.5.1 Number of Registers

There are eight PCI status/control registers which are accessible by the navigation processor of

which only three will normally be accessed. The others are intended to be accessed only by the PCI master (i.e. C&DH subsystem).

2.1.5.1.1 Reg 0x6 - Transaction Status Register

Only bits b5 & b6 will normally be accessed by the GNS. The other bits are intended to be utilized only by the PCI master (i.e. C&DH subsystem).

2.1.5.1.1.1 Bit 5 - Flash Memory Busy

This flag is used to determine if the Flash memory is in a busy state.
0 = Not-Busy; 1 = Busy.

2.1.5.1.1.2 Bit 6 - IEM ID

This flag is used to identify in which IEM the GNS computer resides.
0 = IEM A; 1 = IEM B.

2.1.5.1.2 Reg 0x8 - PCI Buffer Interrupt Acknowledge

A write access to this register acknowledges the interrupt caused by a write by the C&DH to the PCI buffer address 0x0FFF. The data written is ignored.

2.1.5.1.3 Reg 0xA - GTA 1PPS Interrupt Acknowledge

A write access to this register acknowledges the GTA steered 1PPS interrupt. The data written is ignored.

2.1.5.2 Access Data Width

The data is accessed as 16-bit words, thus the least-significant address bit must be zero.

2.1.5.3 Address Space

The decoded address space for the Actel is 0x1C18.0000 to 0x1C18.000F. Note that bits b24-b25 are utilized to select 1 of 4 I/O address segments, each of which have wait-state values which can be set independently. These bits are defined as b24=0 and b25=0 to select the SPEC3 segment.

2.1.6 PCI Dual-Port RAM Buffer

See Appendix A for memory map.

2.1.6.1 Memory Size

The size of the navigation processor PCI dual-port RAM is 8KB.

2.1.6.2 Access Data Width

The data is accessed as 16-bit words, thus the least-significant address bit must be zero.

2.1.6.3 Address Space

The decoded address space for the PCI dual-port RAM is 0x1D20.0000 to 0x1D20.1FFF. Note that bits b24-b25 are utilized to select 1 of 4 I/O address segments, each of which have wait-state values which can be set independently. These bits are defined as b24=1 and b25=0 to select the SPEC2 segment.

2.1.7 Navigation Processor/Tracking Processor Dual-Port RAM Buffer

This memory buffer is logically divided into two sections of 4KB each. Although the entire memory space is both read and write accessible to the navigation processor. the tracking processor has only read access to the lower half (and full read/write access to the upper half). The lower half is used to provide 'pseudo non-

volatile' memory to the tracking processor and is used during the boot process to provide both the boot code and application software to the tracking processor. After booting, the lower memory space can be used by the navigation processor to provide data to the tracking processor, and the upper half can be used for bi-directional data transfers between the processors.

2.1.7.1 Memory Size

The size of the navigation processor to tracking processor dual-port RAM is 8KB.

2.1.7.2 Access Data Width

The data is accessed as 16-bit words, thus the least-significant address bit must be zero.

2.1.7.3 Address Space

The decoded address space for the PCI dual-port RAM is 0x1D28.0000 to 0x1D28.1FFF. Note that bits b24-b25 are utilized to select 1 of 4 I/O address segments, each of which have wait-state values which can be set independently. These bits are defined as b24=1 and b25=0 to select the SPEC2 segment.

2.1.8 GTA I/O Access

Access to the GTA registers by the tracking processor can be enabled or disabled by the navigation processor. This capability is provided so that the GTA register, used for steering the 1PPS output, can be protected from inadvertent writes which may cause unintended jumps in the 1PPS.

2.1.8.1 GTA I/O Access Enable

GTA I/O access can only be enabled by the navigation processor writing to the Reset Actel address 0x1C10.CB40. The data written is ignored.

2.1.8.2 GTA I/O Access Disable

The GTA I/O access can be disabled by the navigation processor by writing to the Reset Actel address 0x1C10.CB42. The data written is ignored.

2.2 Tracking Processor

2.2.1 Resets

The reset exception vector for the Mongoose V processor is 0xBFC0.0000.

2.2.1.1 Externally Initiated Resets

Note that there are only tracking processor externally generated resets.

2.2.1.1.1 IEM Master Reset

This reset is applied to the entire IEM including the GNS tracking processor.

2.2.1.1.2 Navigation Processor Initiated Reset

This reset is asserted by the navigation processor software.

2.2.2 Interrupts

There are 6 primary interrupts; namely, INT[0] thru INT[5] which are prioritized, INT[0] having the highest priority and INT[5] having the lowest priority. There are 32 expansion interrupts; namely, INT[5-0] thru INT[5-31] which are not prioritized and which are 'funneled' thru INT[5]. INT[5-0] thru INT[5-9] are user-defined interrupts and INT[5-10] thru INT[5-31] are used for internal functions.

2.2.2.1 Peripheral Interrupts

2.2.2.1.1 Navigation Processor Initiated Interrupt

This interrupt, INT[5-0], is asserted by the navigation processor software to alert the tracking processor that it has written data to the NP/TP interface buffer, and it occurs at a nominal rate of 1 per 180seconds. This interrupt is acknowledged by writing to the Reset Actel address 0x1C20.0000 (see Appendix C).

2.2.2.1.2 GTA AIC Interrupt

This interrupt, INT[2], is asserted by the AIC signal generated by the GTA hardware at a nominal rate of 1 per 667microseconds. This interrupt is acknowledged by writing to the GTA (at address BA+12, see Appendix B) and setting bit 2 = 1.

2.2.2.1.3 GTA MIC Interrupt

This interrupt, INT[4], is asserted by the MIC signal generated by the GTA hardware at nominal rate of 1 per second, but can be increased or decreased for testing purposes. This interrupt is acknowledged by writing to the GTA (at address BA+12, see Appendix B) and setting bit 3 = 1.

2.2.2.1.4 GTA Steered 1PPS Interrupt

This interrupt, INT[5-1], is asserted by the steered 1PPS signal generated by the GTA hardware at a 1 per second rate This interrupt is acknowledged by writing to the GTA (at address BA+12, see Appendix B) and setting bit 4 = 1.

2.2.2.2 Mongoose V Interrupts

The descriptions below only indicate which interrupts are asserted by the Mongoose V processor functions. See Applicable Document #5 (Section 1.4) for additional information.

2.2.2.2.1 Timer 1 Interrupt

This asserts INT[0].

2.2.2.2.2 Timer 2 Interrupt

This asserts INT[1].

2.2.2.2.3 Floating Point Unit Interrupt

This asserts INT[3].

2.2.2.2.4 UART 0 Interrupts

This asserts INT[5-11 thru 5-15].

2.2.2.2.5 UART 1 Interrupts

This asserts INT[5-17 thru 5-21].

2.2.2.2.6 Memory R/W Access Violation Interrupts

This asserts INT[5-22 and 5-23].

2.2.2.2.7 EDAC Error Interrupts

This asserts INT[5-30 and 5-31].

2.2.3 Reset Actel Registers

See Appendix C for a memory map and a complete list of all discrete I/O in the Reset Actel.

2.2.4 Memory Access

2.2.4.1 Static RAM

2.2.4.1.1 Memory Size

The size of the tracking processor SRAM is 2MB.

2.2.4.1.2 Access Data Width

The data is accessed as 32-bit words, thus the least-significant two address bits must be zero.

2.2.4.1.3 Address Space

The decoded address space for the tracking processor SRAM is 0x1000.0000 to 0x101F.FFFF. Note that bits b21-b26 are not decoded for this address space and, if used, will cause rollover into the decoded address space.

2.2.5 Navigation Processor/Tracking Processor Dual-Port RAM Buffer

This memory buffer is logically divided into two sections of 4KB each. Although the entire memory space is both read and write accessible to the navigation processor, the tracking processor has only read access to the lower half (and full read/write access to the upper half). The lower half is used to provide 'pseudo non-volatile' memory to the tracking processor and is used during the boot process to provide both the boot code and application software to the tracking processor. After booting, the lower memory space can be used by the navigation processor to provide data to the tracking processor, and the upper half can be used for bi-directional data transfers between the processors.

2.2.5.1 Memory Size

The size of the tracking processor to navigation processor dual-port RAM is 8KB. It is segmented into two 4KB sections by hardware, such that the lower half is read-only and the upper half is read/write.

2.2.5.2 Access Data Width

The data is accessed as 16-bit words, thus the least-significant address bit must be zero.

2.2.5.3 Address Space

The decoded address space for the PCI dual-port RAM is 0x1FC0.0000 to 0x1FC0.1FFF. Note that bits b24-b25 are utilized to select 1 of 4 I/O address segments, each of which have wait-state values which can be set independently. These bits are defined as b24=1 and b25=1 to select the SPEC0 segment. This segment must be selected since it is the segment which is where the processor reset vector points, and this dual-port RAM will contain the initial tracking processor boot-up software.

2.2.6 GTA Registers

See Appendix B for memory map, and Applicable Documents Section 1.4, item #6.

2.2.6.1 Number of Registers

There are (206) registers accessible to the tracking processor. 14 of the registers are for control/status, and 16 registers are designated for each of 12 tracking channels. See Applicable Document #6 (Section 1.4) for additional information.

2.2.6.2 Access Data Width

The data is accessed as 16-bit words, thus the least-significant address bit must be zero.

2.2.6.3 Address Space

The decoded address space for the GTA registers is 0x1D30.0000 to 0x1D37.FFFF. Note that

bits b24-b25 are utilized to select 1 of 4 I/O address segments, each of which have wait-state values which can be set independently. These bits are defined as b24=1 and b25=0 to select the SPEC2 segment.

2.2.7 GTA I/O Access

2.2.7.1 GTA I/O Access Enable

GTA I/O access can only be enabled by the navigation processor.

2.2.7.2 GTA I/O Access Disables

The Reset Actel will generate an interrupt to the navigation processor for any cause of a GTA I/O access disable.

2.2.7.2.1 Master Reset GTA Disable

The GTA I/O access is disabled if the GNS tracking processor receives an IEM master reset. This reset is applied to the entire IEM including the GNS tracking processor.

2.2.7.2.2 Tracking Processor Initiated GTA Disable

The GTA I/O access can be disabled by the tracking processor by writing to the Reset Actel address 0x1C20.0002.

2.2.7.2.3 Navigation Processor Initiated GTA Disable

The GTA I/O access can be disabled by the navigation processor.

2.2.7.2.4 EDAC Unrecoverable Double-Error GTA Disable

The GTA I/O access is disabled if the tracking processor EDAC circuit detects that the last memory access has two or more bit errors which is non-recoverable condition.

2.2.7.2.5 Invalid DRAM Address Space Access GTA Disable

The GTA I/O access is disabled if the tracking processor attempts to access memory in the address range of 0x0000.0000 to 0x0FFF.FFFF. These addresses are reserved for DRAM which does not exist in the tracking processor hardware.

Appendix A

Rev2	09/30/1997					
PCI Buffer Starting Byte Offset	PCI Buffer Ending Byte Offset	Byte Count	Word Count	Field Description	Buffer Id	Direction
0x0000	0x0021	34	17	Spacecraft Attitude	0	GNS Input
0x0022	0x0023	2	1	*Reserved*	0	
0x0024	0x0843	2080	1040	Telecommand Packet	0	GNS Input
0x0844	0x0845	2	1	*Reserved*	0	
0x0846	0x08CB	134	67	Unpacketized Data	0	GNS Output
0x08CC	0x08CD	2	1	*Reserved*	0	
0x08CE	0x09D3	262	131	Packet #1	0	GNS Output
0x09D4	0x09D5	2	1	*Reserved*	0	
0x09D6	0x0ADB	262	131	Packet #2	0	GNS Output
0x0ADC	0x0ADD	2	1	*Reserved*	0	
0x0ADE	0x0BE3	262	131	Packet #3	0	GNS Output
0x0BE4	0x0BE5	2	1	*Reserved*	0	
0x0BE6	0x0CEB	262	131	Packet #4	0	GNS Output
0x0CEC	0x0CED	2	1	*Reserved*	0	
0x0CEE	0x0DF3	262	131	Packet #5	0	GNS Output
0x0DF4	0x0DF5	2	1	*Reserved*	0	
0x0DF6	0x0EFB	262	131	Packet #6	0	GNS Output
0x0EFC	0x0EFD	2	1	*Reserved*	0	
0x0EFE	0x0F1F	34	17	Spacecraft Attitude	1	GNS Input
0x0F20	0x0F21	2	1	*Reserved*	1	
0x0F22	0x1741	2080	1040	Telecommand Packet	1	GNS Input
0x1742	0x1743	2	1	*Reserved*	1	
0x1744	0x17C9	134	67	Unpacketized Data	1	GNS Output
0x17CA	0x17CB	2	1	*Reserved*	1	
0x17CC	0x18D1	262	131	Packet #1	1	GNS Output
0x18D2	0x18D3	2	1	*Reserved*	1	
0x18D4	0x19D9	262	131	Packet #2	1	GNS Output
0x19DA	0x19DB	2	1	*Reserved*	1	
0x19DC	0x1AE1	262	131	Packet #3	1	GNS Output
0x1AE2	0x1AE3	2	1	*Reserved*	1	
0x1AE4	0x1BE9	262	131	Packet #4	1	GNS Output
0x1BEA	0x1BEB	2	1	*Reserved*	1	
0x1BEC	0x1CF1	262	131	Packet #5	1	GNS Output
0x1CF2	0x1CF3	2	1	*Reserved*	1	
0x1CF4	0x1DF9	262	131	Packet #6	1	GNS Output
0x1DFA	0x1DFB	2	1	*Reserved*	1	
0x1DFC	0x1DFD	2	1	Vector Word		GNS Output
0x1DFE	0x1E01	4	2	Spacecraft Time		GNS Input
0x1E02	0x1E05	4	2	Separation Time		GNS Input
0x1E06	0x1E07	2	1	New Data Buffer		GNS Input
0x1E08	0x1E09	2	1	New Data Available		GNS Input
0x1E0A	0x1FF7	494	247	*Spare*		
0x1FF8	0x1FF9	2	1	*(Intr Addr3) - Not Used*		GNS Input
0x1FFA	0x1FFB	2	1	*(Intr Addr2) - Not Used*		GNS Input
0x1FFC	0x1FFD	2	1	*(Intr Addr1) - Not Used*		GNS Input
0x1FFE	0x1FFF	2	1	(Intr Addr0) - C&DH 1PPS		GNS Input

PCI Buffer Memory Map

Appendix B

Base Address = BA = 0x1D30.0000

Register	Address	I/O	Number of bits
ant_tracker_sela	BA	input	12
mic_div_reg	BA	output	14
ant_tracker_selb	BA+2	input	12
pps_mic_off_lower	BA+2	output	16
ch_code_select	BA+4	input	12
pps_mic_off_upper	BA+4	output	11
nco_carr_clear	BA+6	input	12
tr_dat_ltch	BA+6	output	12
nco_code_clear	BA+8	input	12
ant0_agc	BA+8	output	12
corr_config	BA+10	input	9
timing_config	BA+12	input	6
(unused)	BA+14	bi	-
pps_div_lower	BA+16	bi	16
pps_div_upper	BA+18	bi	9
aux_decode1	BA+20	bi	16
aux_decode2	BA+22	bi	16
aux_decode3	BA+24	bi	16
aux_decode4	BA+26	bi	16

Addressing of the GTA assumes proper set-up of the SPEC register for 16-bit access

GTA Memory Map (p1 of 2)

Appendix B

Individual Tracker Addressing for tracker number x, x=1:12

Tracker Address (TA): TA = BA + 16*x

Register	Address	I/O	Number of bits
chx_carnco_phincr_upper	TA	input	16
chx_carnco_phase	TA	output	16
chx_carnco_phincr_lower	TA+2	input	8
chx_codenco_phase	TA+2	output	16
chx_code_phincr_upper	TA+4	input	16
chx_cacode_phase	TA+4	output	10
chx_code_phincr_lower	TA+6	input	8
chx_epoch_cnt	TA+6	output	10
chx_cacode_svphs	TA+8	input	10
chx_cyc_cnt_upper	TA+8	output	16
chx_epochaccum	TA+10	input	5
chx_cyc_cnt_lower	TA+10	output	16
chx_accum_ie	TA+12	output	16
chx_accum_ip	TA+14	output	16
chx_accum_il	TA+16	output	16
chx_accum_qe	TA+18	output	16
chx_accum_qp	TA+20	output	16
chx_accum_ql	TA+22	output	16
	TA+24		
	TA+26		
	TA+28		
	TA+30		

Addressing of the GTA assumes proper set-up of the SPEC register for 16-bit access

GTA Memory Map (p2 of 2)

Appendix C

Rev1 9/29/97	
NAVIGATION PROCESSOR	**PHY. ADDRESS**
Resets:	
Reset Watchdog	0x1C10.794C
Reset Navigation Processor	0x1C10.B466
Reset Tracking Processor	0x1C10.B468
Set GTA Reset Flip-Flop (Reset GTA)	0x1C10.7876
Clear GTA Reset Flip-Flop	0x1C10.7874
Cause Register:	
Read Navigation Processor/Tracking Processor Cause Register	0x1C10.0000
Clear Cause Register Navigation Processor Bits [6:0]	0x1C10.B464
Clear Cause Register Tracking Processor Bits [11:7]	0x1C10.B46E
Interrupts:	
Navigation Processor to Tracking Processor Interrupt	0x1C10.B46C
MIC-Delayed (TP to NP) Interrupt Acknowledge	0x1C10.B46A
GTA I/O Control:	
Enable GTA I/O Access	0x1C10.CB40
Disable GTA I/O Access	0x1C10.CB42
Flash Memory:	
Enable Flash Write	0x1C10.CB4A
Disable Flash Write	0x1C10.CB48
Enable Flash Reset	0x1C10.CB4E
Disable Flash Reset	0x1C10.CB4C
Test Outputs:	
Set Navigation Processor Test Point Flip-Flop #1	0x1C10.787A
Clear Navigation Processor Test Point Flip-Flop #1	0x1C10.7878
Set Navigation Processor Test Point Flip-Flop #2	0x1C10.787E
Clear Navigation Processor Test Point Flip-Flop #2	0x1C10.787C
TRACKING PROCESSOR	**PHY. ADDRESS**
Interrupts:	
MIC-Delayed (TP to NP) Interrupt	0x1C20.0004
Navigation Processor to Tracking Processor Interrupt Acknowledge	0x1C20.0000
GTA I/O Control:	
Disable GTA I/O Access	0x1C20.0002
Test Outputs:	
Set Tracking Processor Test Point Flip-Flop #1	0x1C20.000A
Clear Tracking Processor Test Point Flip-Flop #1	0x1C20.0008
Set Tracking Processor Test Point Flip-Flop #2	0x1C20.000E
Clear Tracking Processor Test Point Flip-Flop #2	0x1C20.000C

Reset Actel Memory Map

SEA-97-0092
14 Oct 97
ICR01DJB

To: Distribution

From: A. A. Chacos

Subject: Transmittal of TIMED GPS Navigation Subsystem Software-Hardware Interface Document.

Attachment: Software-Hardware Interfaces for the GPS Navigation Subsystem v1.0, 7363-9348, 29 Sep 97.

✓ The attached document is provided for your files.

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