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Command and Data Handling (C&DH)

Introduction

Common Processor

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C&DH Requirements

- **Same generic requirements as PDR**
  - **Uplink command processing**
  - **Stored command management**
  - **Telemetry data collection and processing**
  - **Mass storage of science and engineering data**
  - **Autonomous fault protection**
  - **Subsystem intercommunication**
- **The TIMED unique requirement is to achieve unprecedented spacecraft autonomy and seamless operation with mission operations**

Changes To C&DH Since PDR

- **The cross coupling between redundant IEMs via high speed data links and 1PPS signals is eliminated. This reduces software operating modes, reduces test time, and lowers cost.**
- **The baseline processor is the Mongoose-V. A successful build of this MIPS based processor had not been accomplished by PDR.**
- **A dual processor card design has been added for the GNS. The clock rate of each processor is 12-MHz**
- **Common Processor SRAM capacity is 2-megabytes instead of 4-megabytes**
- **Other changes internal to the C&DH system are highlighted**

The accompanying block diagram gives the partitioning of the command and data handling subsystem. The cards within the Integrated Electronics Module (IEM) are shown in the same order they are place in the physical housing. The processor/1553 card executes the C&DH software. It is the bus controller for the dual redundant MIL-STD-1553 data bus. The software is presented by Steve Williams. The hardware is presented by James Perschy. The solid state recorder holds 2.5 gigabit of data partitioned as Reed Solomon code blocks. It has multi sector capability. The recorder card, designed by Joe Bogdanski and George Theodorakos is presented by George Theodorakos. The Command and Telemetry (C&T) card digitizes voltages and temperature values within the IEM. It controls the I^2C bus which gathers external temperatures around the spacecraft. The C&T card serves as the interface and temporary buffer between the processor/1553 card and the uplink card. Steve Oden presents the C&T card. The framer on the downlink card formats telemetry frames. Reed Solomon code blocks are converted to CCSDS compatible packets. Packets are assembled into frames. John Penn presents the downlink framer. The critical command decoder decodes real-time commands and provides the interface between the IEM and the power switching unit. It sequences through commands under low voltage and other trip conditions. Steve Oden presents the critical command decoder. PCI is the communication bus within the IEM backplane. It is a multimaster synchronous bus tailored to meet the IEM communication requirements. Dan Rodriguez presents the PCI design. The Remote I interface Units (RIU) digitize temperatures throughout the spacecraft. The RIUs interface to the I^2C bus and the power lines provided by the IEM. The RIU design is presented by Al Reiter. The IEM testbed is used during all phases of C&DH hardware and software integration to validate design. Tom LeFevere presents the IEM testbed.

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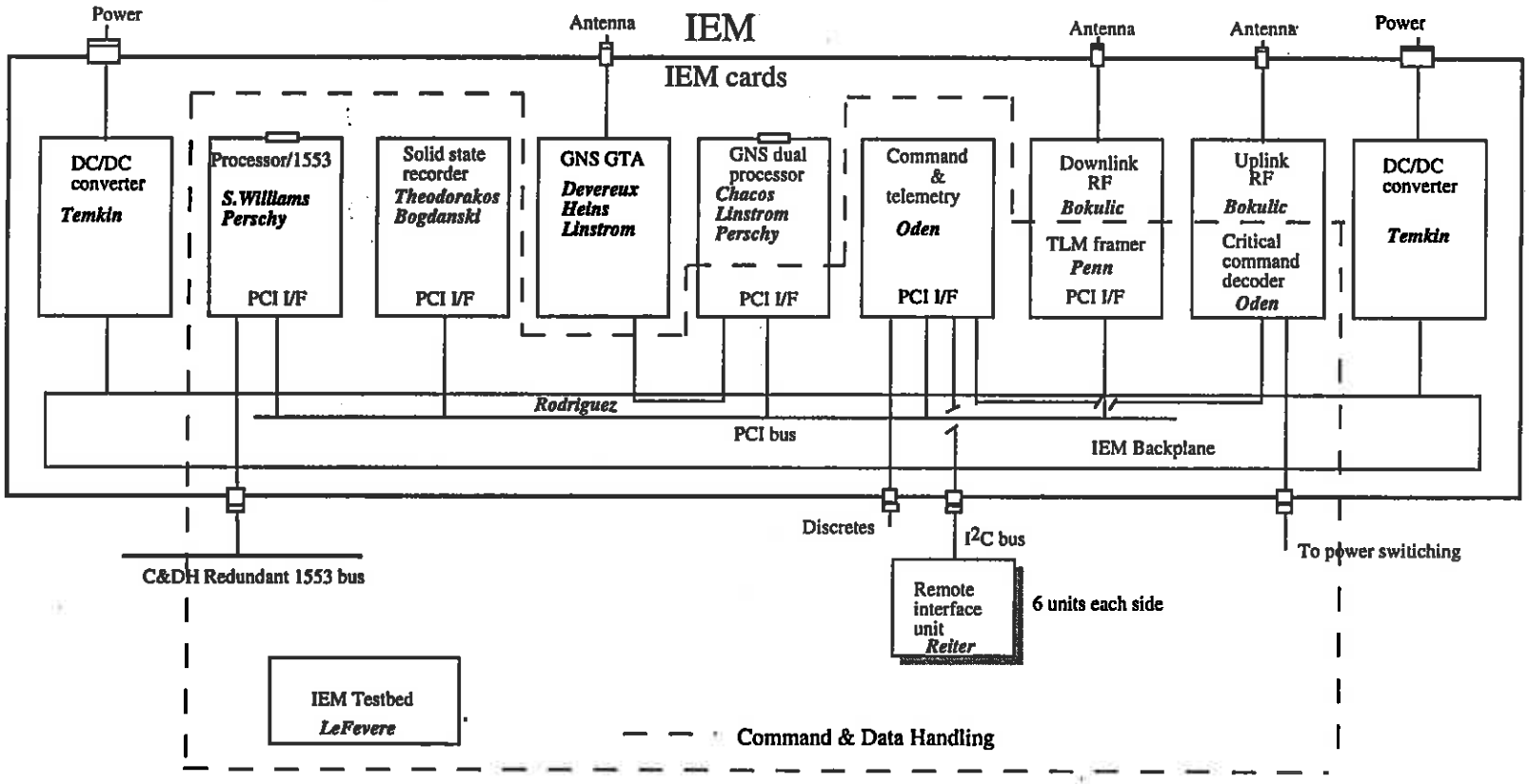
C&DH Partitioning



Processor Requirements (1 of 2)

- **CPU**
  - **32-bit architecture for ease of SW development**
  - **IEEE-754 floating point for navigation and attitude**
  - **Latchup free**
  - **No proton induced non-recoverable upsets**
- **Throughput**
  - **3-VAX MIPS minimum with separate C&DH, GNS, & Attitude Flight Computer (AFC) processors**
- **Memory capacity**
  - **2-megabyte EDAC SRAM, 4-megabyte EDAC Flash EEPROM, scrubbing to eliminate soft errors**

Processor Requirements (2 of 2)

- **Input/Output**
  - **MIL-STD-1553 for C&DH and AFC processors**
  - **PCI bus for C&DH and GNS processors**
  - **Local bus for GNS processor (16 address and 16 data lines)**
  - **Interrupts and discretes to meet C&DH, GNS, and AFC requirements. The driver is GNS.**
  - **All non-transformer coupled interfaces have series protection resistors**

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Processor Specification (1 of 2)

- **CPU**
  - **Mongoose-V MIPS based processor**
- **Throughput**
  - **3-VAX MIPS at 12 MHz using no-wait-state SRAM**
- **Memory**
  - **2- megabyte SRAM using 4-Meg Iridium/Motorola/Auston epi-MCM6246, 5 total for 32-bit word with 8-EDAC parity bits**
  - **4 -megabyte Flash EEPROM using Intel M28F008, 5 total for 32-bit word with 8-EDAC parity bits**
  - **1 -megabyte console boot ROM using Intel M28F008, one for 8-bit wide bus**

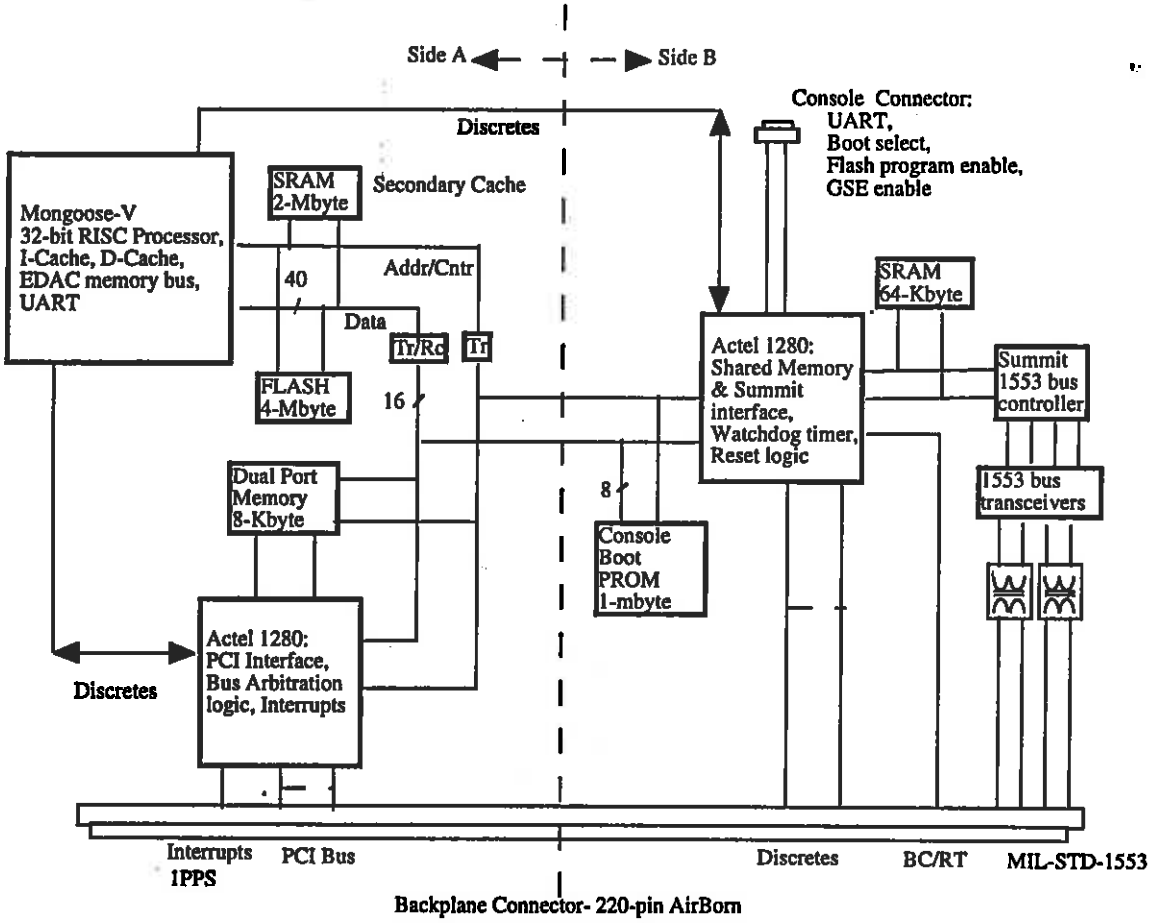
Correct per JAP 4/14/99

Processor Specification (2 of 2)

- **Input/Output**
  - **UTMC Summit 1553 protocol ASIC for NEAR SW heritage**
    - » **backplane BC/RT control**
    - » **backplane wired RT address**
  - **PCI with 8-Kbytes UTC138 dual port SRAM**
  - **Local bus for GNS dual processor card to GTA card**
- **Interrupts**
  - **12 total external interrupts used**
- **Power**
  - **+5V, 3.5-W peak at 12 MHz per processor w/o 1553, add 4-W peak for 1553 at 100% transmit**

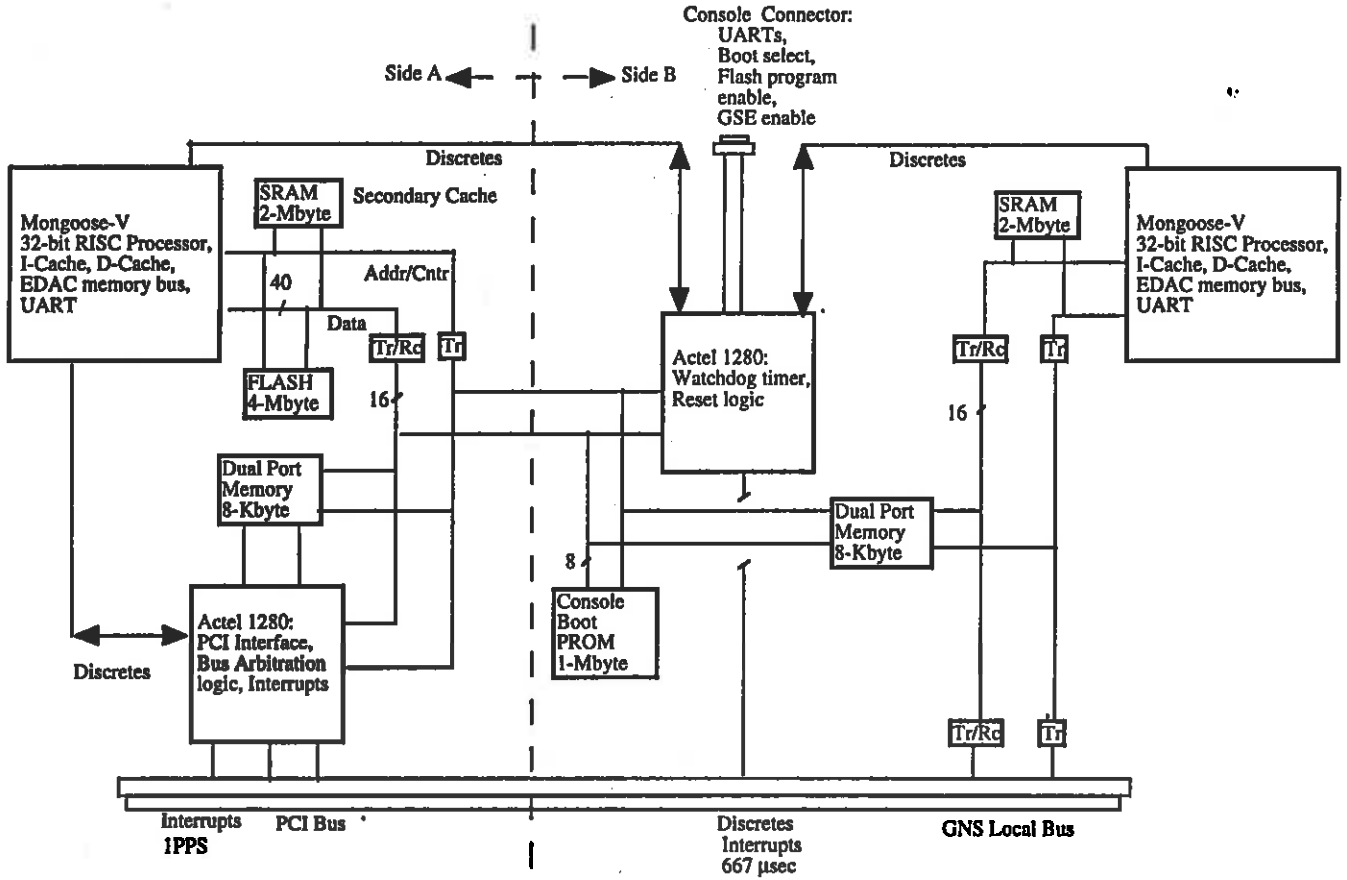
The processor/1553 card is partitioned onto two printed circuit boards. The A-side board contains the Mongoose-V microprocessor, 2-megabytes of SRAM, 4-megabytes of Flash EEPROM, 8-kilobytes of dual port memory and the PCI bus interface. The B-side contains the console interface, the console boot PROM, and the MIL-STD-1553 interface. The A and B sides are partitioned so the A side design may be reused for the GNS dual processor card. Each side contains one Actel-1280. On the A-side the main use of the Actel is The PCI protocol logic. On the B-side the Actel is used as the controller for the memory shared by the MIL-STD-1553 Summit bus controller and the Mongoose-V processor. The B-side Actel also contains console interface logic and the reset logic including the watchdog timer. This card design is used for both the C&DH processor and the Attitude Flight Computer.

Processor/1553 Card Block Diagram

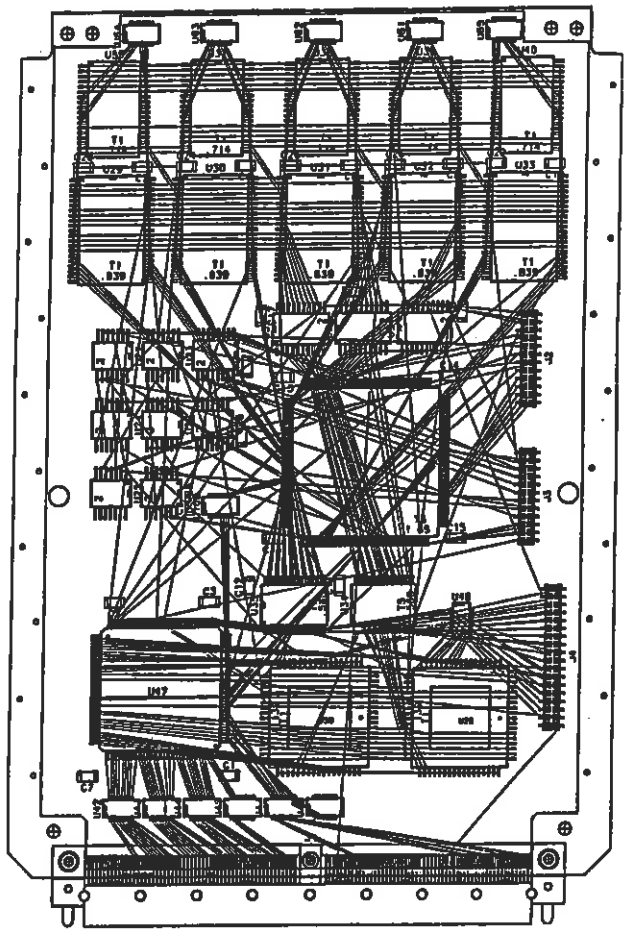


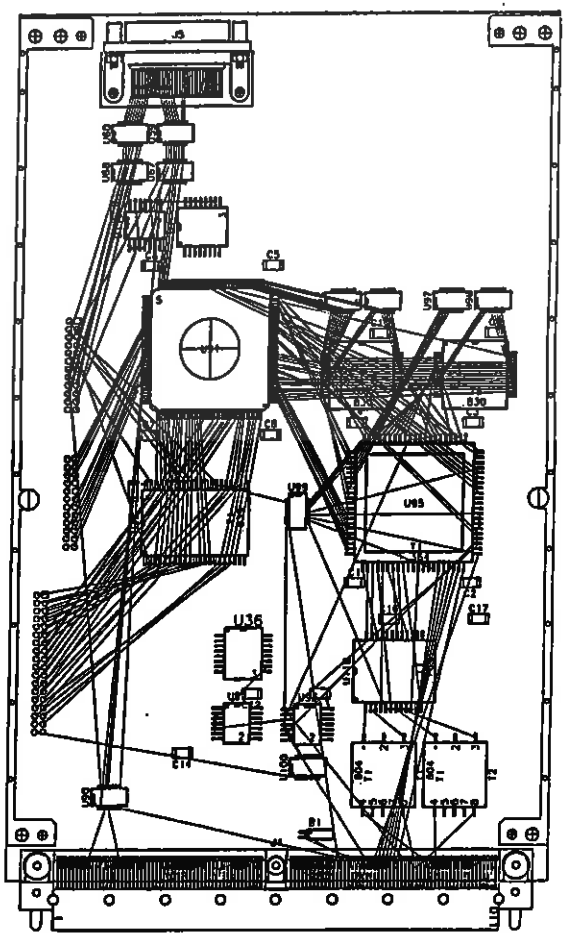
The dual processor card is partitioned onto two printed circuit boards. The A-side board is identical to A-side of the processor/1553 card. It contains the Mongoose-V microprocessor, 2-megabytes of SRAM, 4-megabytes of Flash EEPROM, 8-kilobytes of dual port memory and the PCI bus interface. The B-side contains the console interface, the console boot PROM, and the second processor. The second processor is supported by a dedicated 2-megabyte bank of SRAM. The first and second processor communicated with each other via an 8-kilobyte dual port memory located on the B-side board. The second processor boots through this dual port memory of which half is read-only to the second processor. Each side contains one Actel-1280. On the A-side the main use of the Actel is The PCI protocol logic. On the B-side the Actel contains the console interface logic and the reset logic including the watchdog timer. The B-side board has a local bus interface to the backplane connector for communicating with the GNS GTA card.

GNS Dual Processor Block Diagram



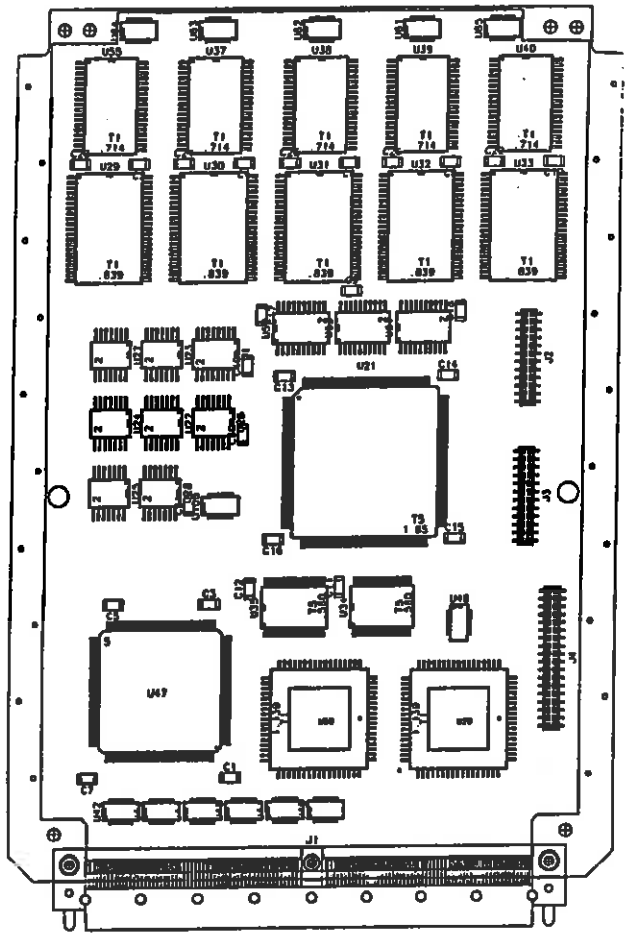
Backplane Connector- 220-pin AirBorn

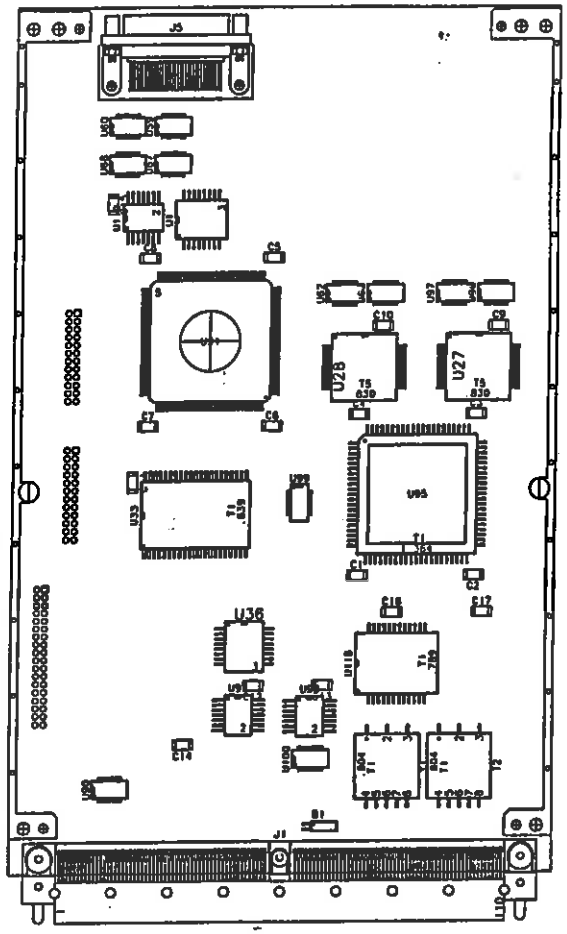


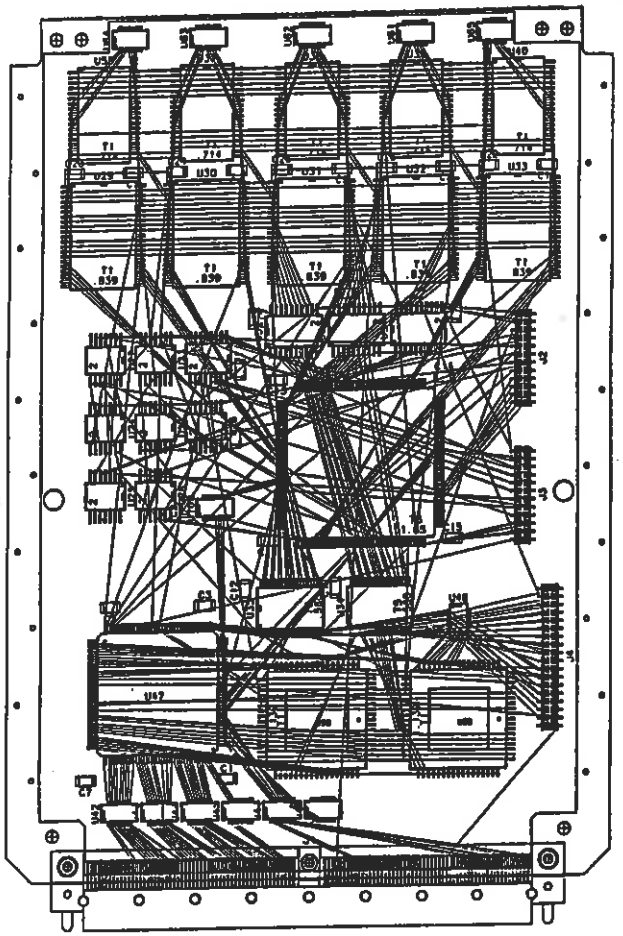


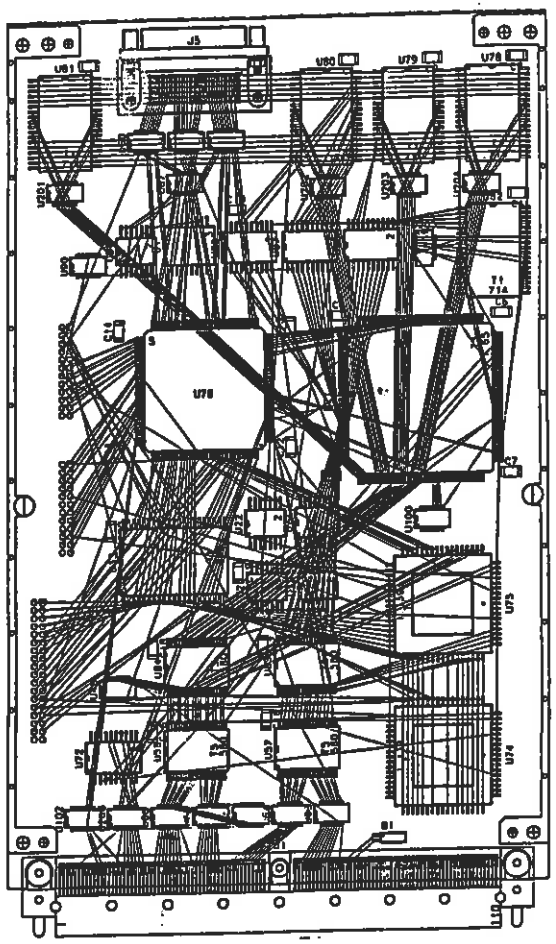
The processor/1553 card package design layout below was generated using Mentor Boardstation. Above is the layout with the interconnect guides turned on. Components are partitioned to minimize interconnect crossovers.

Processor/1553 Card Layout









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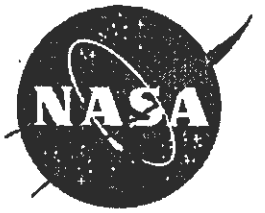

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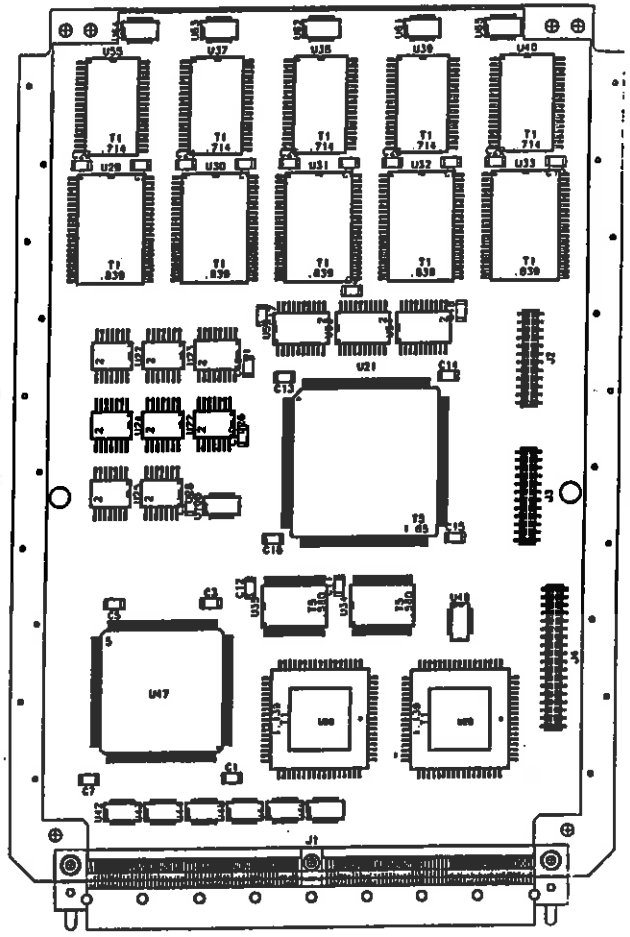
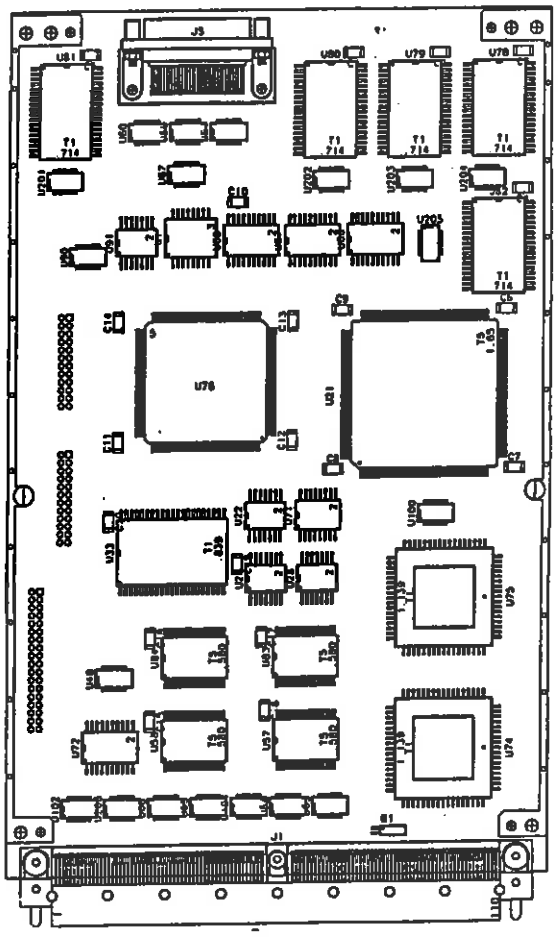
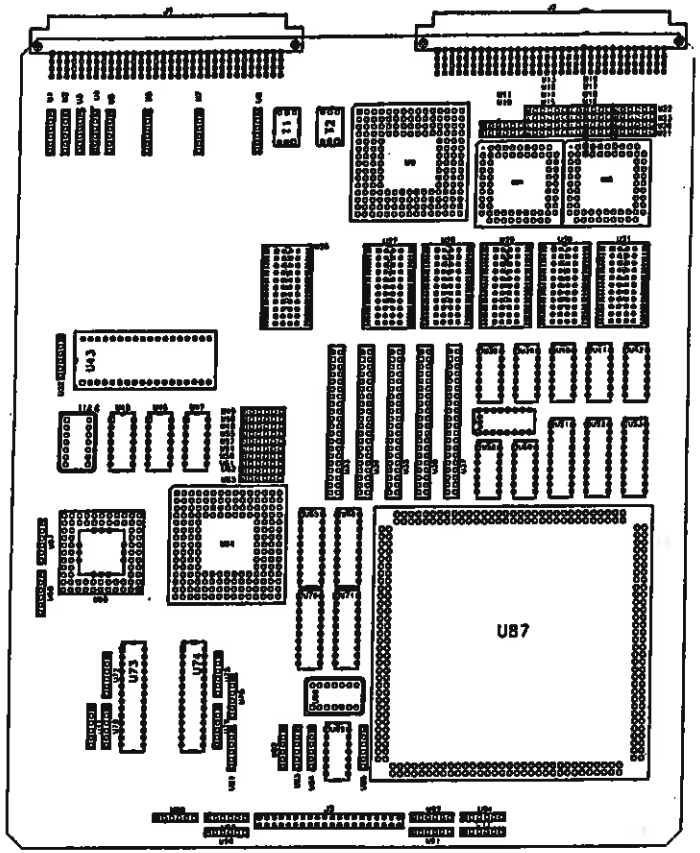
Dual Processor Card Layout

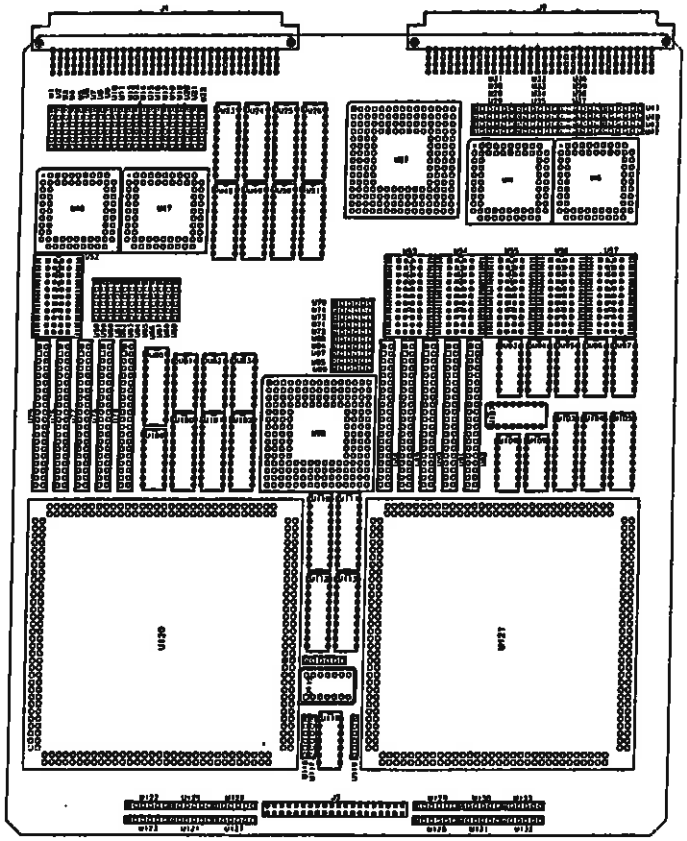




Processor/1553 Testbed Card



Dual Processor Testbed Card



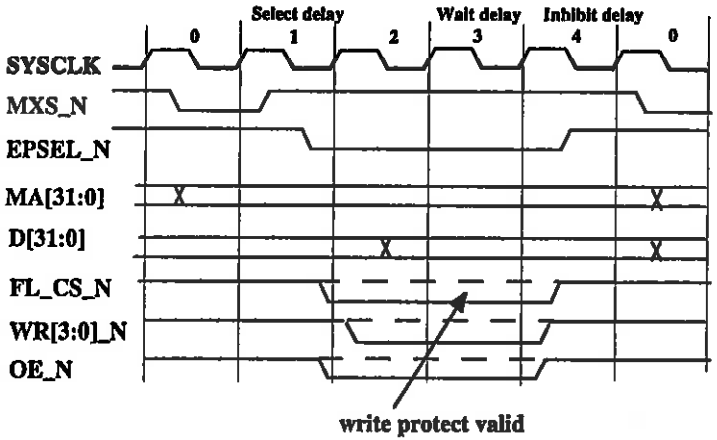
Above is a Mentor Boardstation generated layout of the test bed version of the processor/1553 card and the dual processor card. Both testbed cards are assembled and are in test.

Design Verification

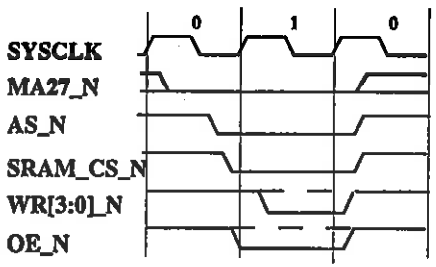
- **Perform detailed electrical design of the flight card**
  - **Parts are selected and their availability verified**
  - **Actel designs are simulated verifying their functional operation**
- **The flight card is partitioned and components placed using Mentor Boardstation design tool**
  - **Thermal analysis made**
  - **Preliminary fabrication feasibility review held**
- **A high fidelity breadboard of the electrical design is partitioned onto the test bed wire wrap card**
  - **Actel designs are back annotated for pin placement and routing and simulated using worst case delays**
- **The breadboard design is verified**

Timing for the major waveforms on the processor card are given. The waveforms give the number of clock cycles to perform the transaction, and the control signals involved in the transaction.

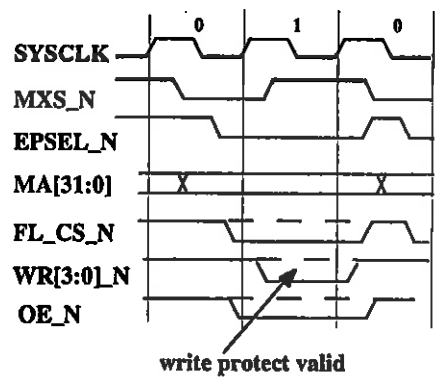
FLASH Timing: 1-select, 1-wait, & 1-inhibit



SRAM Timing

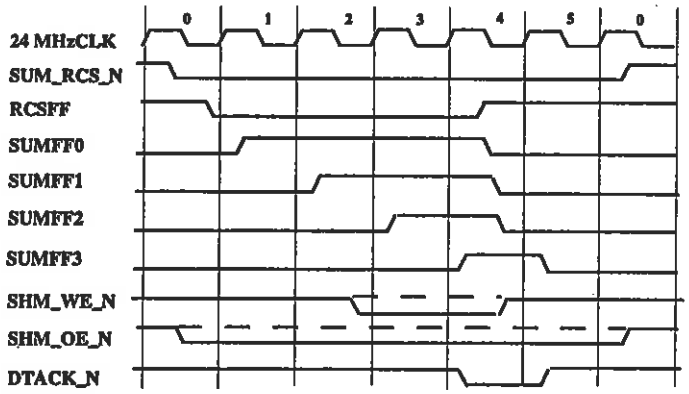


Flash no-wait-state Timing (not operational)

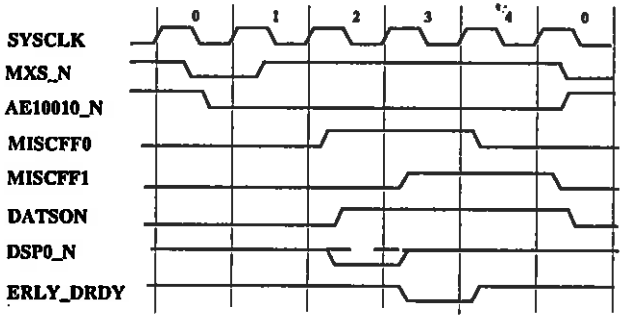


Processor Card Timing Diagrams

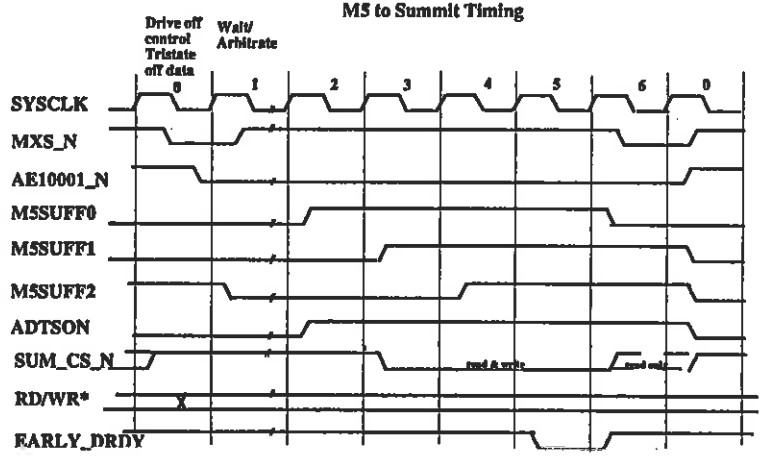
Summit to Shared Memory Timing



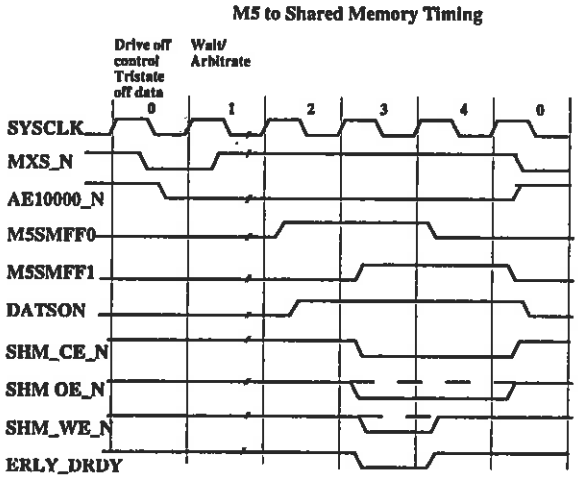
M5 to Watchdog Timer & Discrete Out Timing



M5 to Summit Timing

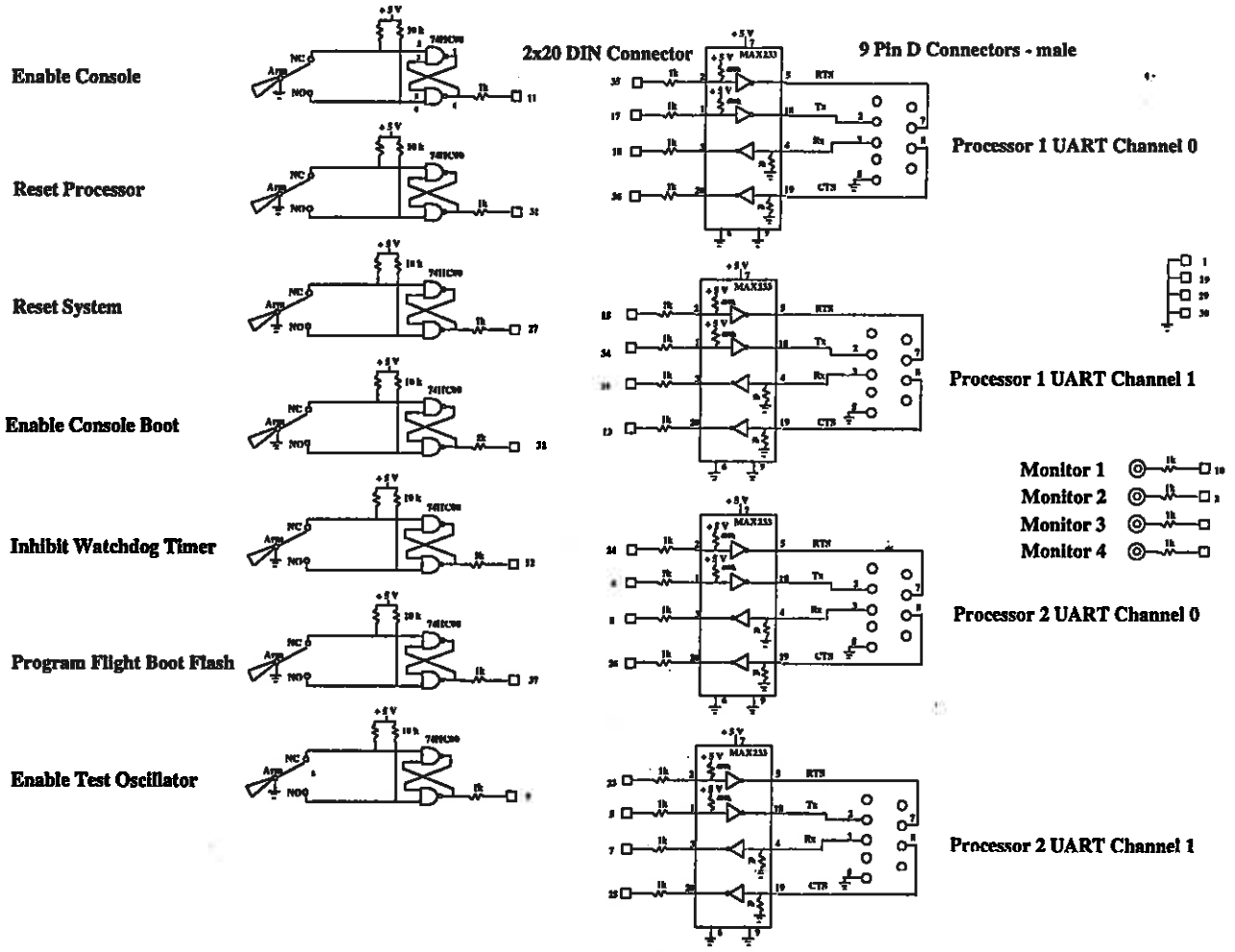


M5 to Shared Memory Timing



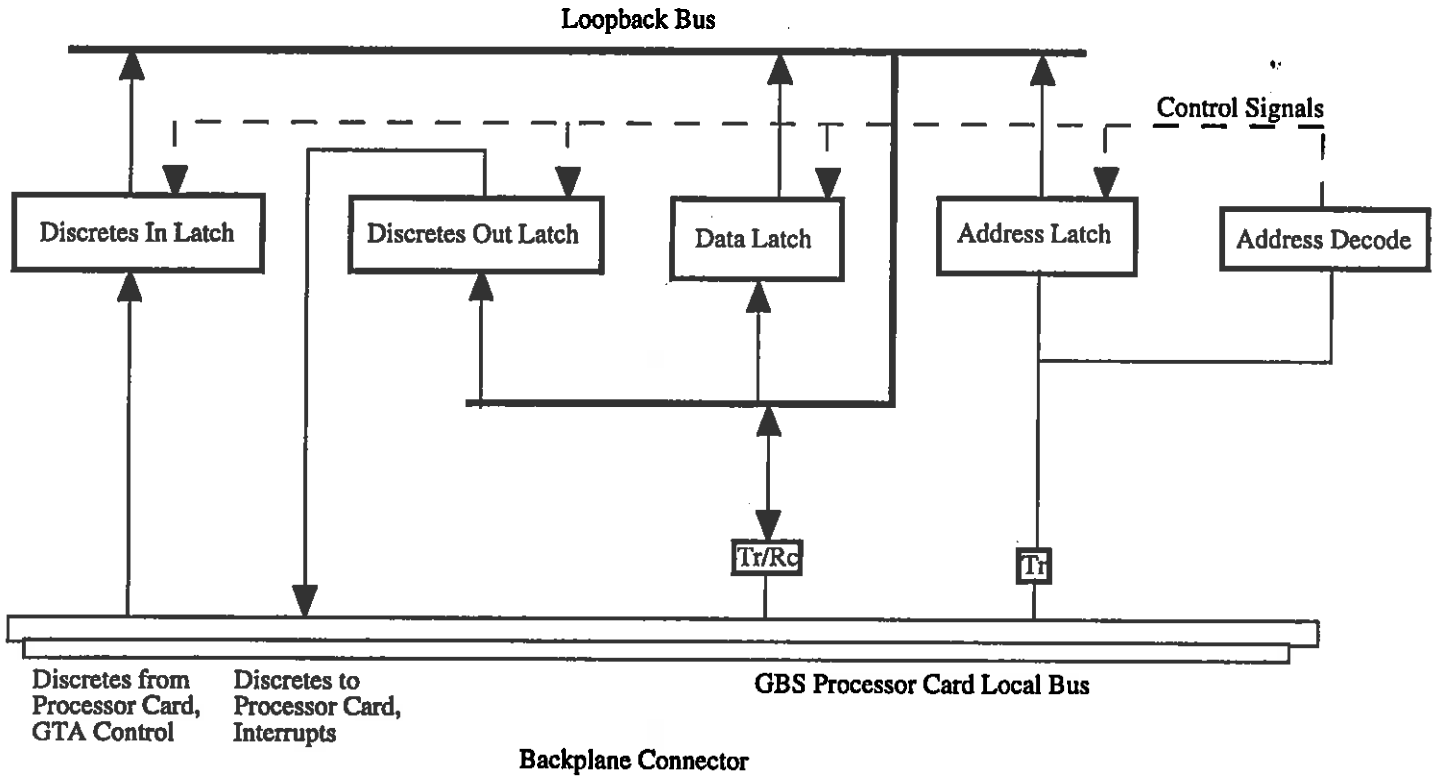
The processor console is used during software development. The in-flight boot code is loaded through the console. The console may be attached to the processor card when the front panel of the housing is removed. The final opportunity to modify the processor boot code in the spacecraft will come before assembly for environmental tests in mid 1999.

Processor Console



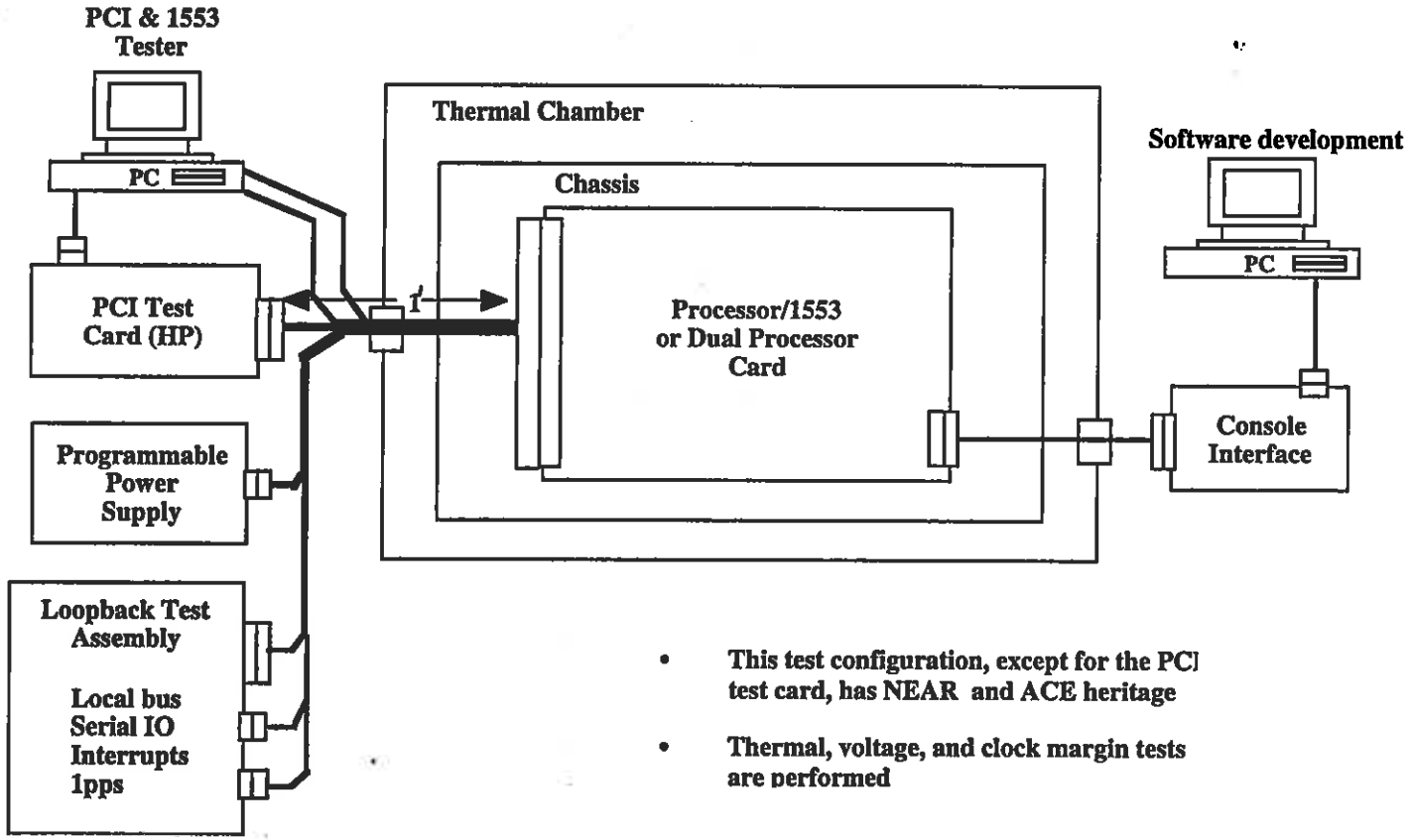
The GNS local bus test card facilitates stand alone testing of the dual processor for the GNS. Its purpose is to exercise all the interface lines between the GNS processor and GTA cards. Both data and address signals are latched when the processor writes to the test card. Then, both address and data are read back and checked. The discrete interfaces to and from the processor are also checked.

GNS Processor Loopback Test Card



The test configuration shown below accommodates both the processor/1553 card and the dual processor card. The pinout on the backplane connector for both configurations are compatible. The local bus pins needed for the dual processor configuration are not used for the processor/1553 configuration.

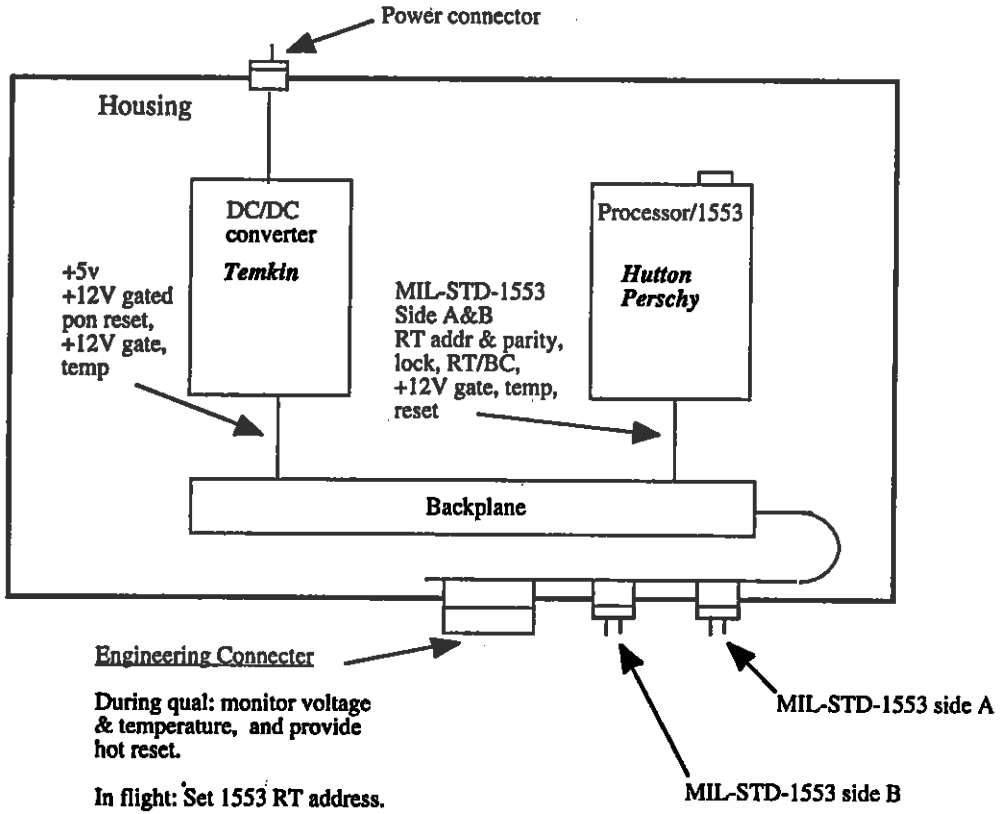
Common Processor Test Configuration



- This test configuration, except for the PCI test card, has NEAR and ACE heritage
- Thermal, voltage, and clock margin tests are performed

The flight computer uses two cards developed for the IEM. The DC/DC converter card uses a subset of the voltages generated for the IEM. The processor/1553 card is identical to the C&DH card used in the IEM although the PCI interface on the A-side of the card is not utilized. The two in-flight interfaces used are the power and the dual redundant MIL-STD-1553. The engineering connector is capped with a jumper plug defining the flight computer's MIL-STD-1553 remote terminal address.

Attitude Flight Computer (AFC)



Below is a computer aided design assembly of the flight computer. Shown are the two extended SEM-E size IEM cards inserted in the housing. The power connector is mounted on the front cover and the redundant MIL-STD-1553 connectors and the engineering connector is mounted on the back cover.

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AFC Assembly