Solid State Recorder

Critical Design Review
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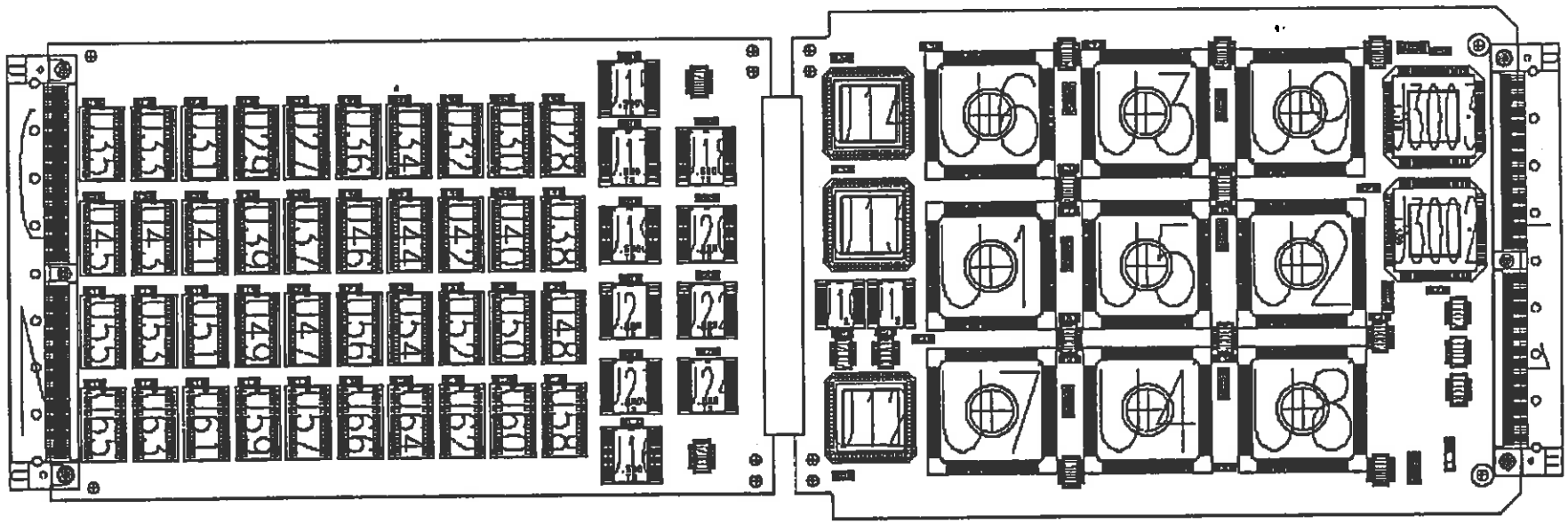
Solid State Recorder (SSR)



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SSR Design Considerations

Requirement

- 1.9-Gbits User Data Space
- Peak Write Rate 30-Kbits/sec
- Peak Read Rate 4-Mbits/sec
- Simultaneous Read & Write
- Random Read & Write
- Low Power Mode
- Map Around Bad Memory

Performance

- Total Data Capacity (2.5-Gbits)
- 8-Mbits/sec Peak Write Data Rate
- 8-Mbits/sec Peak Read Data Rate
- Simultaneous Read & Write (8-Mbits/sec combined)
- Random Data Access, at the RS Code Block level, 244-Bytes / Read Solomon (RS) Code Block
- Low Power Mode
  - Memory Refresh Only (2.1-watts)
  - No Memory Retention (1.1-watts)
- Auto Incrementing Read/Write Pointers can be set by Processor to map around bad blocks

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SSR Changes Since PDR

CDR

- Max Data Rate 8-Mbits
- Expected EOL Power 5.35W
- 9 Actels on Board
- 8 RAMs in Refresh

PDR

- Max Data Rate 10-Mbits
- Expected EOL Power 4.5W
- 8 Actels on Board
- 4 RAMs in Refresh

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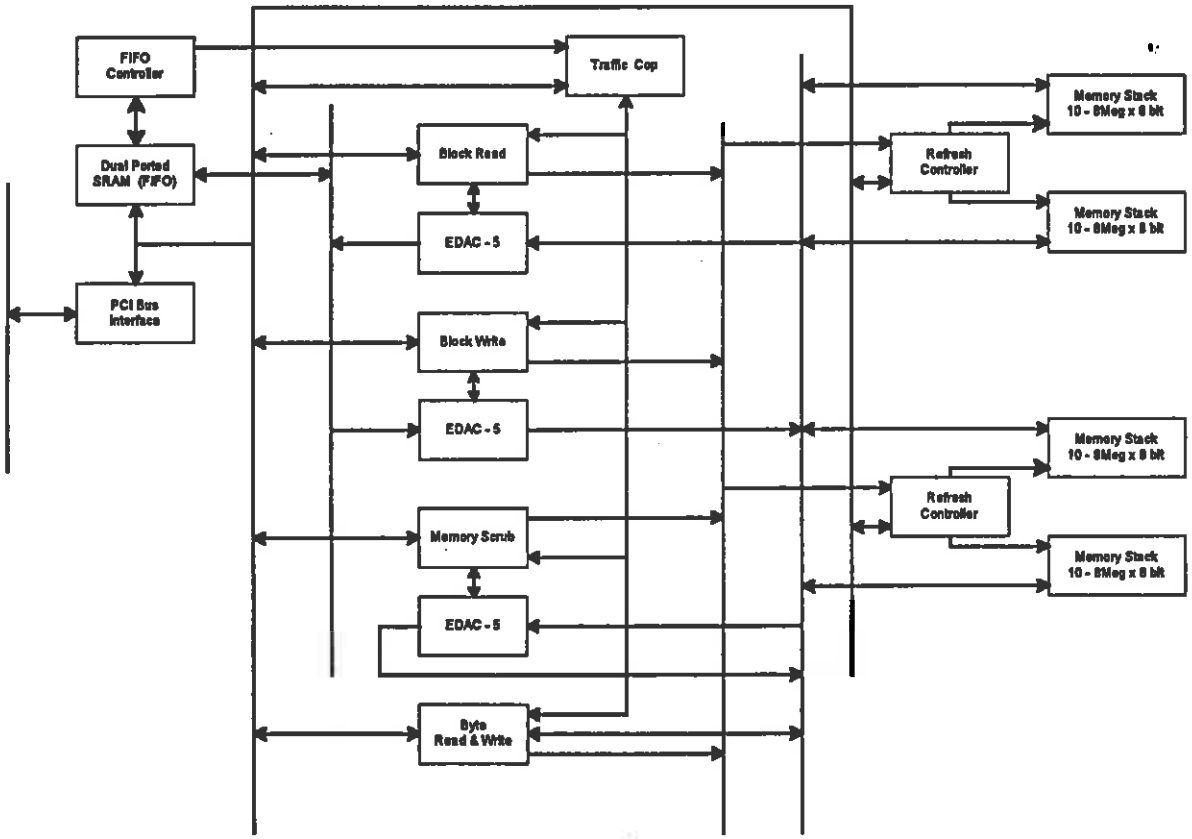
SSR Design Diagram



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SSR Operation (Data Movement)

PCI compatible target device

- **Write Port**

  1 RS code block (244 bytes) per PCI transaction

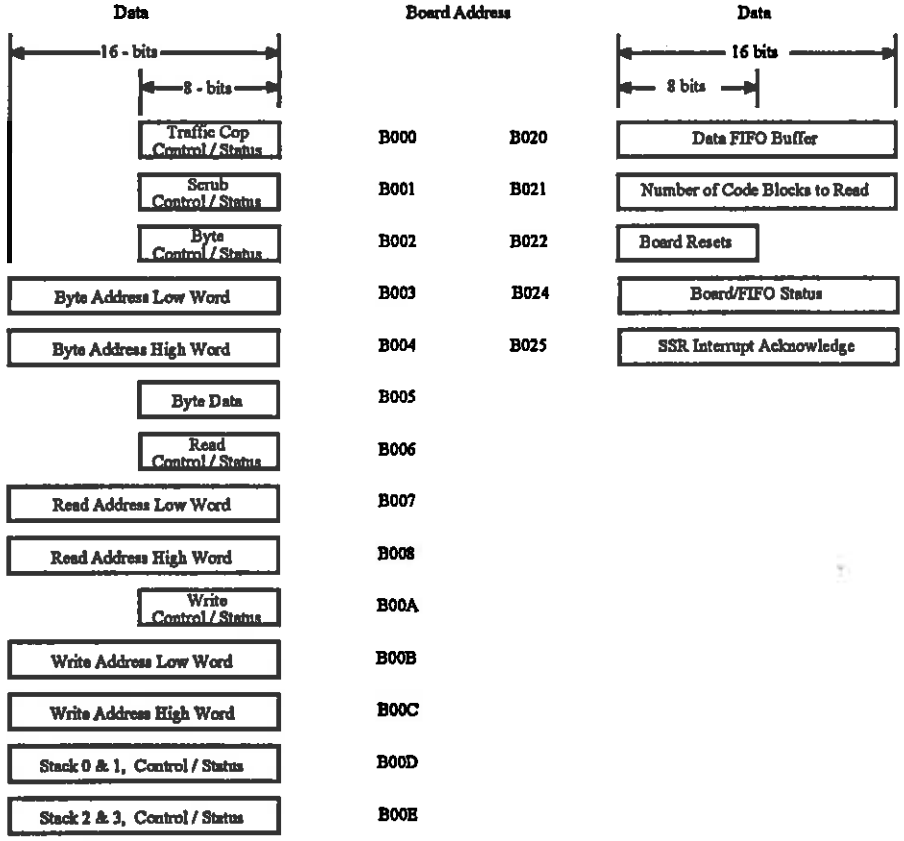
- **Read Port**

  1 RS code block + 2 error reporting bytes per PCI transaction

- **Byte Port**

  byte read & write (primarily for test)

SSR Operation (Addressing)



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SSR Operation (Error Management)

EDAC-5 Designed by University of New Mexico

- Reed Solomon encoding, RS code (254,244)
- Correct up to 5-Bytes with errors per block
- Scrub rate set by processor

Actel 1280A

- Triple voting and self refreshing logic (@ 12MHz, 1 error every 6 years)

Memory

- Memory Error Rate (Samsung 64-Mbit DRAM, 3.3Volt)
  $<10^{-12}$ Errors/bit/Sec
- Memory Error Rate With EDAC-5 (Probability of >5-bytes in errors per block)
  $<10^{-21}$ (24 hour scrub rate)
  $<10^{-25}$ (4 hour scrub rate)

SSR Operation (Power at Board)

Operating

- Actel 4.5 watts
- Memory 0.4 watts
- EDAC-5 0.45 watts
- Total 5.35 watts

Standby

- Actel 0.9 watts
- Memory 0.1 watts
- EDAC-5 0.1 watts
- Total 1.1 watts

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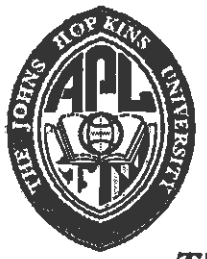

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SSR Issues & Concerns

No Design Issues or Concerns

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SSR Test Status

All nine ACTELs completed

- Simulated over full Military temperature and voltage range

Breadboard used for full functional testing

- PCI interface driven by PCI Exerciser/Analyzer purchased from Hewlett-Packard

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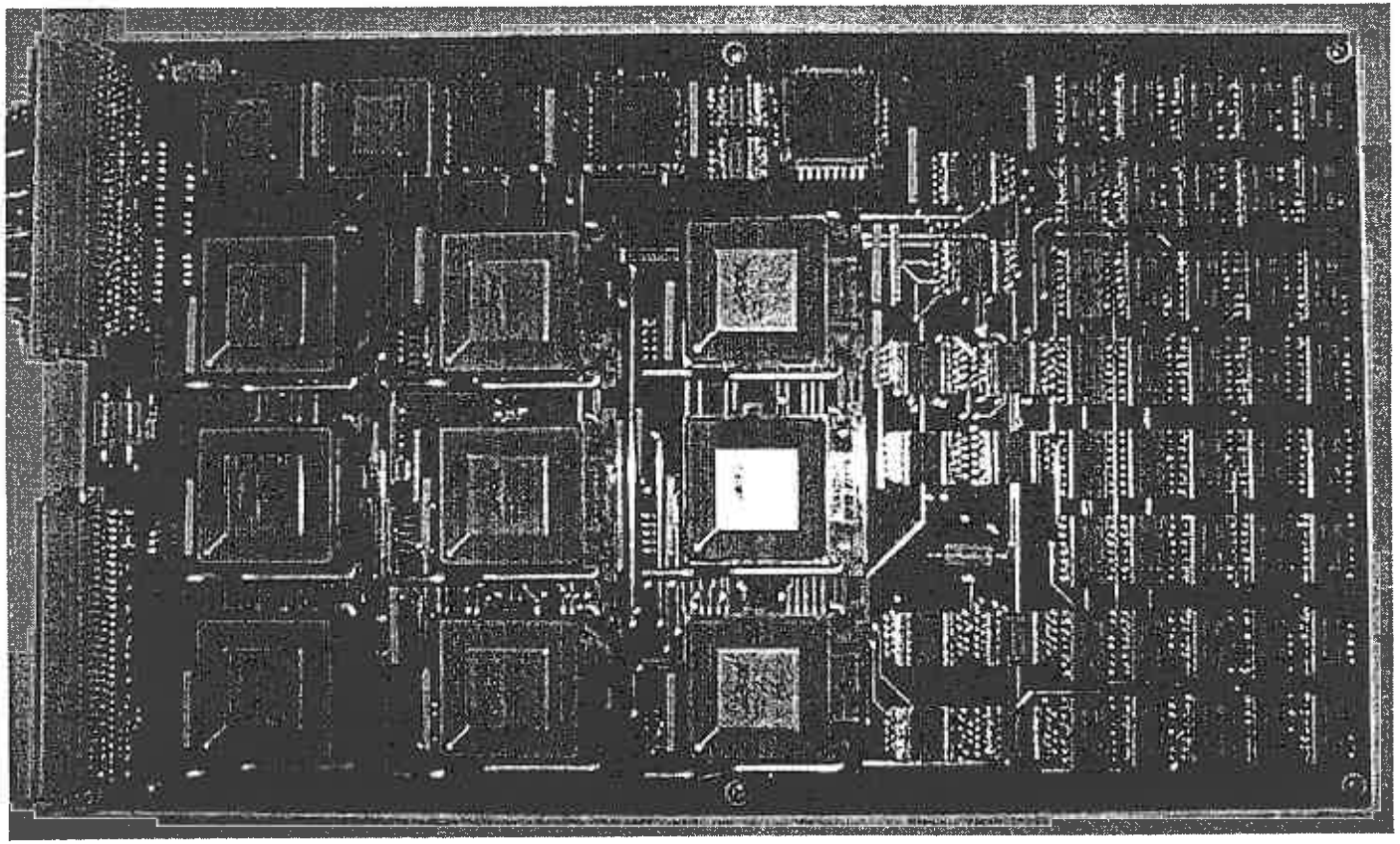
Bread Board



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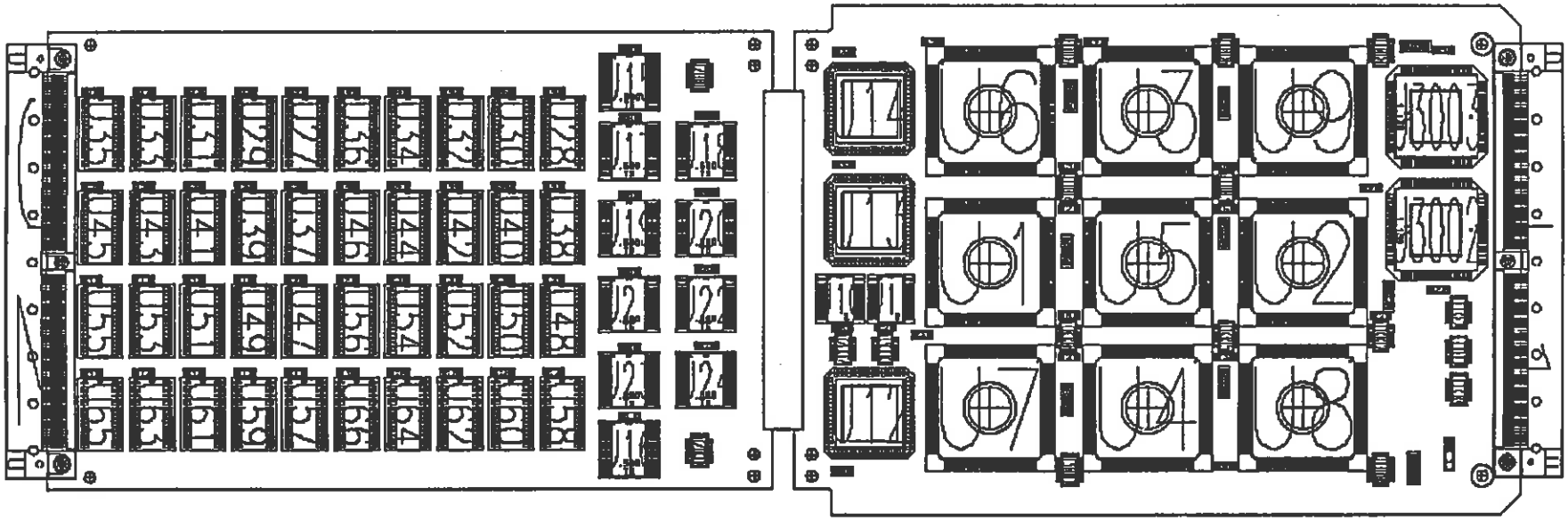
Solid State Recorder - Flight



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