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INTEGRATED ELECTRONICS MODULE (IEM)

UPLINK BOARD CRITICAL COMMAND DECODER

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CRITICAL COMMAND DECODER (CCD) REQUIREMENTS

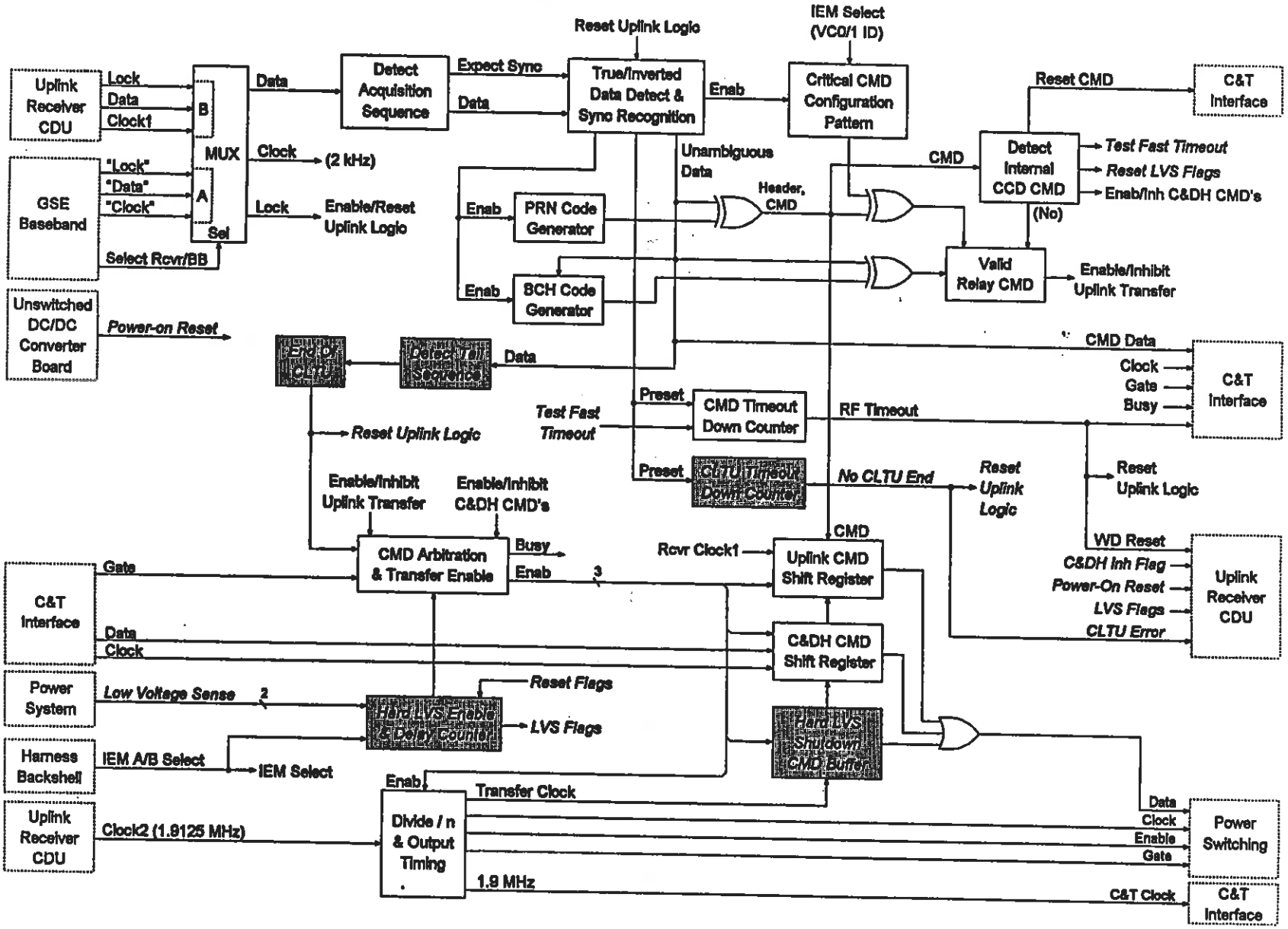
- Receive CCSDS compatible commands from Uplink Receiver Command Detector Unit (CDU) or from GSE (baseband)
- Forward all commands to C&DH Processor via Command & Telemetry Interface board
- Send all uplinked, locally addressed relay commands to Power Switching Unit

⇒ *Decode and implement several internal CCD (non-relay) commands*

- Send C&DH Processor-generated relay commands to Power Switching Unit; notify Processor when relay command has been sent

⇒ *Upon receipt of a "Hard" low bus voltage indication from the Power Subsystem, issue a stored set of relay commands for orderly load reduction; send flag(s) to C&DH Processor*

- Perform "No commands received" timeout (RF Watchdog Timer); reset CCD and CDU digital circuits and send flag to C&DH Processor
- Provide stable clock to Command & Telemetry Interface board

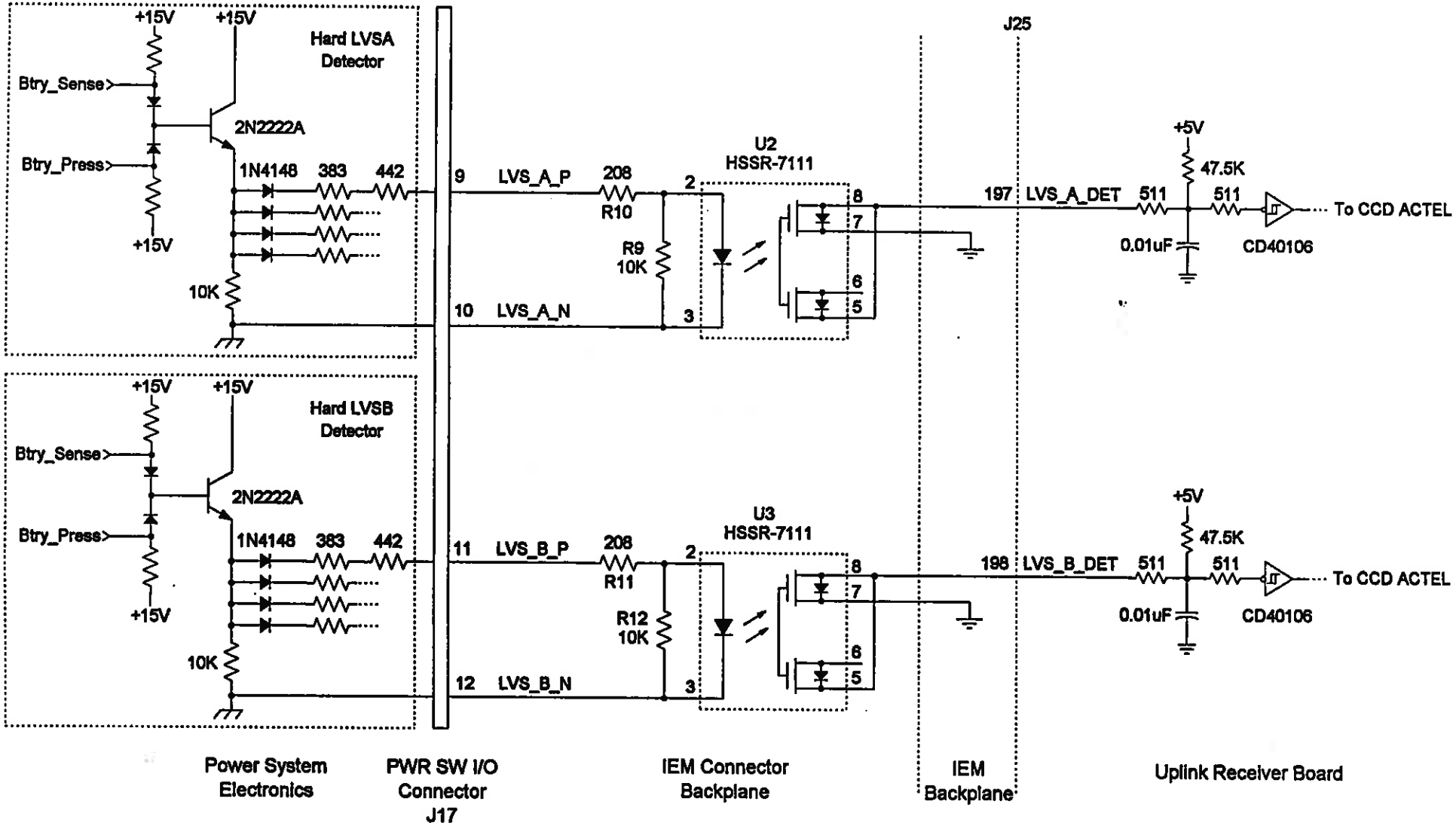


TIMED Critical Command Decoder (CCD)

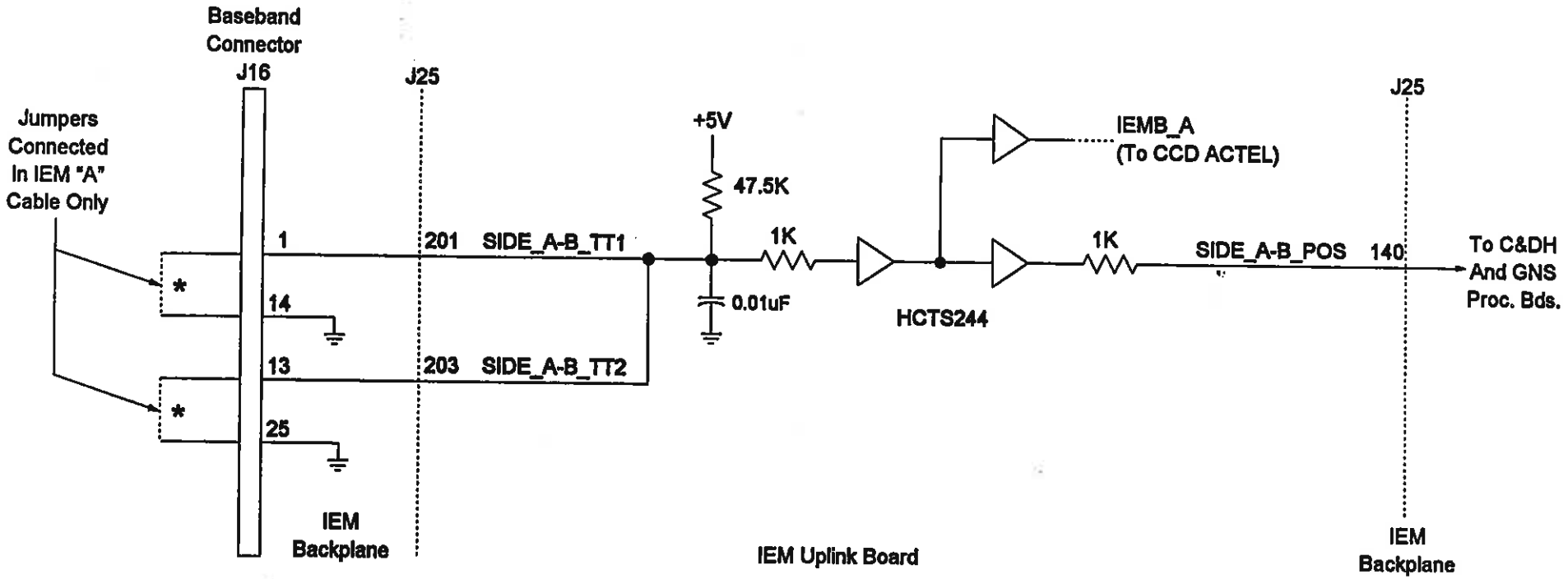
SFO-3

Critical Command Decoder (CCD) Testing & Status

- ACTEL Simulations
  - Uplink relay commands (VC0,1), C&DH-generated relay commands, Hard-LVS-generated relay commands, combinations of all three
  - Internal CCD commands: enable/inhibit C&DH relay commands, reset C&DH processor, fast test of command timeout, reset Hard-LVS flags
  - Non-CCD commands, errors in commands, errors in tail sequence
- Breadboard Tests
  - Wirewrap breadboard includes CCD circuitry, digital front end of Power Switching relay circuitry, "Relay on/off" indicators, other indicators
  - Successful tests with Receiver/CDU breadboard included: uplink relay commands, including errors; internal CCD commands; Hard-LVS detection, command generation
  - Successful tests with IEM Testbed & C&DH simulator included: Baseband uplink commands (all relays, true and inverted data), including errors; internal CCD commands; C&DH-generated commands; Hard-LVS detection, command generation
- Status
  - Suggestions from Uplink EDR being implemented



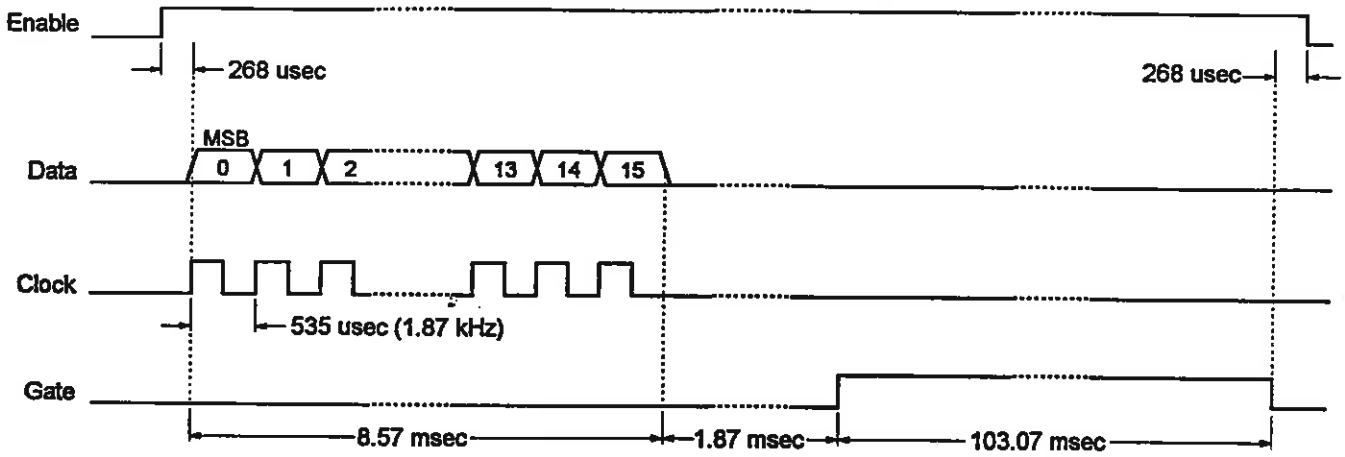
Critical Command Decoder / Power System LVS Interface

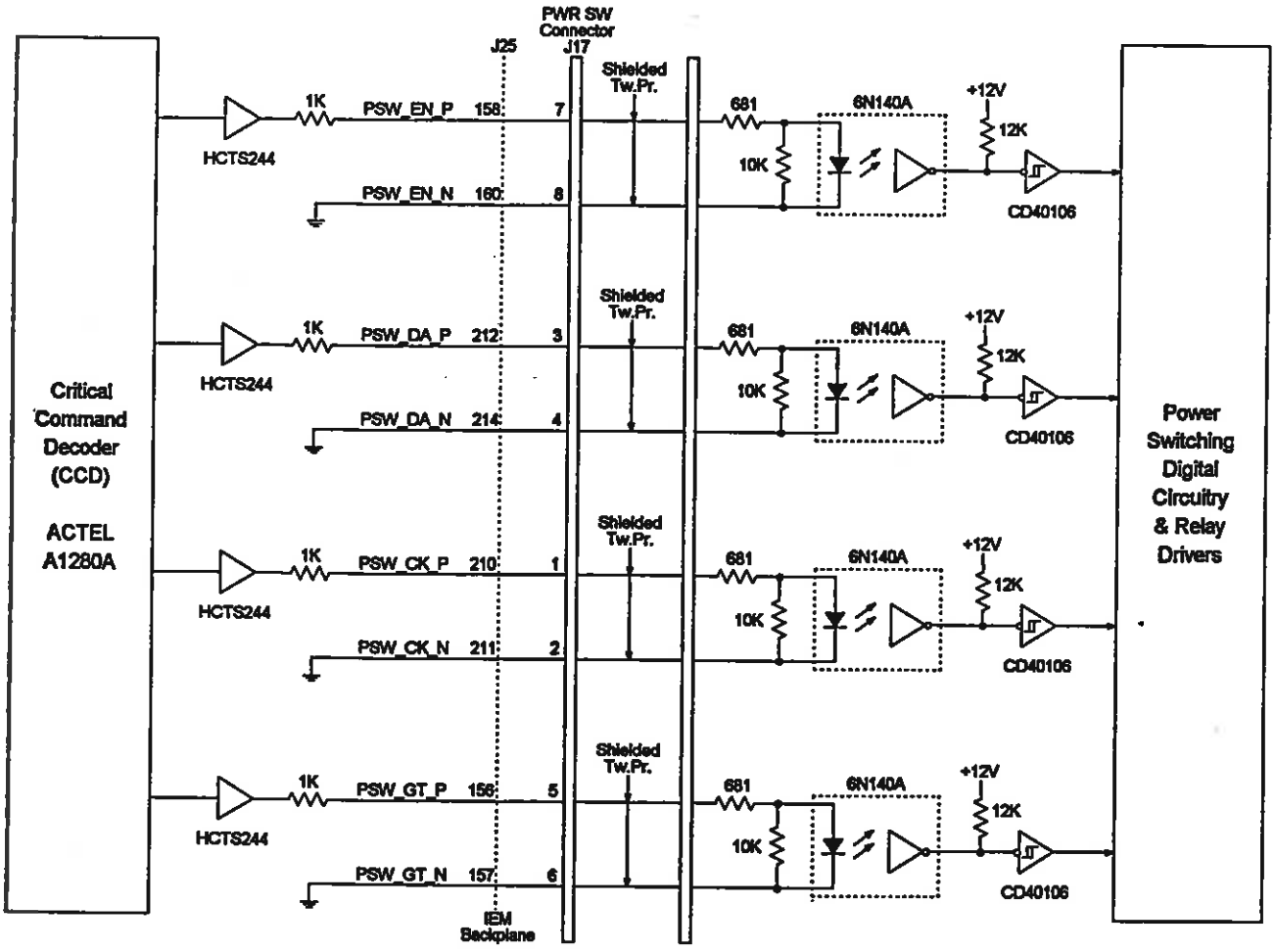


* (Jumpers in Harness Backshell)

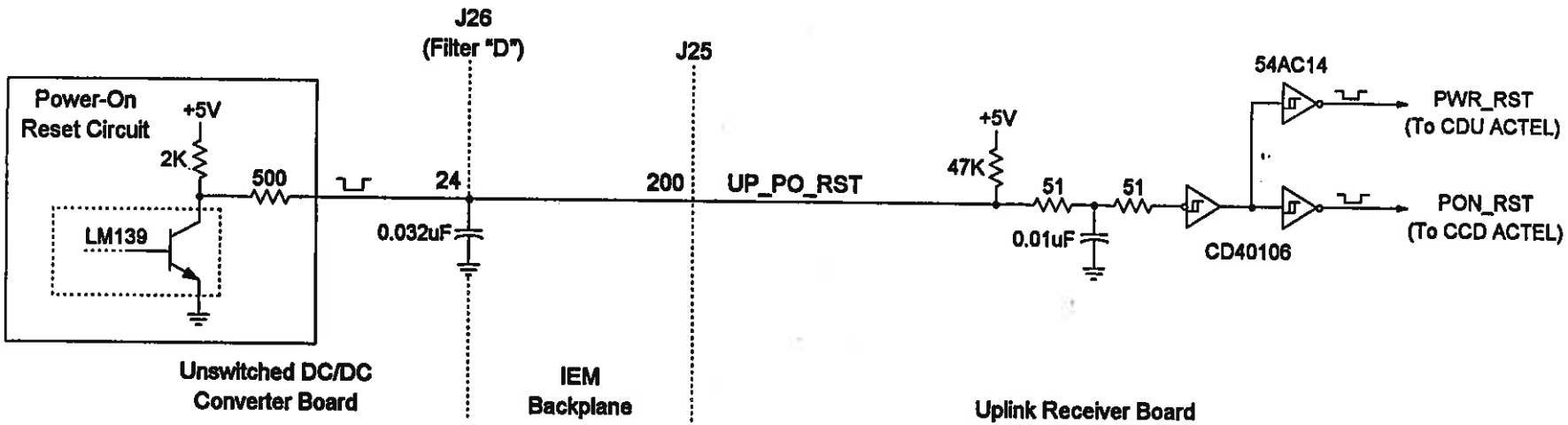
IEM A/B Jumper / Critical Command Decoder (CCD) / IEM Processors Interface

SFO-10

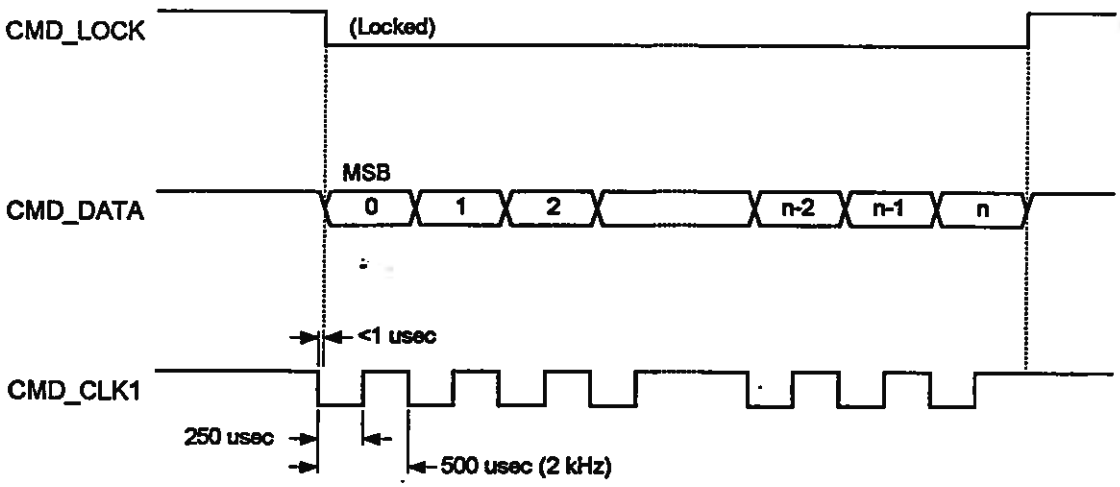


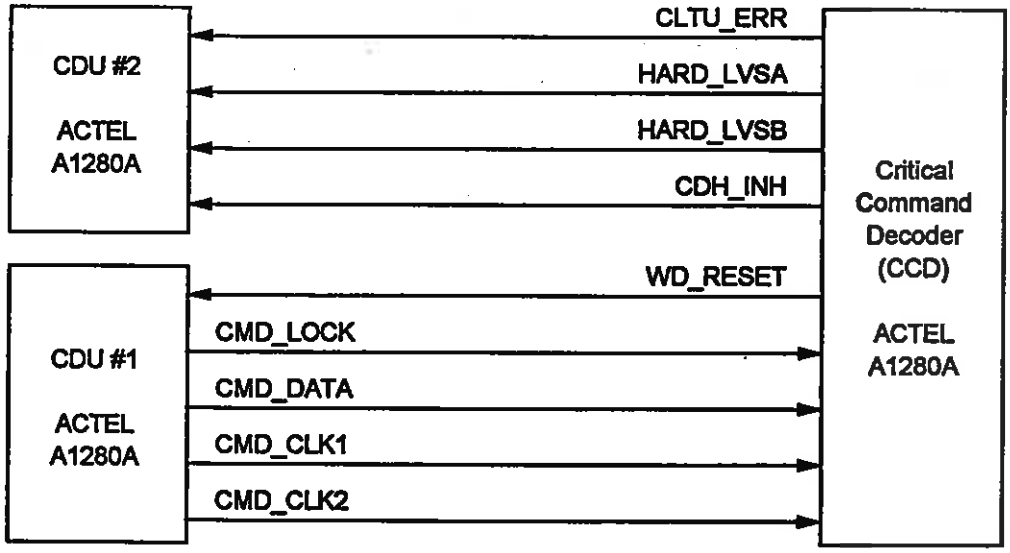


Critical Command Decoder (CCD) / Power Switching Unit Interface SFO-7



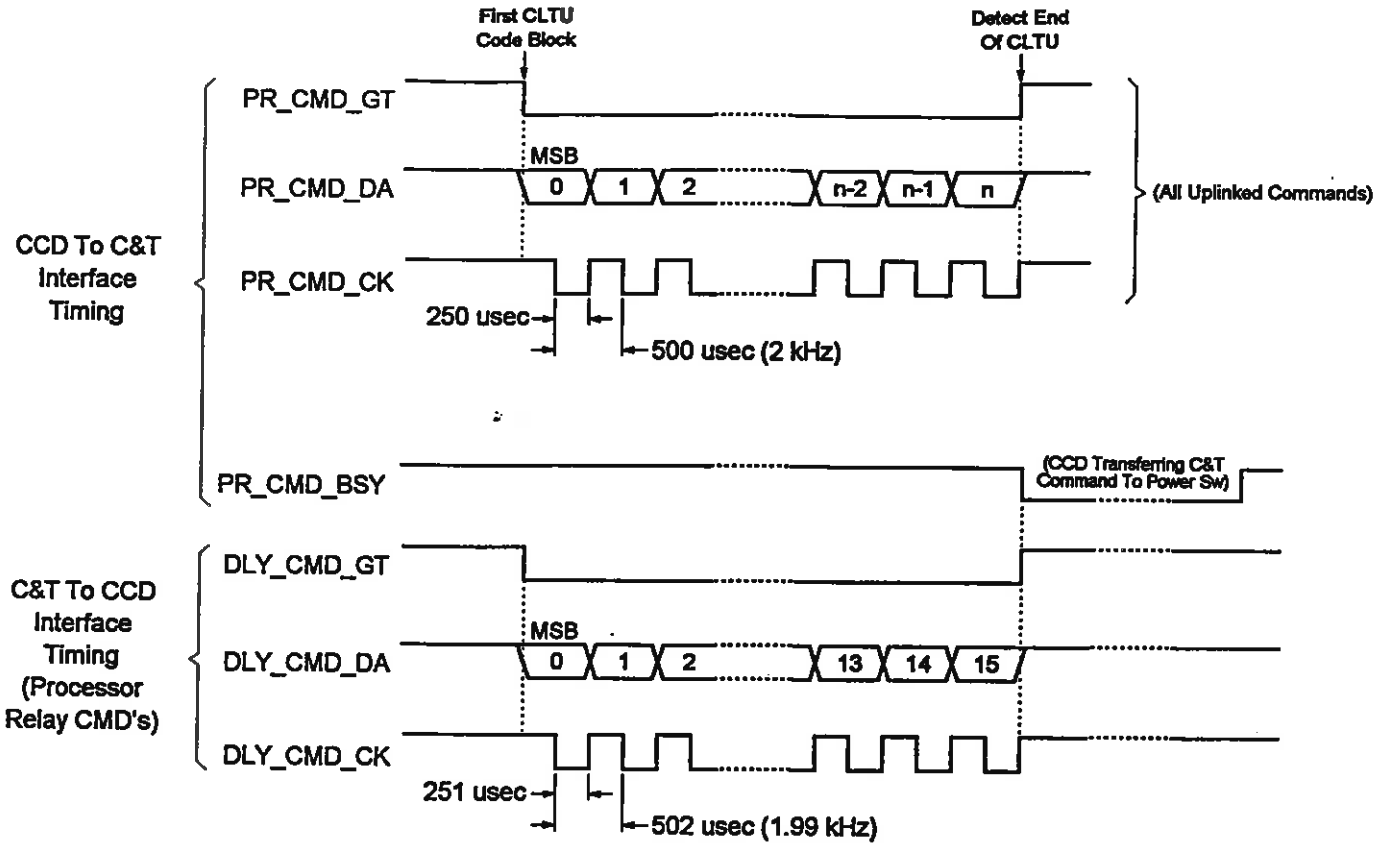
Critical Command Decoder (CCD) / DC/DC Converter Interface

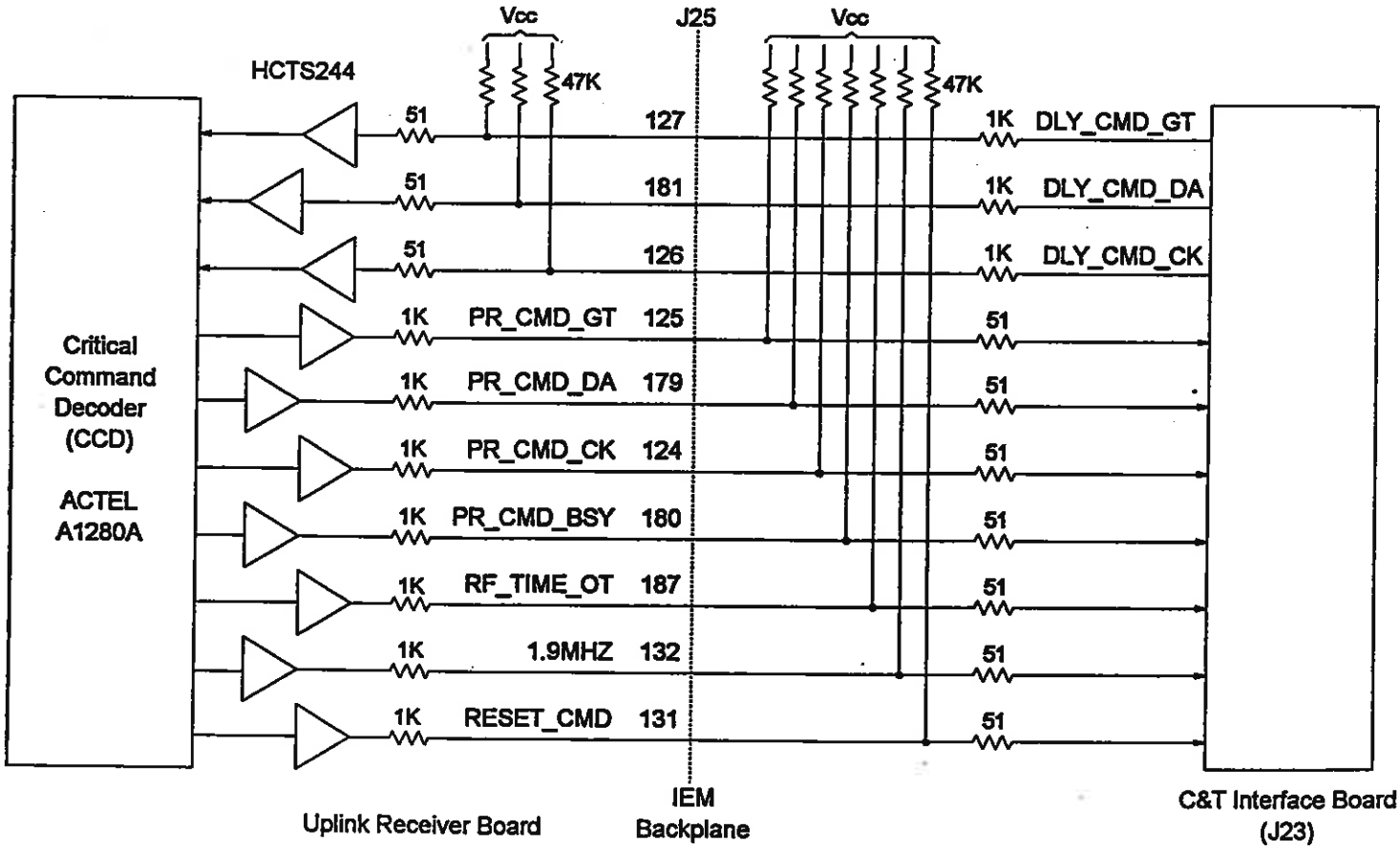




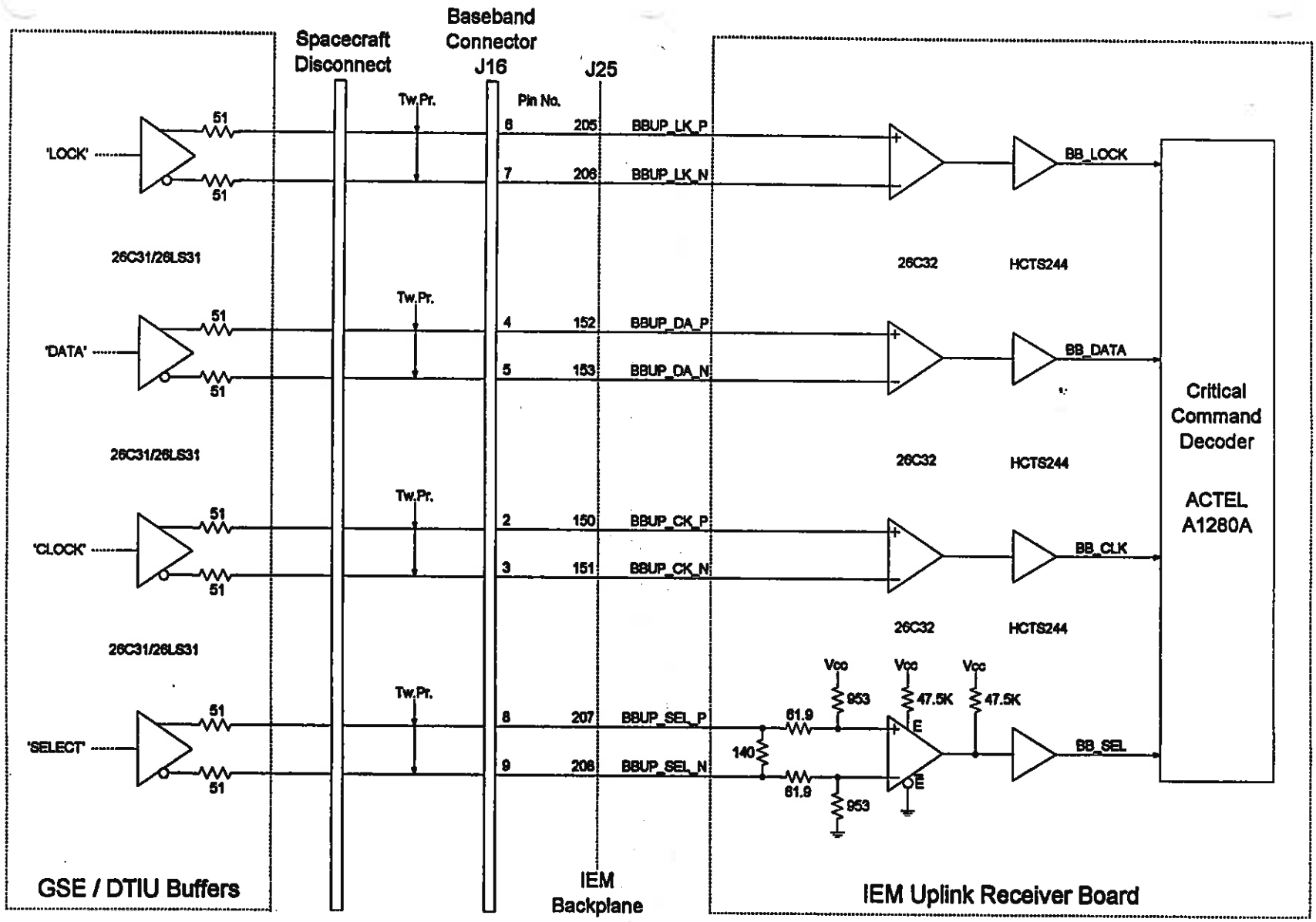
Uplink Receiver Board
(J25)

Critical Command Decoder (CCD) / Command Detector Unit (CDU) Interface





Critical Command Decoder (CCD) / Command & Telemetry (C&T) Interface SFO-6



Critical Command Decoder (CCD) / Baseband Test Interface

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COMMAND & TELEMETRY INTERFACE BOARD

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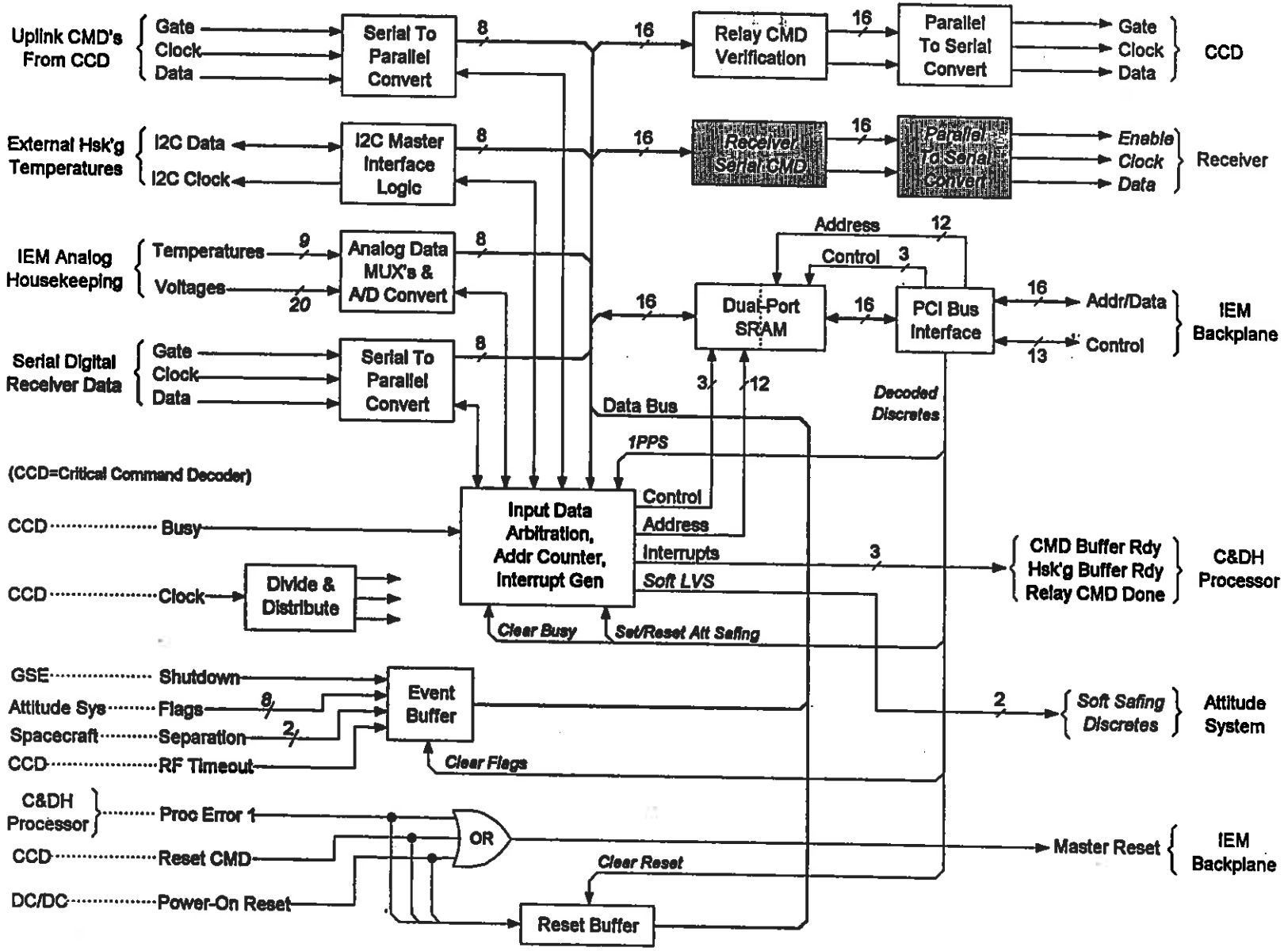
COMMAND & TELEMETRY INTERFACE REQUIREMENTS

- Route all uplink commands from Critical Command Decoder to C&DH Processor
- Route all C&DH Processor-generated relay commands to Critical Command Decoder

⇒ *Route Receiver command from C&DH Processor to IEM Uplink board*

- Collect remote temperature telemetry data via I2C serial bus
- Collect and digitize IEM temperature and voltage telemetry data
- Collect serial digital telemetry data from IEM Uplink board
- Collect and report "Events" to C&DH Processor
- Detect error conditions and generate reset for IEM functions

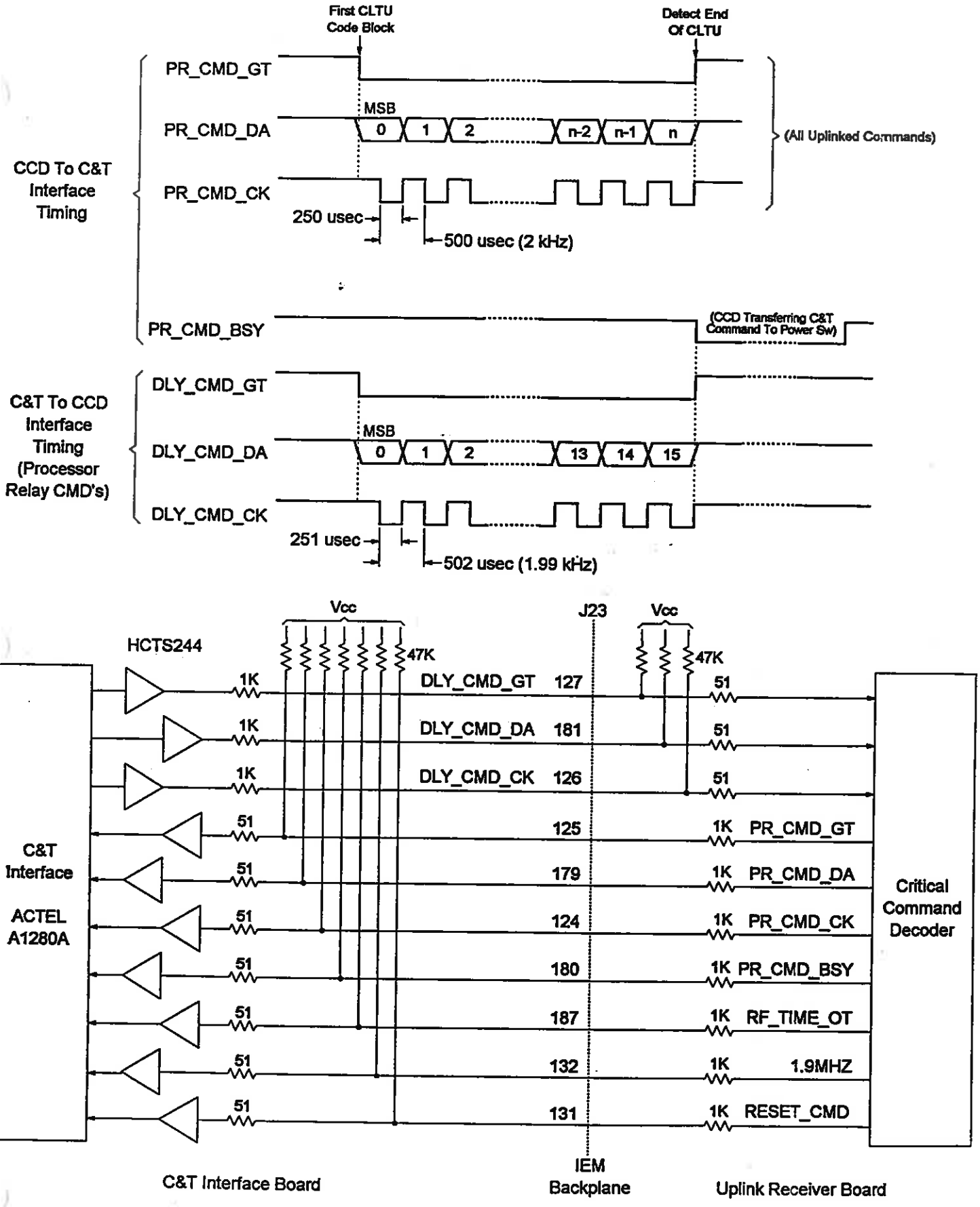


IEM Command & Telemetry Interface Board

SFO-14

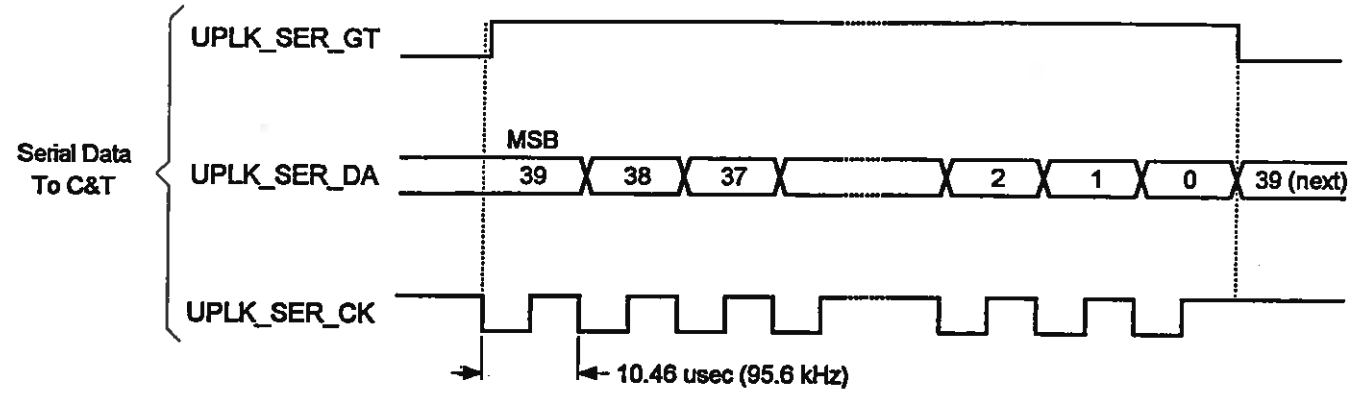
Command & Telemetry (C&T) Interface Board Testing & Status

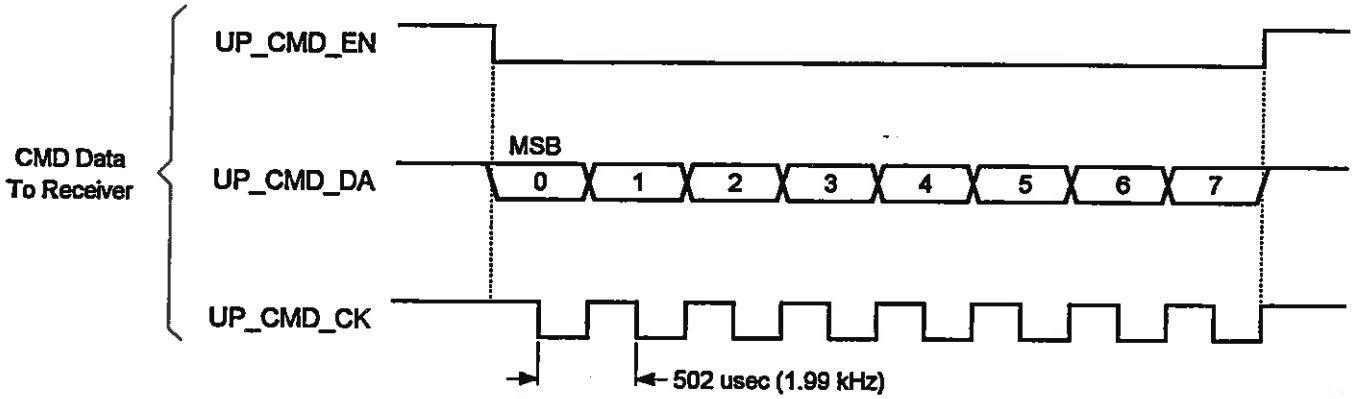
- ACTEL Design and Simulations Completed
  - Receipt of uplinked commands from Critical Command Decoder (CCD)
  - I2C interface for remote temperature telemetry gathering
  - Multiplexing and A/D conversion of IEM temperature and voltage telemetry
  - Receipt of Receiver serial digital telemetry
  - Receipt, verification, and transfer of relay commands from C&DH Processor to CCD
  - Receipt and transfer of Receiver serial command from C&DH Processor to Uplink board
- ACTEL Design in Progress
  - Memory address generation, control for above data transfers
  - Event buffer and reset circuitry details
  - Arbitration logic and interrupt generation
- Breadboard Status
  - Board populated with all except C&T and PCI ACTEL's, memories
  - Analog multiplexers, temperature current-to-voltage conversion, filter and gain stages for IEM temperature and voltage telemetry tested
- PC Board Layout Status
  - Preliminary layout done; minor revisions required

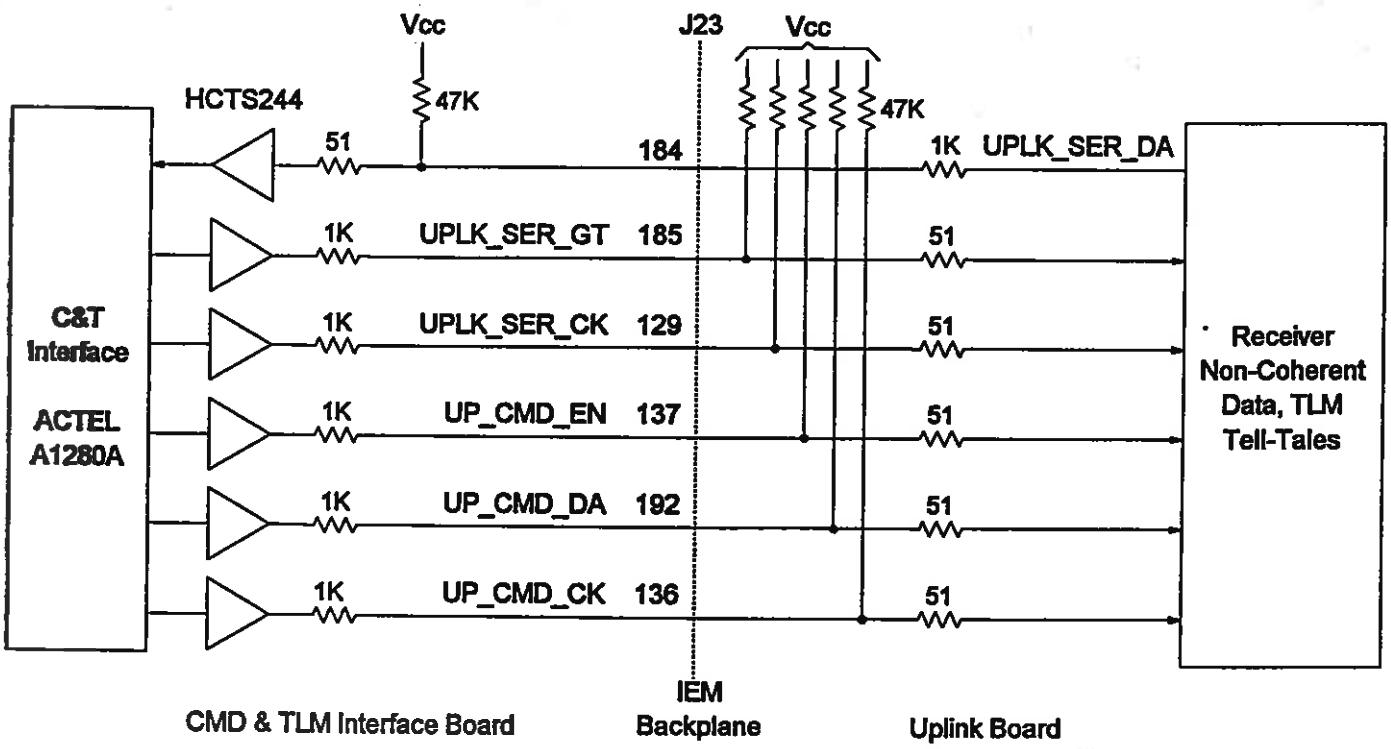


Command & Telemetry (C&T) / Critical Command Decoder Interface

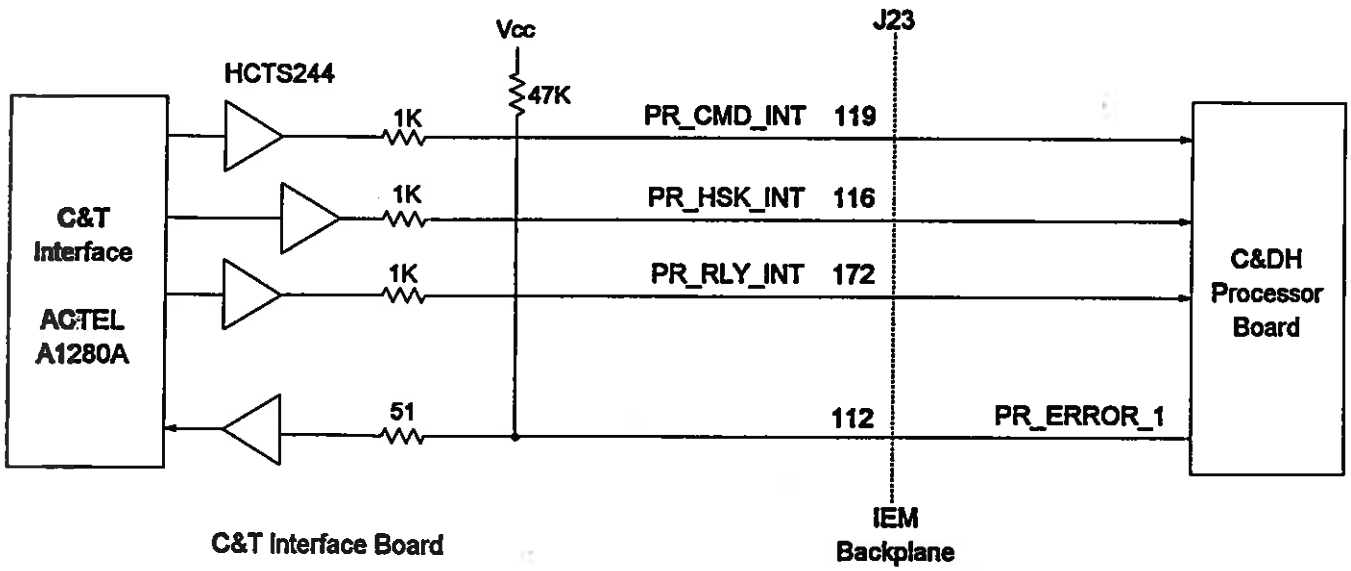
SFO-16



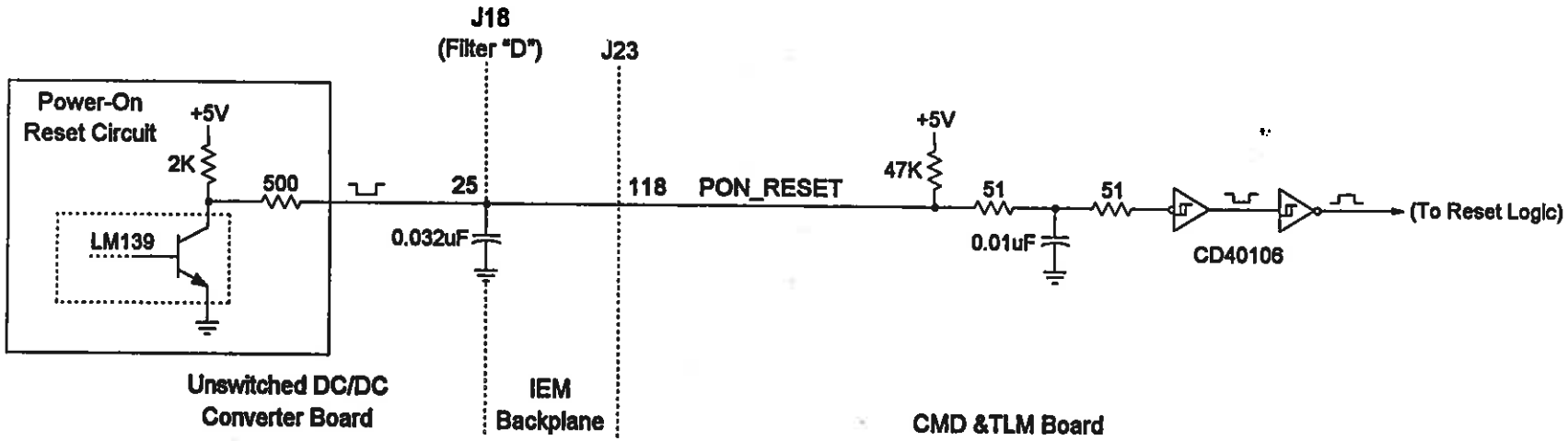




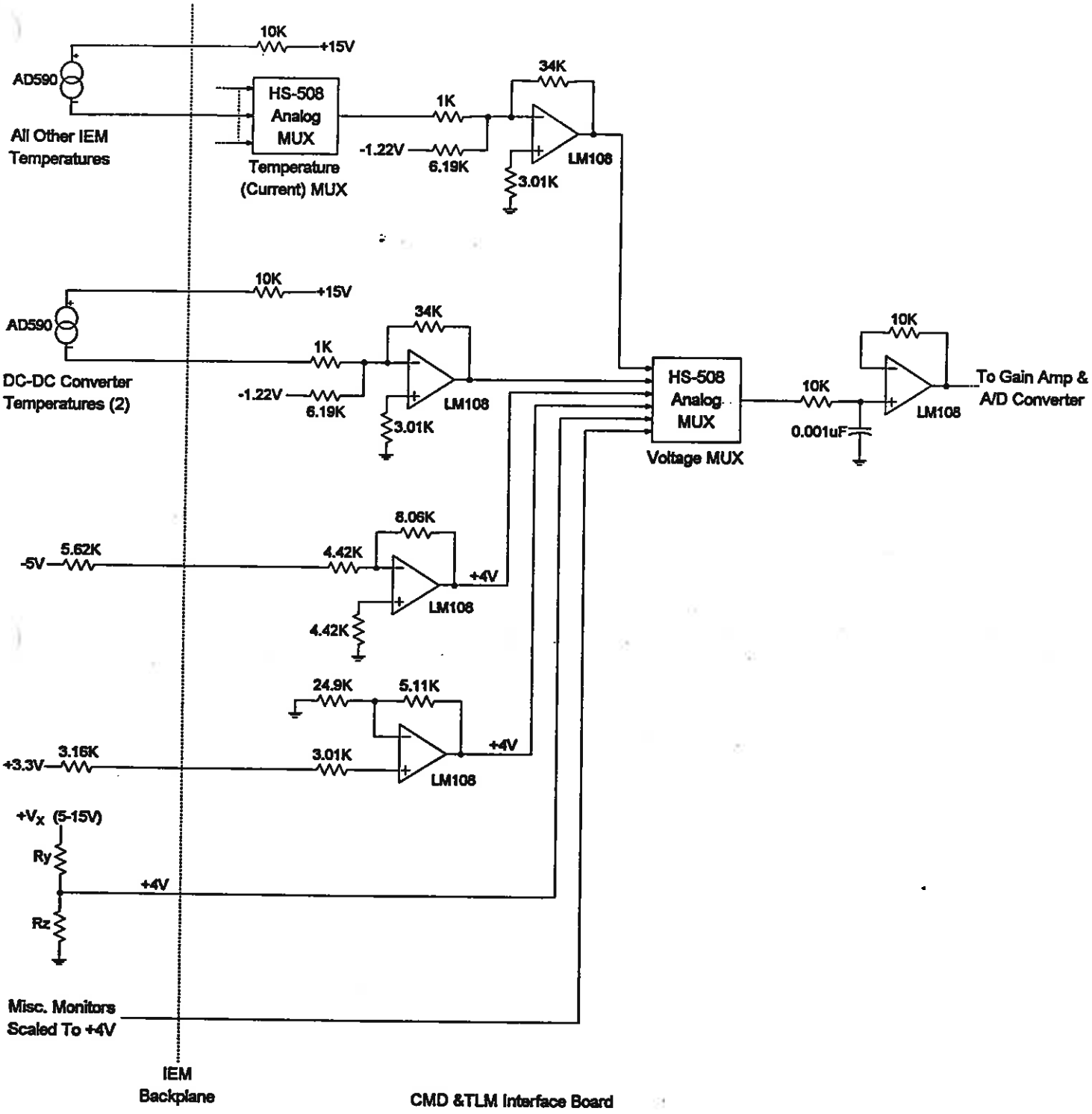
Command & Telemetry (C&T) / Uplink Receiver Interface SFO-17



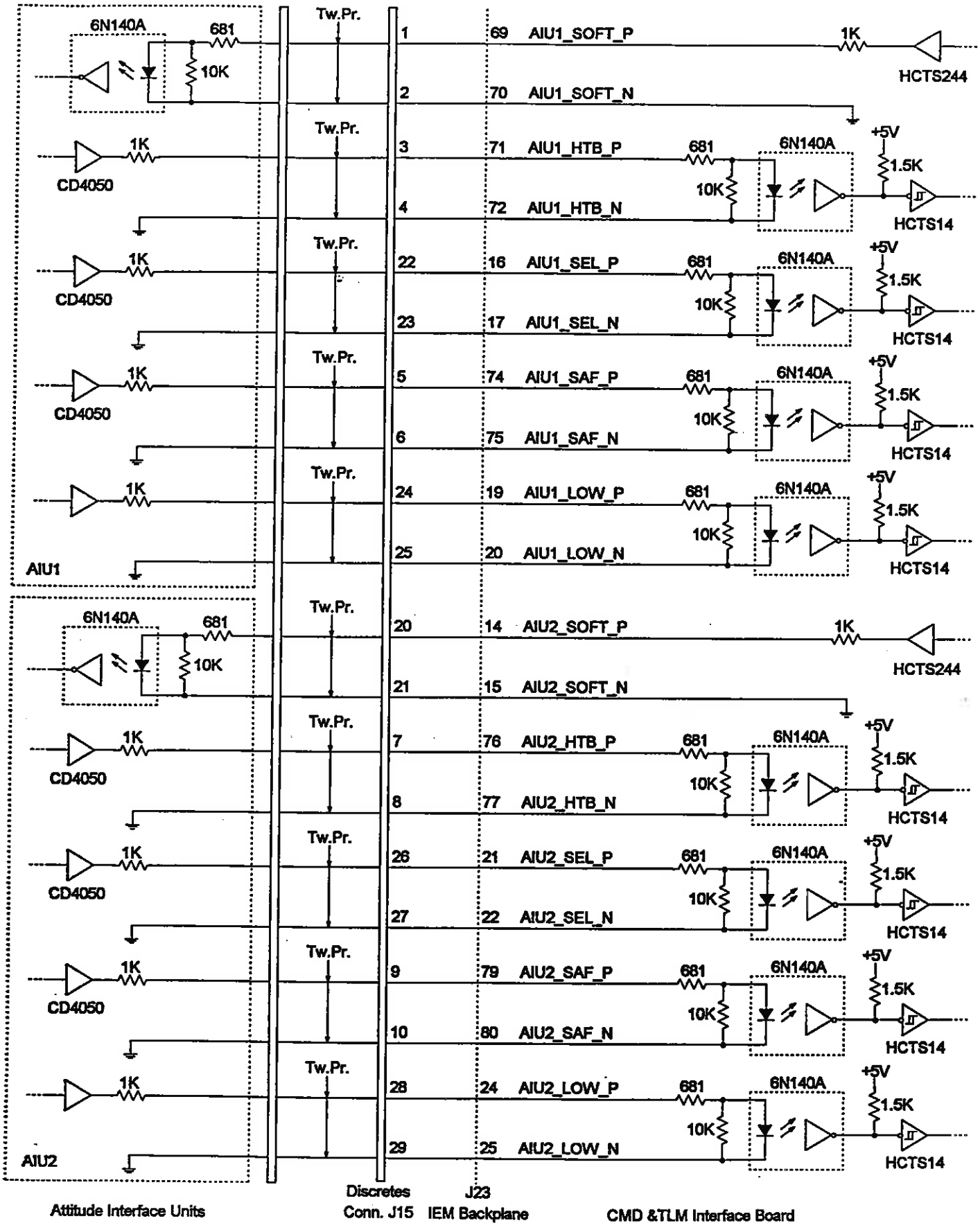
Command & Telemetry (C&T) / C&DH Processor Discretes Interface



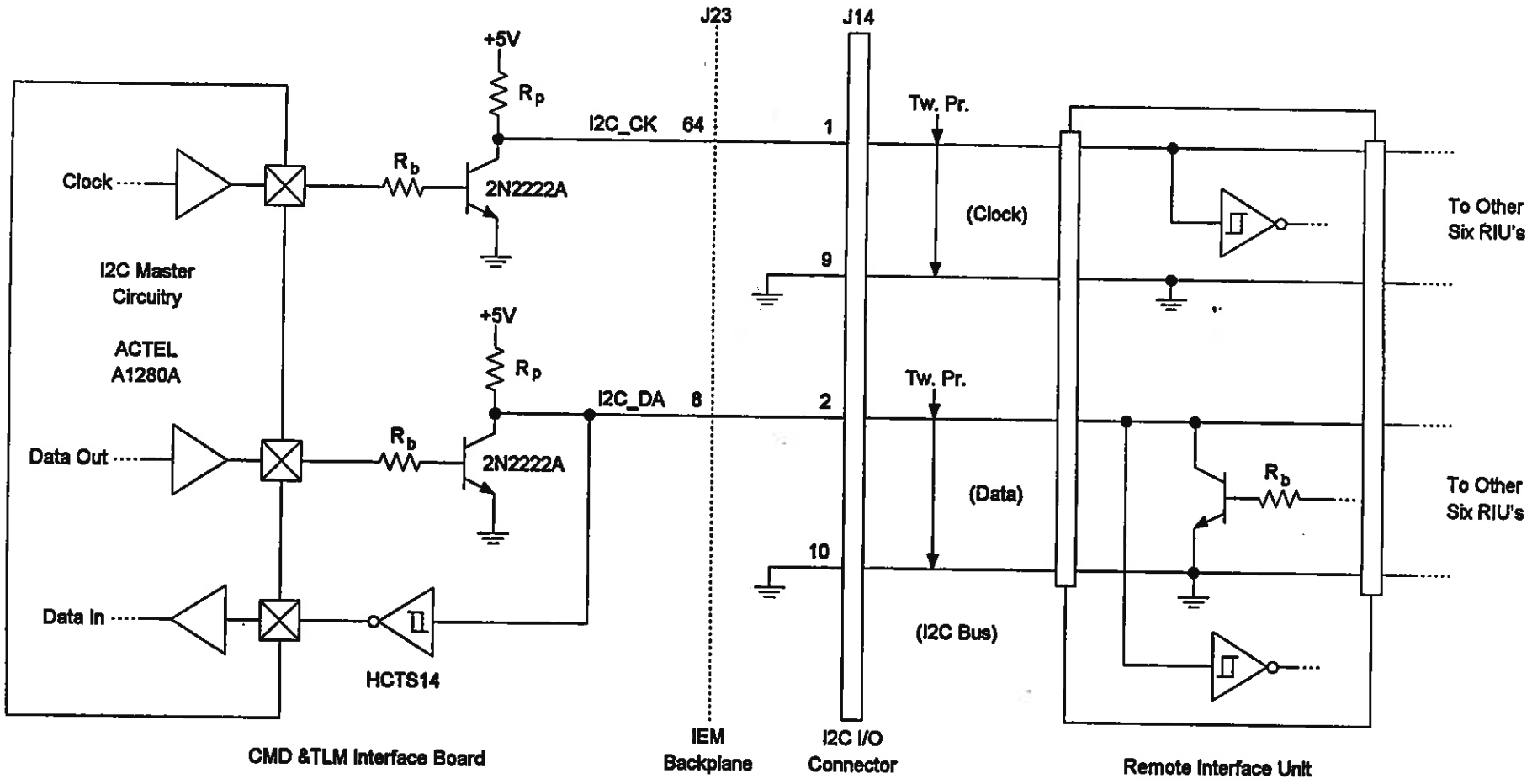
Command & Telemetry (C&T) / DC/DC Converter Interface



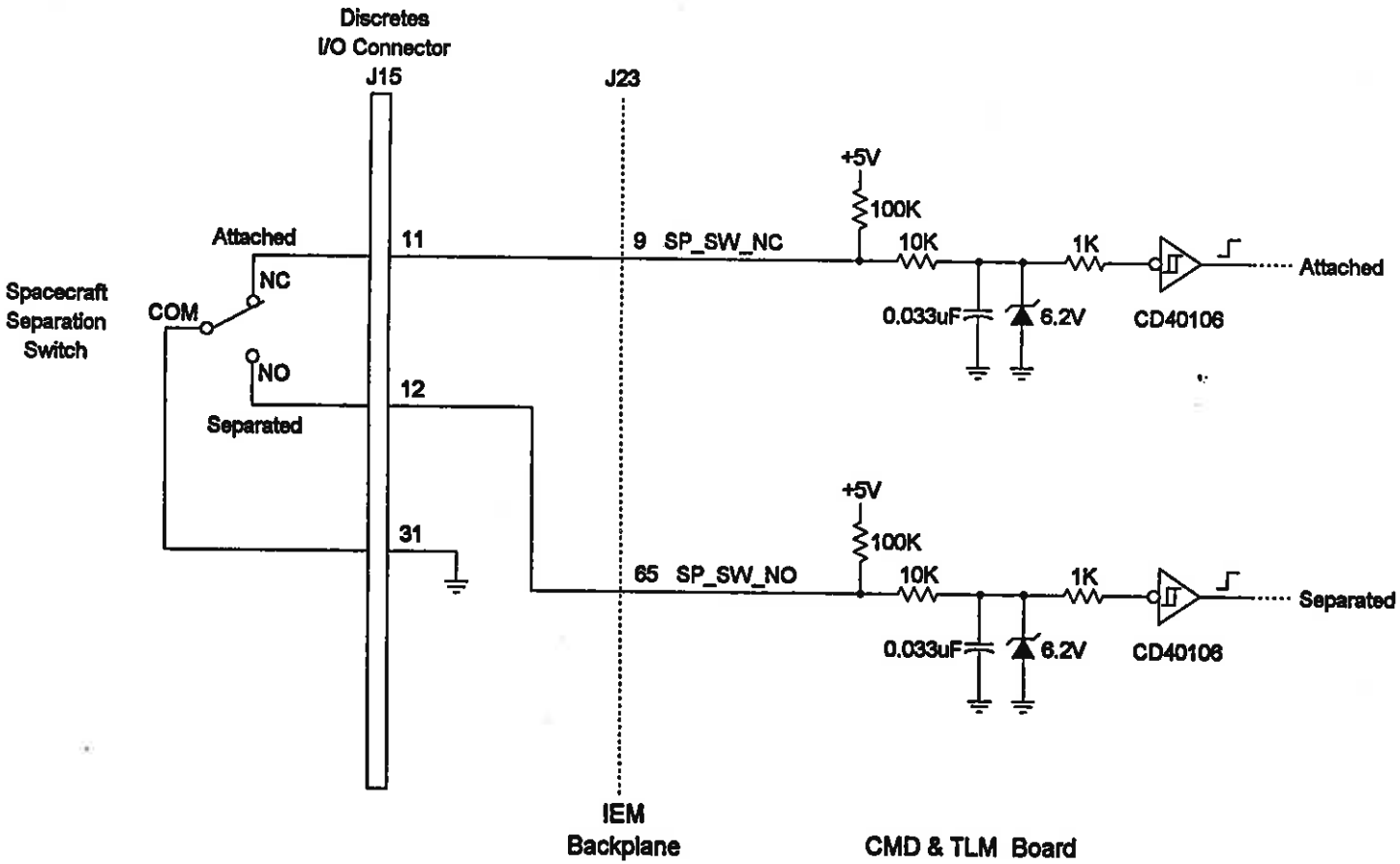
Command & Telemetry (C&T) / IEM Housekeeping Telemetry Interface



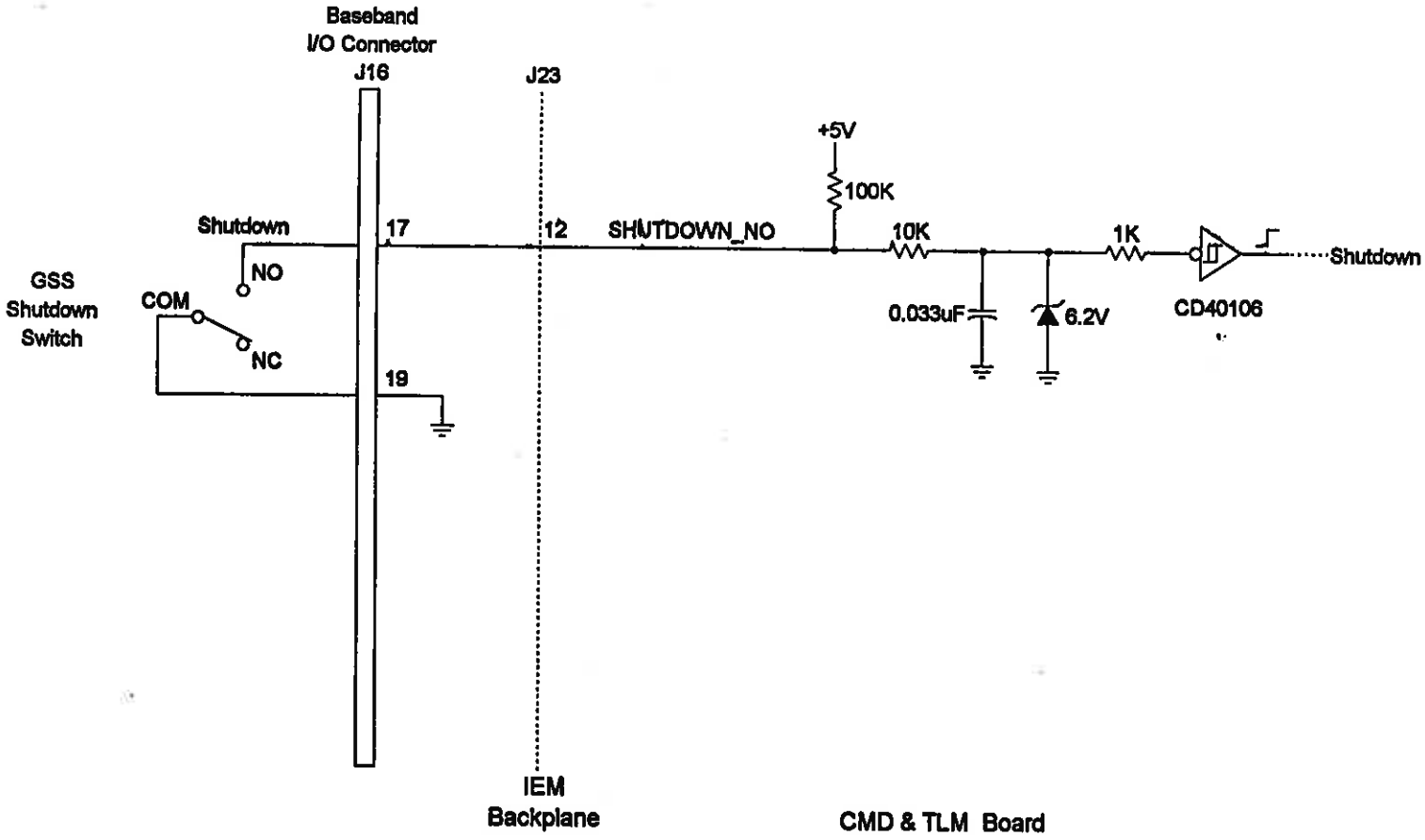
Command &Telemetry (C&T) /Attitude Interface Unit (AIU) Interface



Command & Telemetry (C&T) / Remote Telemetry I2C Interface



Command & Telemetry (C&T) / Spacecraft Separation Interface



Command & Telemetry (C&T) / Ground Support System (GSS) Interface

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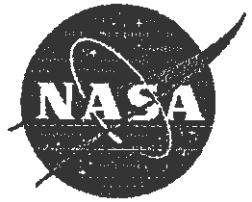

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Downlink TLM Framer

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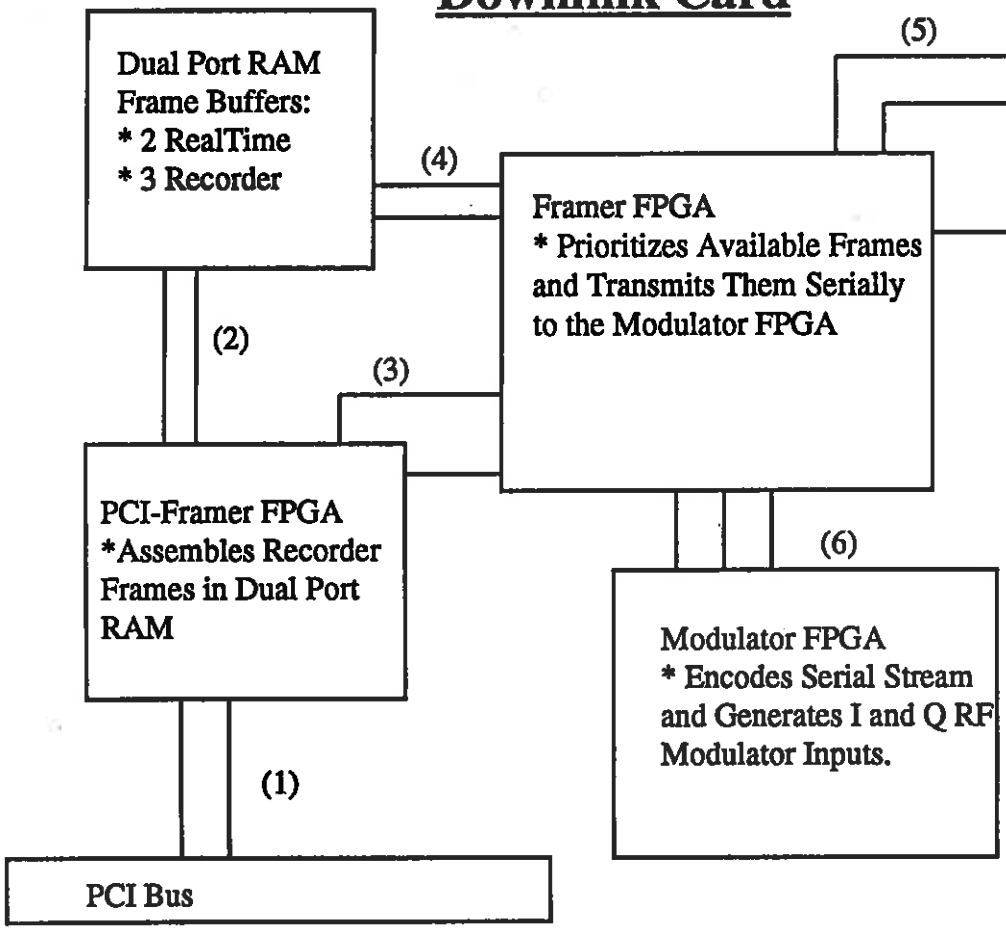
TLM Framer Function

- Assembly of Transfer Frames Consists of Two Actel FPGAs--Framer FPGA, and a PCI-Framer FPGA.
- Framer FPGA transmits Realtime, Recorder and Null frames based on buffered data in the downlink dual port RAMs and sends serial data to the RF Modulator.
- PCI-Framer FPGA performs normal PCI transfer functions and it requests Recorder packets which are assembled into Recorder frames in the dual port RAM.
- Processor uses normal PCI transfer function to buffer Realtime frames in the downlink dual port RAM.

Downlink Card

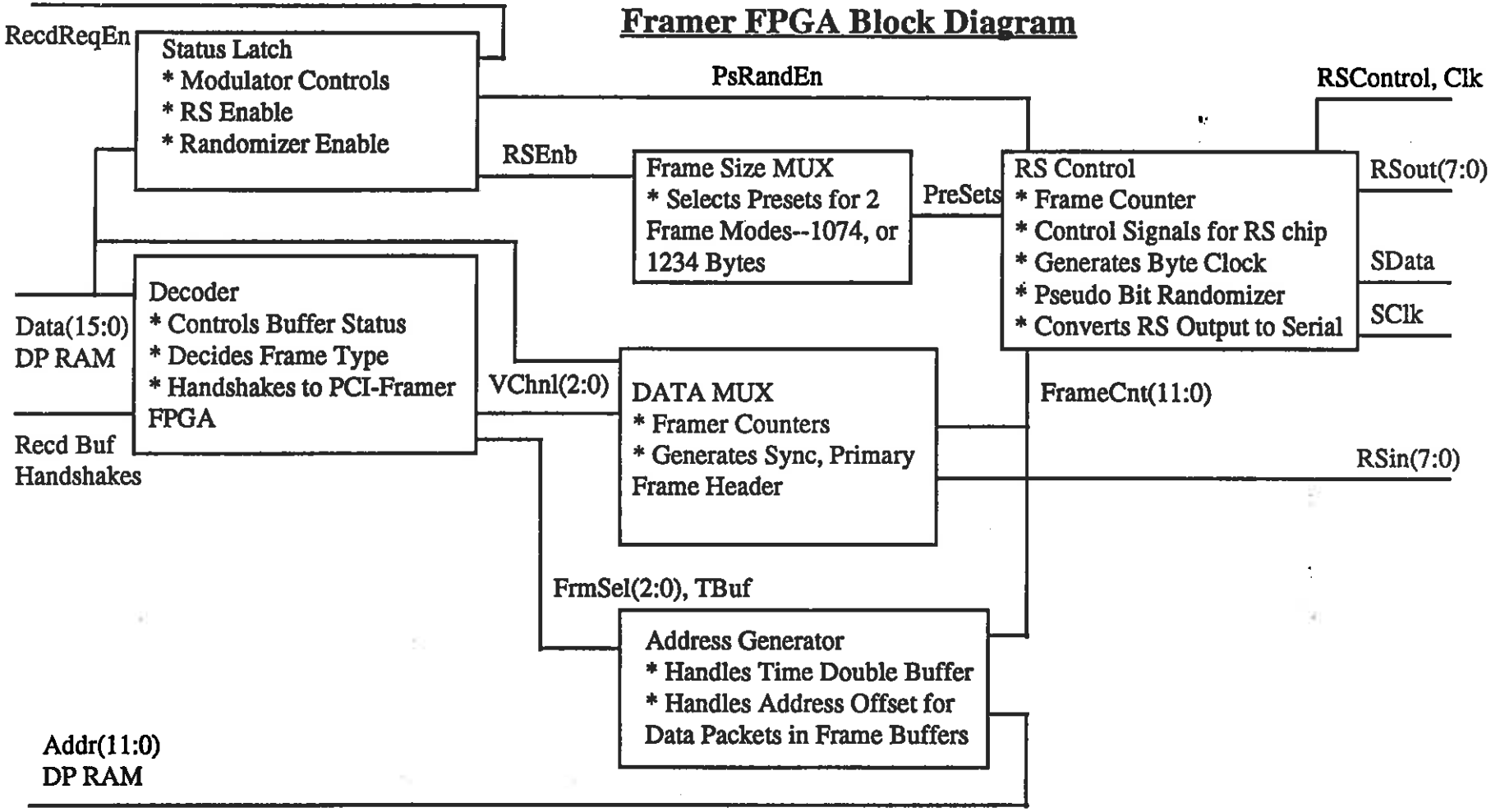


Interfaces:
(1) Data Passes Between PCI Bus and Dual Port RAM(2)
(3) Controls PCI Master requests for Recorder Data
(4) Reads Status and Assembled Frame Data from Dual Port RAM
(5) Passes Data Bytes and Control to the Reed Solomon Encoder
(6) Provides Modulator Controls and Serial Data Stream. Receives Bit Clock for Framer Timing.

Framer FPGA Functions:

- Assembles Realtime, Recorder, and Null frames from the data buffers in the downlink dual port RAM.
- Relays Modulator Control Inputs.
- Controls PCI-Framer Recorder frame buffer assembly.
- Sends normal or randomized serial data to the RF.
- Generates sync header and primary frame header.
- Counts Realtime, Recorder, and NULL frames.
- Realtime Frames via Processor/PCI Bus.
- Controls Reed Solomon encoding IC.

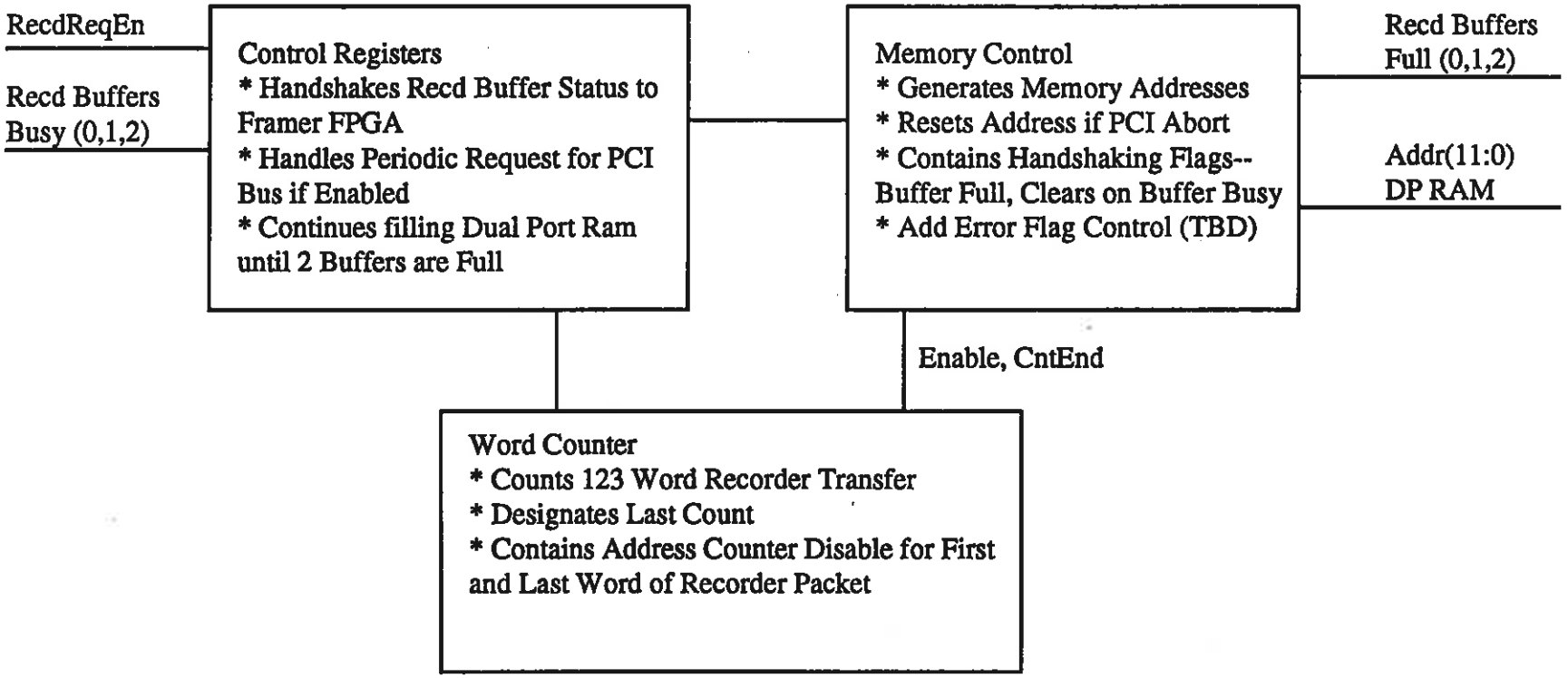
Framer FPGA Block Diagram

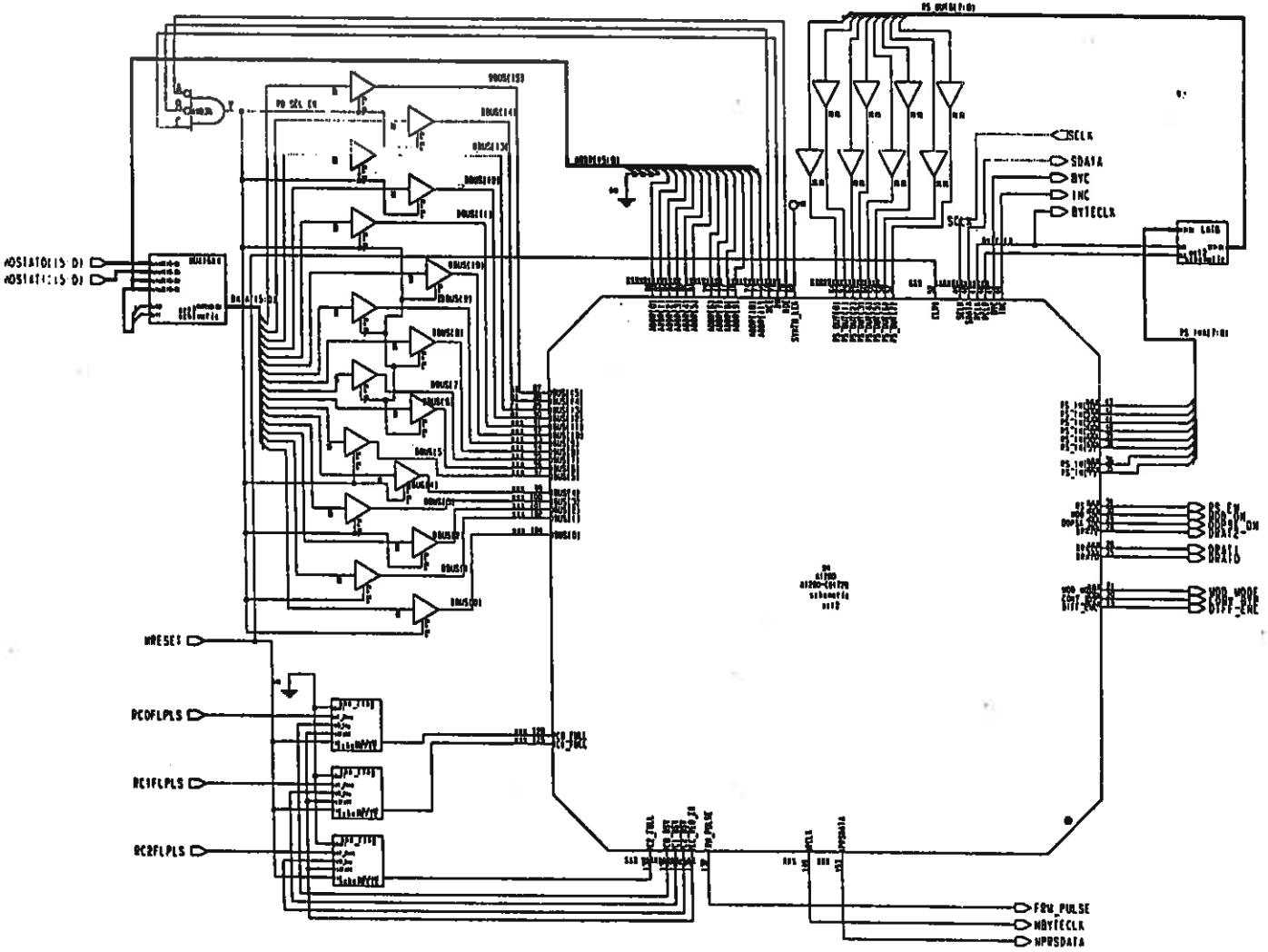


PCI-Framer FPGA Functions:

- Controls Transfer of Recorder Packets.
- Keeps track of Recorder Reed Solomon Errors.
- Uses Dual Port RAM for 3 frame buffers.
- Handshakes to Framer FPGA to get "Recorder_Request_Enable" signal. Sets buffer full flags and receives buffer clear flags (busy).

Modifed Master PCI Block to Handle Recorder Packet Transfers to Downlink Dual Port RAM Buffers--Only Modified Blocks Shown




SCLK
SDATA
BYC
INC
BYTECLR
nRESET
PCOFLPLS
PC1FLPLS
PC2FLPLS
FRM_PULSE
nBYTECLK
nPRSDATA