TIMED

Thermosphere . Ionosphere . Mesosphere . Energetics and Dynamics

IEM MOTHERBOARD
PCI BUS

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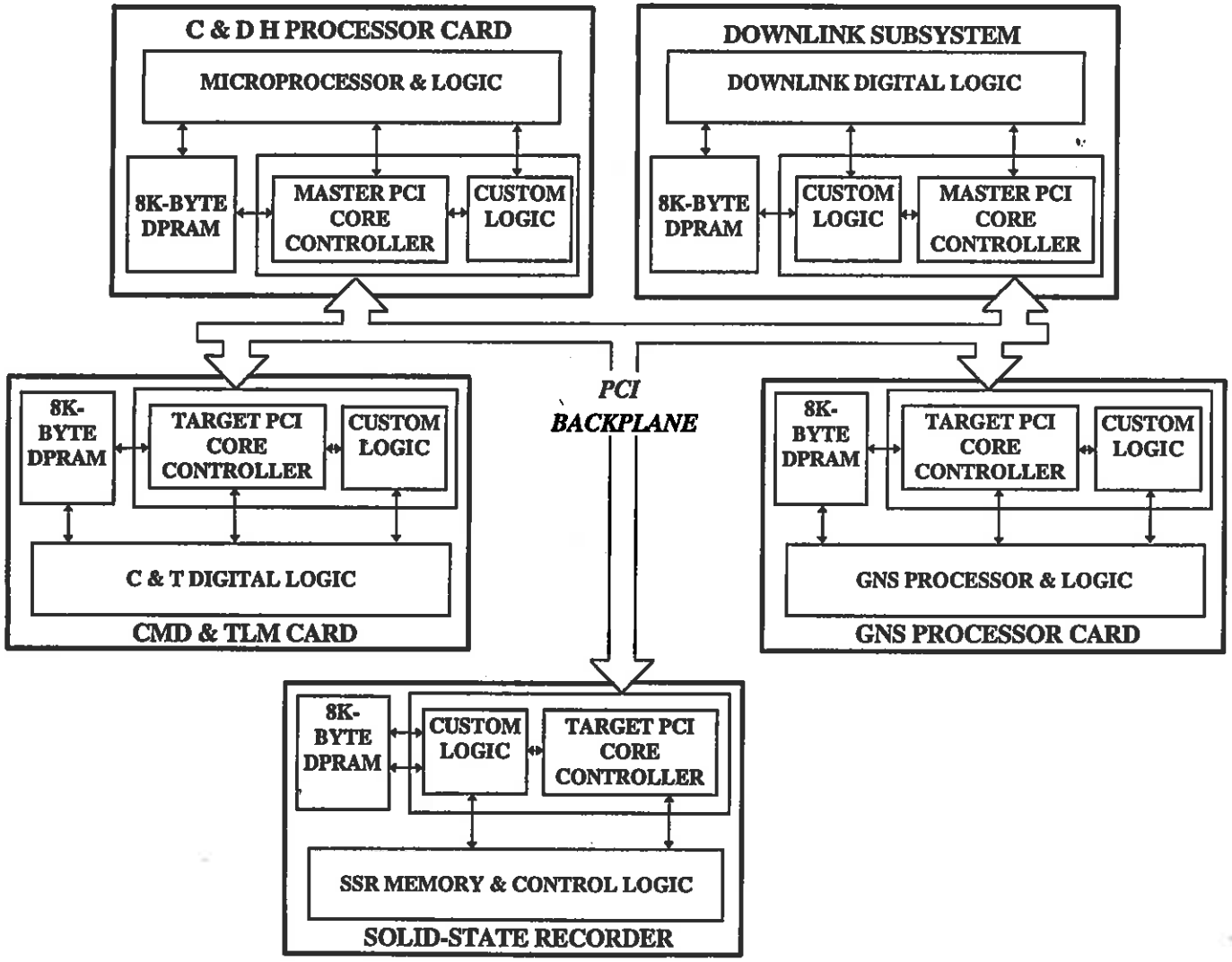
IEM BACKPLANE BUS REQUIREMENTS & SPECIFICATIONS

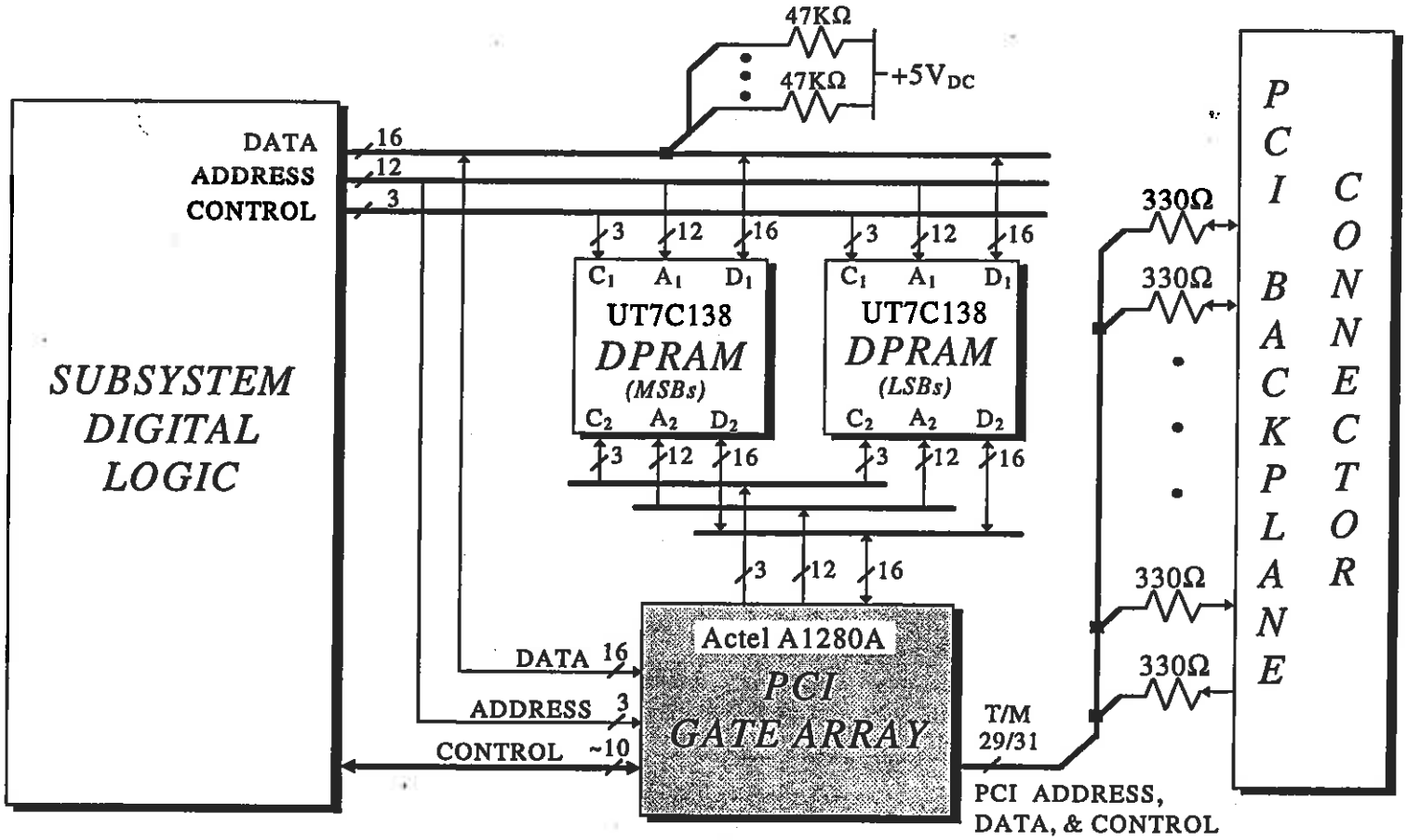
- *GENERAL REQUIREMENTS :*
  - **PROVIDE THE CAPABILITY TO RELIABLY TRANSFER DATA AND COMMAND INFORMATION ACROSS THE BACKPLANE BETWEEN SUBSYSTEMS AT A PEAK RATE OF $\geq$ 5 Mbytes/sec.**

- *GENERAL SPECIFICATIONS :*
  - **COMMERCIAL PERIPHERAL COMPONENT INTERCONNECT (PCI) SPECIFICATION (Rev. 2.1) USED AS A BASIS FOR COMMUNICATION PROTOCOL**
  - **16-BIT DATA BUS, CLOCKED AT 5 MHz, YIELDS A PEAK DATA TRANSFER RATE OF 10 Mbytes/sec.**
  - **ACTEL, FPGA IMPLEMENTATION (P/N: A1280A) - Single Device**
  - **POWER DISSIPATION (calculation):**
    - » **MASTER: 215mW @ nominal 20% duty cycle**
    - » **TARGET: 144mW @ nominal 10% duty cycle**

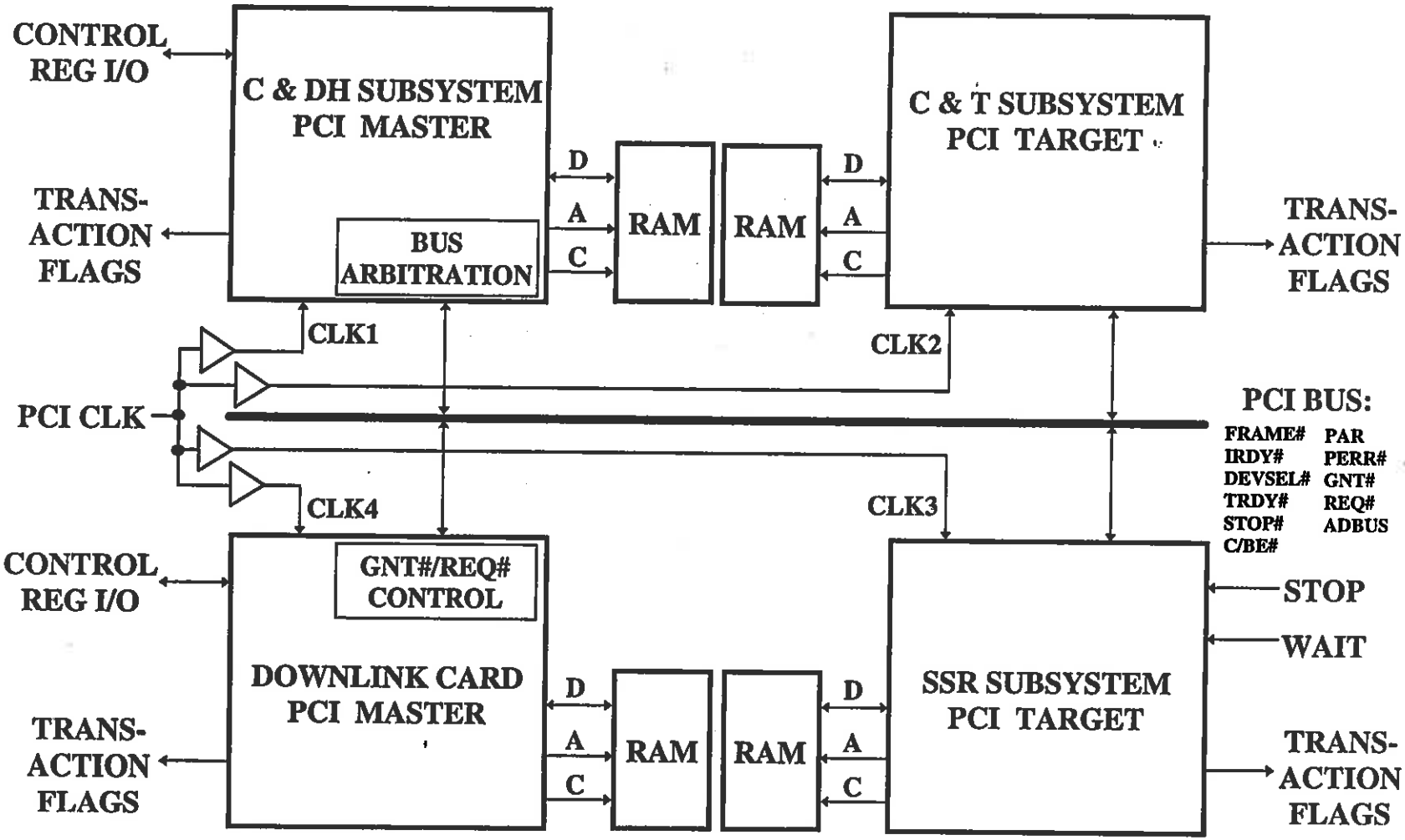
IEM BACKPLANE PCI SYSTEM



IEM SUBSYSTEM
PCI CHIP IMPLEMENTATION



PCI SYSTEM SIMULATION SETUP

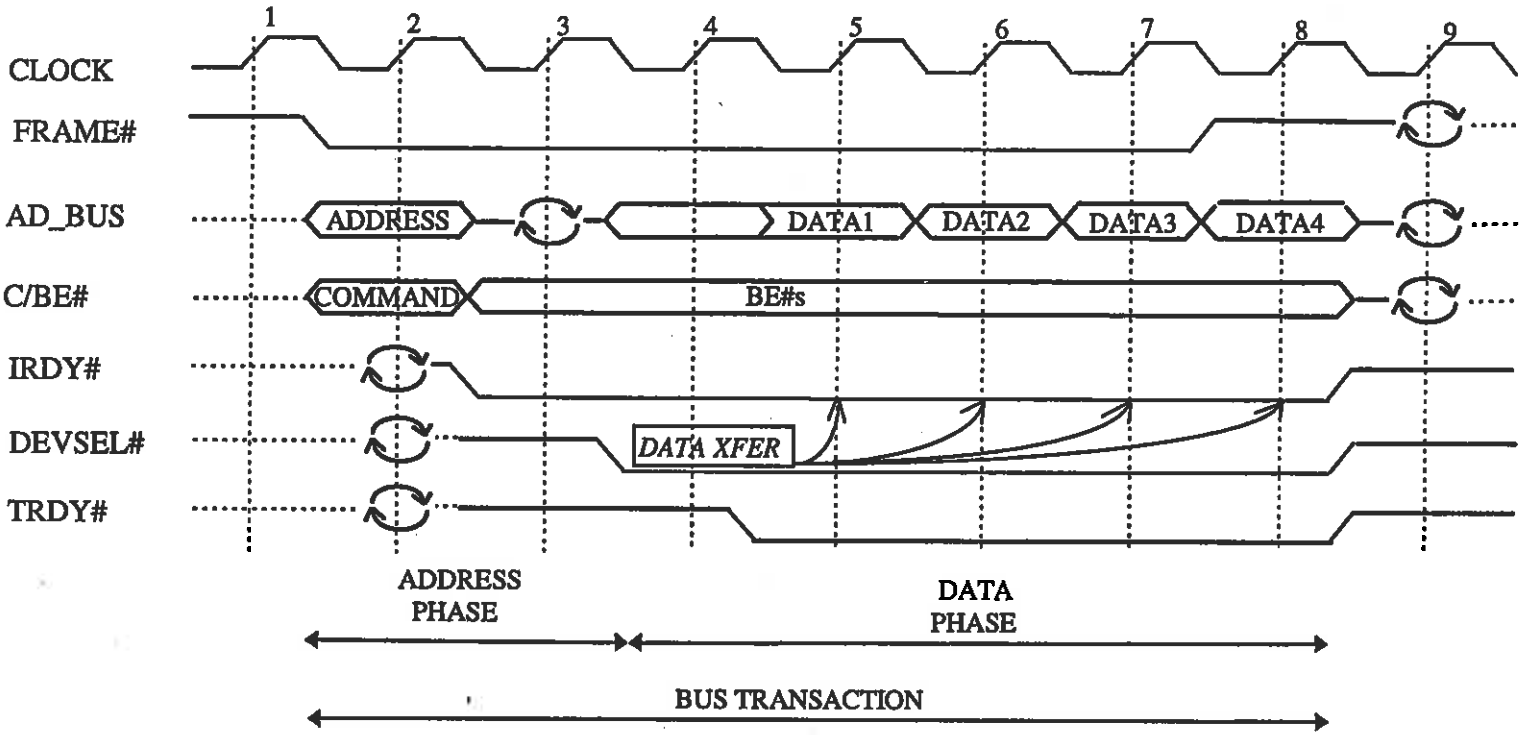


SIMULATION CONDITIONS & RESULTS

- *TYPES OF SIMULATIONS PERFORMED:*
  - DEVICE FUNCTIONAL SIMULATION - Idealized Timing
  - DEVICE OPERATIONAL SIMULATION - Fully Routed With Back-Annotated Internal Delay Values
  - IEM PCI SYSTEM OPERATIONAL SIMULATION
- *OPERATIONAL SIMULATION CONDITIONS*
  - MILITARY TEMPERATURE RANGE: -55° C to +125° C
  - MIL VOLTAGE TOLERANCE: +/- 10%
- *SIMULATION RESULTS - PERFORMANCE TESTING*
  - PROVEN OPERATION AT 5MHz CLOCK, WITH MAX AT 7MHz
  - CLOCK SKEW BETWEEN MASTER AND TARGET TOLERATED TO 9 nsec (< 2 nsec max. expected)
  - BACKPLANE SIGNAL DELAYS BETWEEN MASTER & TARGET TOLERATED TO 80 nsec (< 60 nsec max. expected)

PCI SUPPLEMENTAL INFORMATION (1 of 2)

TIMING FOR TYPICAL READ OPERATION



PCI SUPPLEMENTAL INFORMATION (2 of 2)

TIMING FOR TYPICAL WRITE OPERATION