TIMED

POWER

By
George Dakermanji

The John Hopkins University
Applied Physics Laboratory
Building 23, Room 212
Laurel, MD 20723-6099
Tel: (301) 953-5079
FAX: (301) 953-6556
E-Mail: george.dakermanji@jhuapl.edu

TIMED

AGENDA

- Requirements
- S/C PDR action items
- Changes since PDR
- Power System Description
- Solar Array
- Battery
- Power System Electronics
- Power Switching and Distribution
- Breadboard Test Results
- Issues

TIMED

Power System Requirement Overview

- Spacecraft Mission Life: 2 Years
  Altitude: 625km
  Inclination: 74.1°
- Operating Bus Voltage Range 22 to 35V: Critical Loads
  24 to 35V: Non-critical Loads
- Spacecraft Orbital Average Load: 383.8W
  S/A sized for 426W (11% margin)
- Provide Low Battery State of Charge Protection
- Provide fusing and power switching to all redundant & non-critical subsystems
- Provide fusing for unswitched subsystems
- Provide status telemetry for switched subsystem
- Provide Power bus current telemetry for all subsystems

TIMED

Power Subsystem Flow-Down Requirements

- Single fault tolerant with no reduction in mission capabilities
- Solar Array must not affect the instruments' fields of view, the cold thermal radiation environment and minimize any unbalance in the drag torque during flight
- The power subsystem electronics must survive any IEM processor faults and be capable of maintaining the S/A and battery health in safe mode

TIMED

Spacecraft Power Summary Table

Instruments:		Orbit Avg Beta = 0	Margin	Orbit Avg+
	GUVI:	31.00 W	12.1%	34.74 W
	SABER:	69.80 W	5.3%	73.47 W
	SEE:	27.00 W	8.8%	29.37 W
	TIDI:	23.00 W	15.8%	26.63 W
Spacecraft Subsystems:				
	Power:	31.5 W	16.0%	36.8 W
	Attitude:	106.3 W	7.0%	113.64 W
	IEM1:	42.09 W	16.0%	48.83 W
	IEM2:	7.46 W	10.0%	8.20 W
	Thermal:	40.00 W	20.0%	48.00 W
	Harness:	5.67 W	11.3%	6.31 W
	TOTALS:	383.8 W	11.0%	426.00 W

Margin Assignment Guideline:	
Build to Print:	5%
Small Modification:	
or breadboard test result	10%
Substantial Modification:	15%
Estimate:	20%

TIMED

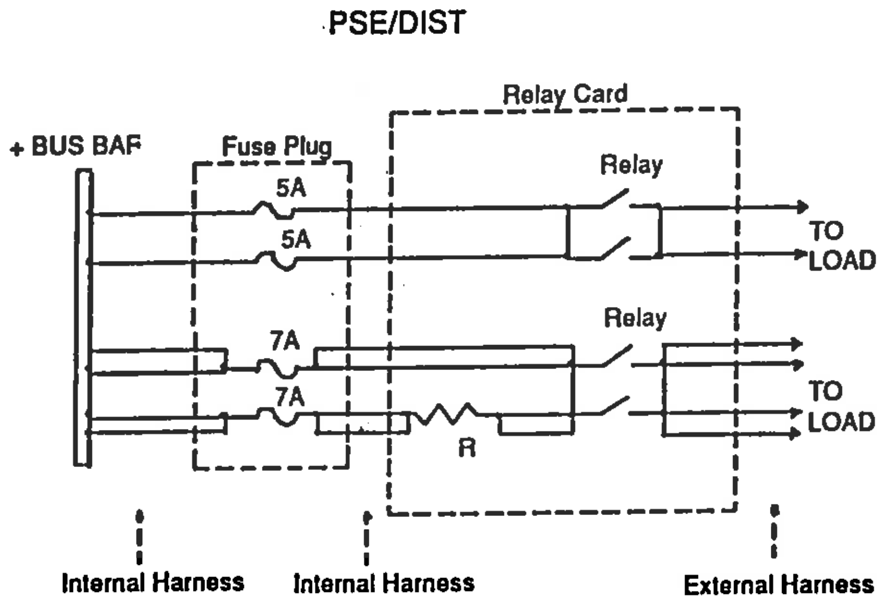
S/C PDR Action Item 14

The philosophy behind the redundant fusing plan seemed unclear and difficult to justify. Why not incorporate the "NASA standard" redundant fuse topology in all cases (two equal fuses in parallel, one with small series resistor so as to force a 1/3-2/3 current split)? Doesn't the use of a diode instead of a resistor result in a larger voltage drop should the primary fuse open?

Response: The rationale behind using two fuses in parallel for small loads and a combination of a fuse in parallel with a fuse/resistor series network for large loads is to minimize the required hardware. The TIMED power distribution uses a minimum of two 20 AWG wires in a D-connectors with 20 AWG pins for each load. A 5 A fused line will have a 5 A relay contacts carrying the current with a combined closed contacts minimum current carrying capability of over 15 A. A ≤5 A fuse can safely be blown using 20 AWG wiring (max. derated current for single wire is 6.5 A) during fault conditions. For fuses ≥7A (the 7 A fuse is the next higher size from 5 A fuse), a resistor is used to steer most of the current through one of the parallel fuses. This will reduce the max. peak current required to blow the fuses so that two parallel 20 AWG wires, a relay with 10 A contact rating and corresponding relay card PC track size can safely survive the fault condition. The use of a small appropriately sized resistor, as planned for TIMED, will provide a smaller voltage drop if the primary fuse is blown compared to using a diode.

Dr. John Day, Head of the Space Power Applications Branch at NASA GSFC, indicated that there is no "NASA Standard" redundant fuse topology. In fact, GSFC uses the two parallel fused with no resistor in series with either fuse topology in their spacecraft designs. The planned approach on TIMED provides the necessary protection without the addition of about thirty power resistors.

PDR Action Item 14 (cont.)



Redundant Fusing Diagram

TIMED

PDR Action Item

PDR chart GD-6 shows latching relays in series with the battery that can be opened only by umbilical command. Although unlikely, if these relays should open during launch the mission would be lost. a) Are these relays really needed? b) If needed, is there any reliability advantage to replacing them with normally closed, *non*-latching relays?

Response: There is no direct or derived requirement for the subject relays. Therefore, the need for the relays is subjective. The relays provide a means for quickly disconnecting the battery from the spacecraft bus in the event of a severe failure on the spacecraft power busses. They provide a more effective means of protecting the flight battery from such a failure than an arming plug, particularly when the spacecraft is in a thermal vacuum chamber or on the launch pad.

It is recognized, as stated in the action item, that if (both) relays were to open on launch, the mission would be lost. Therefore, great care has been exercised in their implementation. Two parallel relays are used for increased immunity to a catastrophic failure. The relays are configured such that only a ground command through the umbilical can disconnect the battery. (Zener diodes in series with the relay coils result in the requirement for a 56 volt power source to operate the coils to the "OFF" position' they cannot be so commanded by a spacecraft command). Also, the relays are physically configured orthogonally to each other, in such a way as to minimize the possibility that either of them could be thrown to the off position during launch, mush less both of them. Finally, this configuration has been previously flown (successfully) on NASA spacecraft, although not by APL.

The use of latching relays is preferred over non-latching. If non-latching relays were used, and ground power were interrupted while the relays were held in the off position, the relays would re-connect the battery to the power bus, resulting in a current surge that would overstress the relays, and probably blow fuses in the capacitive filter bank on board. (Note that the battery will normally be brought on-line after ground GSE power has been brought up first, eliminating such surges in normal operation.) The flight battery might also be subjected to an overstress in this case. These events would potentially require the replacement of flight hardware and/or extensive analyses to show hardware had not abed compromised. Uninterruptable power supplies for non-latching relays can mitigate these concerns, but cannot eliminate them, and add cost. The use of latching relays as planned provides for more reliable fault isolation and recovery.

Changes since PDR

1. **Change face sheet of solar array panels from graphite epoxy to aluminum**
   Reason: to reduce solar array substrate weight

2. **Reduce cover glass thickness from 6 mil to 4 mil**
   Reason: reduce S/A add-on mass while meeting mission power requirement.

3. **Connect the outputs of each with solar array wing strings in parallel with isolation diodes and connect each wing peak power tracker modules in parallel with isolation fuses instead of dedicated S/A strings to a module.**
   Reason: Reduce loss of power if one module fails and to make all peak power tracking modules identical.

Changes since PDR (cont.)

4. Replaced the two non-essential load disconnect relays with load shedding sequencing (LVS) in Critical Command Decoder.

   Reason: Reduce weight and single point failure concerns.

5. Solar wings tilt angle changed from 30° to 20°

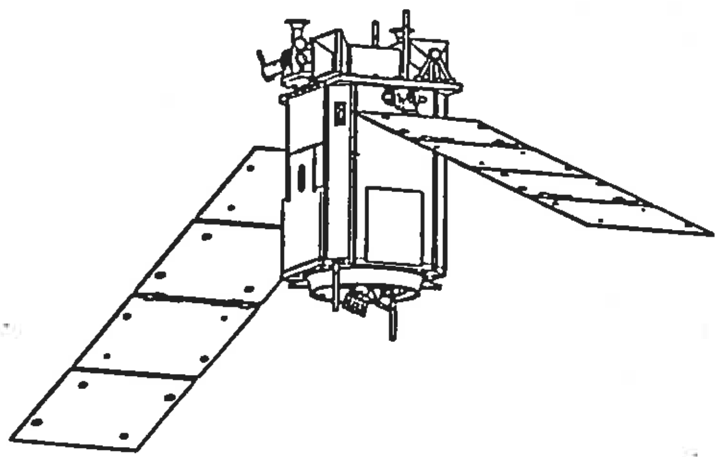
   Reason: To reduce effect of drag induced disturbance torque on spacecraft pointing stability.

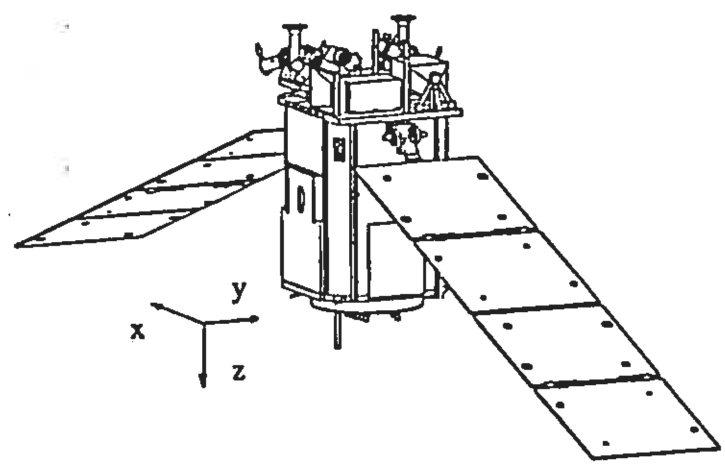
TIMED

Power System Design Drivers

- The requirement to maintain the - Y side in a cold thermal environment, to not block the four instruments' fields of view and to minimize the drag and disturbance torque on the spacecraft during flight impose special demands on the power system design, particularly on the locations width and axis of rotation of the solar array panels.
- The angle between the sun vector and the spacecraft orbit plane, beta, varies between 0 and 180 degrees. The solar array drives compensate for the beta angle variations during the year for optimum sun angle. For Beta >90 degrees the spacecraft is rotated 180 degrees around the orbit plane to maintain the cold side of the spacecraft pointing away from the sun.
- 65° < Beta <115° the spacecraft is in full sun. Otherwise, the sun angle on each solar array wing, its temperature and output power variations during an orbit are sinusoidal.
- Minimum solar power case occurs with maximum eclipse time at Beta angle equal to zero and 180°.

TIMED

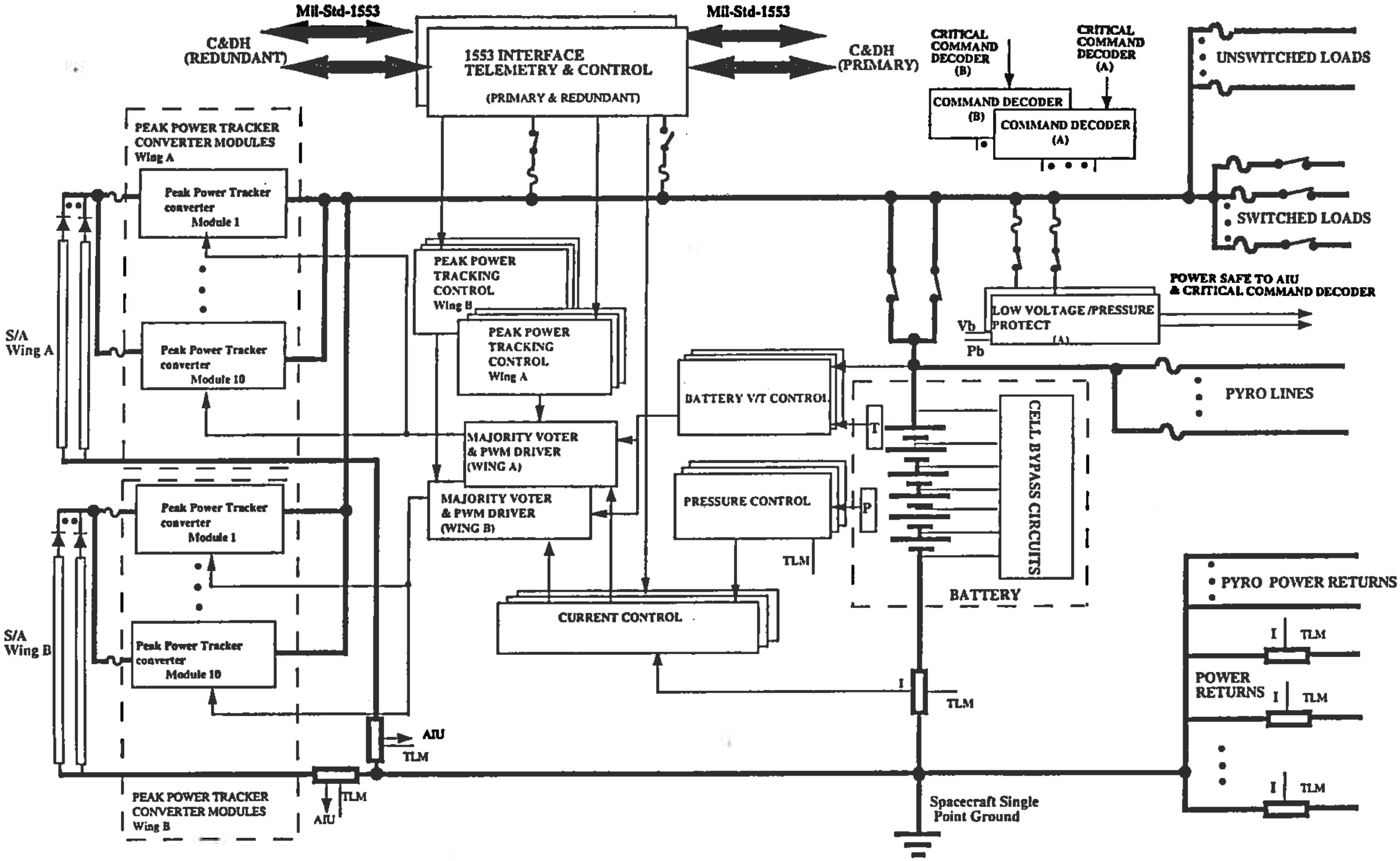




TIMED

Power Systems Configuration

- Two driven solar array wings with shape limited by instrument fields of view, the temperature requirement for SABER, the induced torque imbalance during flight.
- The 20° tilt angle selected to increase the power generation during suntime of the orbit. Also, reduces the peak S/A charge current by cos 20 factor thus lowering the high charge current stresses in the battery, reduces the wiring size and peak current handling of the peak power tracker converter modules. The 20° is a compromise between power system preference and other subsystems.
- The solar arrays are populated with GaAs/Ge cells
- NiH_2 Individual Pressure Vessel (IPV) battery cells were selected because of their superior over-charge tolerance, high specific energy, no memory effect, and the cell pressure gives a very good indication of their state of charge. Operated at lower state of charge where the battery charge efficiency is high which accommodates the sinusoidal shape charge peaks and reduce power dissipation.
- Peak Power Tracking electronics to minimize solar array size.



TIMED Spacecraft Simplified Power System Block Diagram

TIMED

Power System Functional Description

- The TIMED power system is an unregulated bus Peak Power Tracker System with loads connected directly to the battery. The spacecraft bus follows the 22 cell battery voltage.
- The power system hardware consists of:
  - Two solar array wings with four panels per wing populated with GaAs/Ge cells
  - Single NiH_2 battery which consist of two eleven-cell packs in series with a by pass contactor across each cell.
  - Two Peak Power Tracker converter modules (PPT) boxes; each dedicated to one wing.

TIMED

Power System Functional Description (cont.)

- **Power System Electronics/Distribution (PSE/DIST) box which includes:**
  - Solar array power control circuits
  - Battery charge control electronics
  - Battery/bus low voltage protection
  - Battery low pressure protection
  - Serial command interface
  - MIL-STD-1553 interface to C&DH to perform:
    - » Peak Power Tracking Control
    - » Ampere-hour Integration
    - » Battery Charge Control & Protection
    - » Power System telemetry
    - » S/C load current telemetry
    - » S/C load switching status telemetry

Power System Functional Description (cont.)

- Contains all S/C load protection fuses
- Contains all S/C loads switching power control relays & discrete command interface
- Contains relays for firing pyros
- Contains battery disconnect relays
- Contains power diodes to allow battery charging via the umbilical connector
- Contains power diodes to allow relay (command) control during I&T without powering the spacecraft.

• Two Peak Power Tracker fusing and solar array current monitor shunt assemblies, each dedicated to one wing.

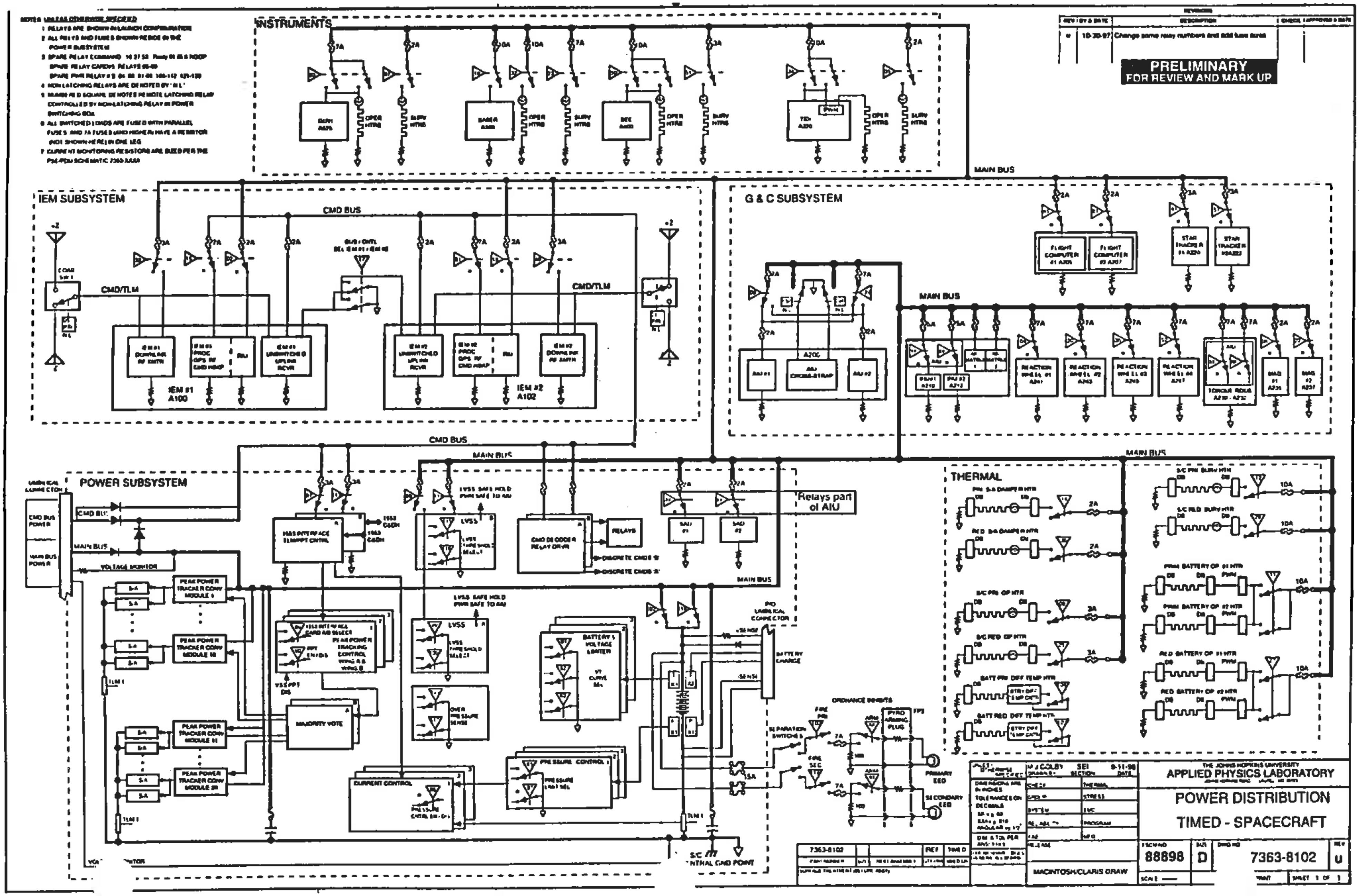
Power System Characteristics

- Bus Voltage variations with the 22 cell NiH2 battery voltage is 22 to 35.
- The power system is designed to support 426W orbital average power at EOL (11% margin).
- Since the two solar array wings can operate at substantially different temperatures, independent peak power tracker electronics for each wing are used.
- The spacecraft C&DH processor performs the primary battery charge control using ampere-hour integration with temperature compensated charge-to-discharge (C/D) ratio control.
- The battery is charged at high rate with available S/A power of the two wings until the C/D ratio is reached, then the charge rate is reduced to a C/100 trickle charge rate by commands from the C&DH computer.
- The battery voltage is limited in hardware to safe voltage levels using eight temperature compensated voltage limits (V/T) which are active simultaneously with the primary battery charge control.

TIMED

Power System Characteristics (cont.)

- If the battery voltage reaches the selected V/T limit, the V/T control circuit will override the peak power tracking control signal from the C&DH and maintain a temperature compensated limit voltage level on the battery. The battery current will continue to taper until the C/D ratio is reached where the C&DH will command the current control circuit to trickle charge.
- The ampere hour integration and C/D ratio control are performed by the spacecraft C&DH computer with the telemetry and commanding done using MIL-STD-1553 interface bus.
- In case of C&DH failures, hardware backups are incorporated in the power system electronics:
  - Majority voted eight level standard V/T control which limits the battery voltage to preset safe charge levels.(Standard NASA/GSFC V/T modified for NiH_2 battery)
  - Selectable temperature compensated maximum pressure limit which switches the charge rate to trickle charge.
- Maximum battery charge current rate limited to C/1.25


INSTRUMENTS
PRELIMINARY
FOR REVIEW AND MARK UP
MAIN BUS
IEM SUBSYSTEM
CMD BUS
CMD/TLM
IEM #1
A100
IEM #2
A102
G & C SUBSYSTEM
CMD BUS
MAIN BUS
POWER SUBSYSTEM
Relays part of AIU
THERMAL
MAIN BUS
APPLIED PHYSICS LABORATORY
POWER DISTRIBUTION
TIMED - SPACECRAFT
88898
D
7363-8102
MACINTOSH/CLARIS DRAW

TIMED

Power System Characteristics (cont.)

- Spacecraft Power Distribution, Switching and Telemetry capabilities:
  - 128 Commands (88 used)
  - 128 Analog Telemetry (75 used)
  - 160 Bilevel Telemetry (107 used)
- All fuses, relays and load current monitors are located in the power system PSE/DIST unit. (AIU contains relays for IRUs, SADs, and Torque Rods)
- The power system monitors the relays status, loads currents, battery and solar array currents, voltages and temperatures.
- Telemetry is sent to the C&DH system through redundant MIL-STD-1553 busses.

Power System Characteristics (cont.)

- Capability to seperately power the C&DH and Critical Command Decoder during ground I&T to allow proper spacecraft configuration before powering the S/C Loads
- Redundant battery disconnect relays to allow battery isolation from S/C bus during I&T and prelaunch
  - Relays can only be commanded OFF by umbilical special 56V command pulses (28V zeners placed in series with disconnect relay coils inside the PSE/DIST unit)

Power System Protection

- Hardware Primary and Redundant Battery Low State of Charge (SOC) protection Low Voltage or pressure sense (LVS).
  - Four voltage limits for BOL, EOL and one cell shorted cases set lower than software limits
  - The power system sends an optically isolated signal to the Critical Command Decoder CCD to generate the commands for non-essential load shedding in case of low battery voltage or pressure.
  - Also sends an optically isolated signal to the attitude control system to place the spacecraft in sun safe mode.
  - Both Low SOC safe protections circuits are disabled during launch and both enabled after solar array deployment.
- In case of C&DH failures which cause a low battery SOC "Safe Hold", the C&DH generated power tracking signal is automatically switched to a fixed reference voltage. The battery charge is performed by the majority voted V/T and pressure control hardware. In this mode:
  - The power system is operated in a non-peak power tracking mode

TIMED

Power System Protection (cont.)

- The battery is charged to the preset V/T limit
- The battery charge current tapers when V/T limit is reached
- When the hardware pressure limit is reached the battery current is switched to C/100 trickle charge.

- Maximum charge current is limited to C/1.25

Power System Interfaces

- The redundant MIL-STD-1553 interface with C&DH perform the following:
  - Peak power tracking algorithm
  - Amper-hour integration and State of Charge calculation
  - Software battery minimum voltage (Four limits for BOL, EOL and one cell shorted cases) and pressure protection
  - Battery max. pressure limit
  - Battery max. temperature limit
  - Fault detection and correction
  - Telemetry of s/c load current, power system temperature, voltage and relay status
- Redundant Serial-Interface for Relay Command
  - Dedicated from A & B side Critical Command Decoder (no cross strapping)
  - Separate lines for Relay Select Data and Relay Gate Pulse
  - Parity check
  - Optical isolation between Critical Command Decoder and Power System Electronics

Power System Autonomy Algorithms

The spacecraft C&DH computer will perform fault detection and correction:

- The C&DH computer will monitor the health (heartbeat) of the PSE/ DIST MIL-STD-1553 interface. If a failure is detected the C&DH will switch to the redundant side.
- The C&DH computer will monitor the battery temperature and pressure. If the battery is charging and the temperature and pressure exceed preset limits for a specified interval then the charging will be switched to trickle.
- The C&DH will monitor the bus voltage and the load current of individual S/C loads. If the power of any load exceeds a preset limit for a specific interval then it is disconnected.
- Low C&DH coulometer counter limit to initiate load shedding.

TIMED

Power System Energy Balance Analysis

- Both APL and GSFC developed energy balance programs were used in TIMED array sizing and verification

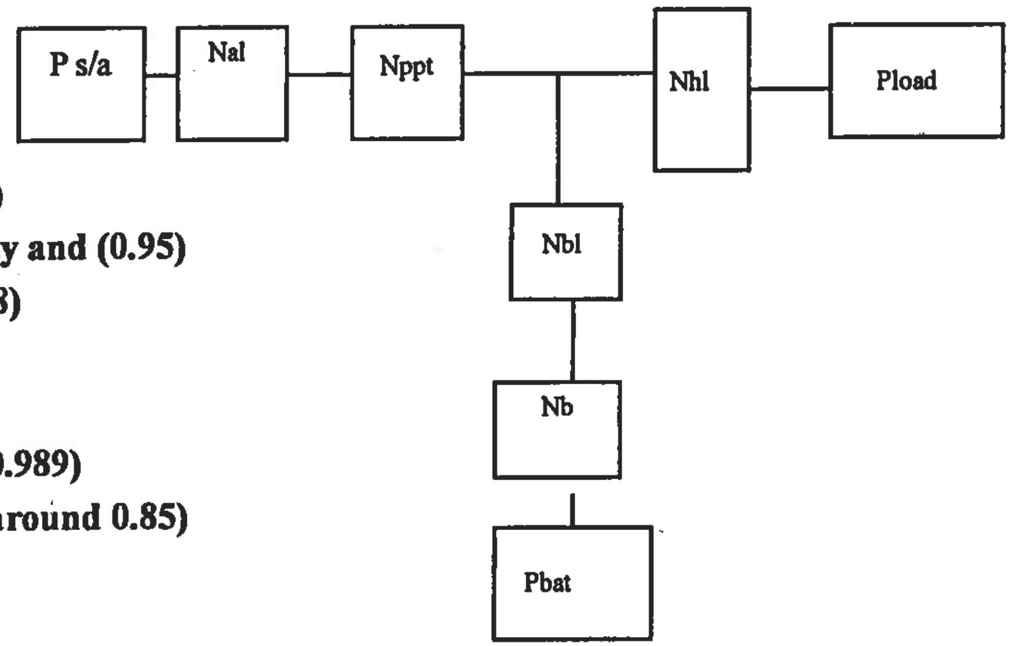
  (DETEB program was developed by J. Jagielski of Code 730 at GSFC. An energy balance program for Direct Energy Transfer topology spacecrafts, with a NiCd battery model. It has been modified for TIMED Peak Power Tracker system and two wing configuration).

  Both programs incorporate effects of:

  - Orbital solar panel sun angle variations
  - Orbital S/C position
  - S/A temperature variations
  - Shadowing effect
- Energy balance analysis verified by testing the power system electronics breadboard using the test battery.

TIMED

Power Subsystem Energy Balance Model



- **P s/a** Solar array power
  Beta = 0 worst case minutes eclipse
  Beta > 66° Full Sun
- **Nal** S/A to Power electronics line loss (0.98)
- **Nppt** Peak power tracker converter efficiency and (0.95)
  peak power tracker accuracy loss (0.98)
- **Nhl** S/C harness loss (0.5V)
- **Pload** S/C orbit average load
- **Nbl** Battery to s/c power bus harness loss (0.989)
- **Nb** Battery orbital Watt-Hour efficiency (around 0.85)
  $\frac{C}{D} \times \frac{Vbatch}{Vbatdis} \times \frac{Tecl}{Tsun}$
- **Pbat** Battery power
- **Tecl** Eclipse time
- **Tsun** Sun time
- **C/D** Charge/Discharge ratio (1.03 to 1.07)
- **Vbatch/Vbatdis** Battery cell average charge to discharge voltage ratio

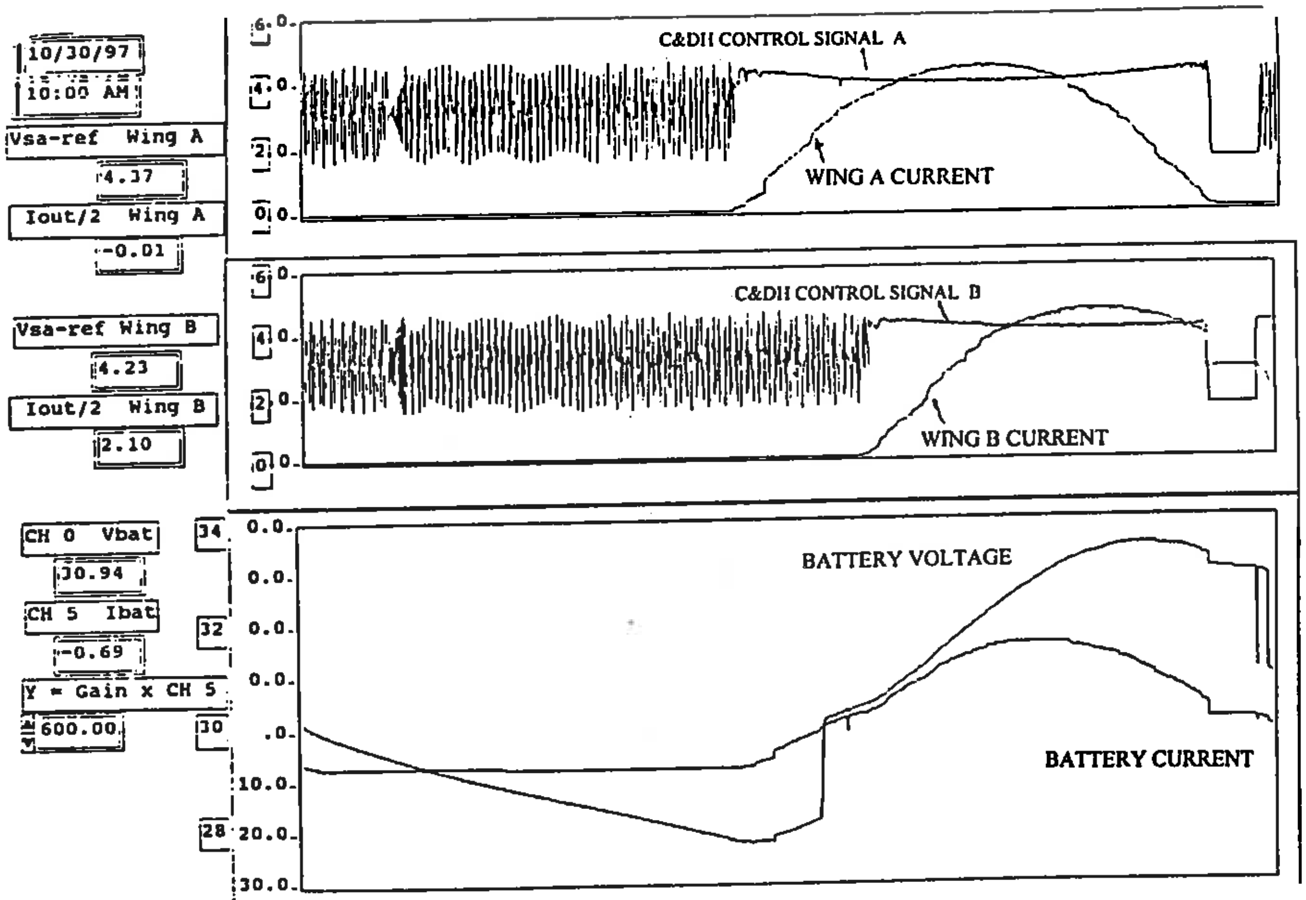
TIMED

Power System Energy Balance Analysis Verification

- The breadboard set-up consists of:
  - Computer driven solar array simulator programmed to provide minimum predicted end-of- life solar array power profiles including shadowing effects from each wing
  - Four peak power tracker modules per wing
  - V/T and constant current controllers
  - Two halves of the test battery (MSX 50 AH cells repackaged into TIMED battery halves).
  - Test data on TIMED cells from GSFC EOS-AM spacecraft life tests were used to modify the charge and discharge voltages to simulate worst case end of life battery behavior.
  - C&DH simulator performing the peak power tracking
  - Constant power load
  - Energy balance conducted with 50% of load power and 50% of S/A power with simulated end of life battery at 22% DOD.

TIMED

Energy Balance Run Plot



This Page intentionally left blank

Solar Array

Solar Array Description

- Two driven wings with four panels per wing
- Each panel size: 47.1” x 49.3”
- 0.625 Al honeycomb with 5 mil thick aluminum face-sheets and 2 mil Kapton insulator
- Total active cell area 109 ft^2
- Six strings per panel
- Each string consists of 59 series cells
- One temperature sensor per panel
- The strings of each wing are connected together through decoupling isolation diodes located on the back of the inner-most panels

TIMED

Solar Cells

- TECSTAR, INC. was Selected for solar panel cells laydown
- GaAs/Ge with dual AR coating
- 5.5 cm x 6.5 cm, 5.5 mil cells
- 4 mil CMX cover glass with UVR coating
- Interconnect: Silver plated Invar
- Absorptance: 0.88 maximum average
- Emittance: 0.87

Solar Cell (cont'd)

Heritage

Cells:	Iridium, MCI, MTSAT, M2A
Interconnect:	TRACE,MCI, MTSAT, M2A, ORBCOM
Cover Glass Adhesive:	All Tecstar panels
Cell adhesive:	All (except GPS program)
Diode board design:	ORBCOM, TRACE, SMEX LITE
End Termination (perforated):	ORBCOM, SMEX LITE, NRL, GPS

TIMED

Solar Array Power Losses / Degradation

	Coeffiecient			
	Voc	Vmp	Imp	Isc
• Assembly loss	10mV	10mV	0.99	0.99
• Coverglass mismatch (CMX/UVR)	-	-	0.99	0.99
• Measurement uncertainties	-	-	0.98	0.98
• Reverse Bias	-	-	1.00	1.00
• Sun Intensity	-	-	0.965	0.965
• UV	-	-	0.98	0.98
• Micrometeorites	-	-	0.99	0.99
• Thermal cycling	0.98	0.98	-	-
• Radiation	0.9475	0.963	0.915	0.9425
• S/A Harness Loss & Diode	-	1.2V	-	-
• Loss of one string	-	-	0.98	0.98

TIMED

Solar Array (cont'd)

- **Shadowing is expected during normal operation. All cells will be screened for reverse bias. Qualification tests will verify performance of the cells for repeated reverse bias at temperature extremes.**
- **Radiation 1 Mev equivalent dosage over two years mission at 95% probability**

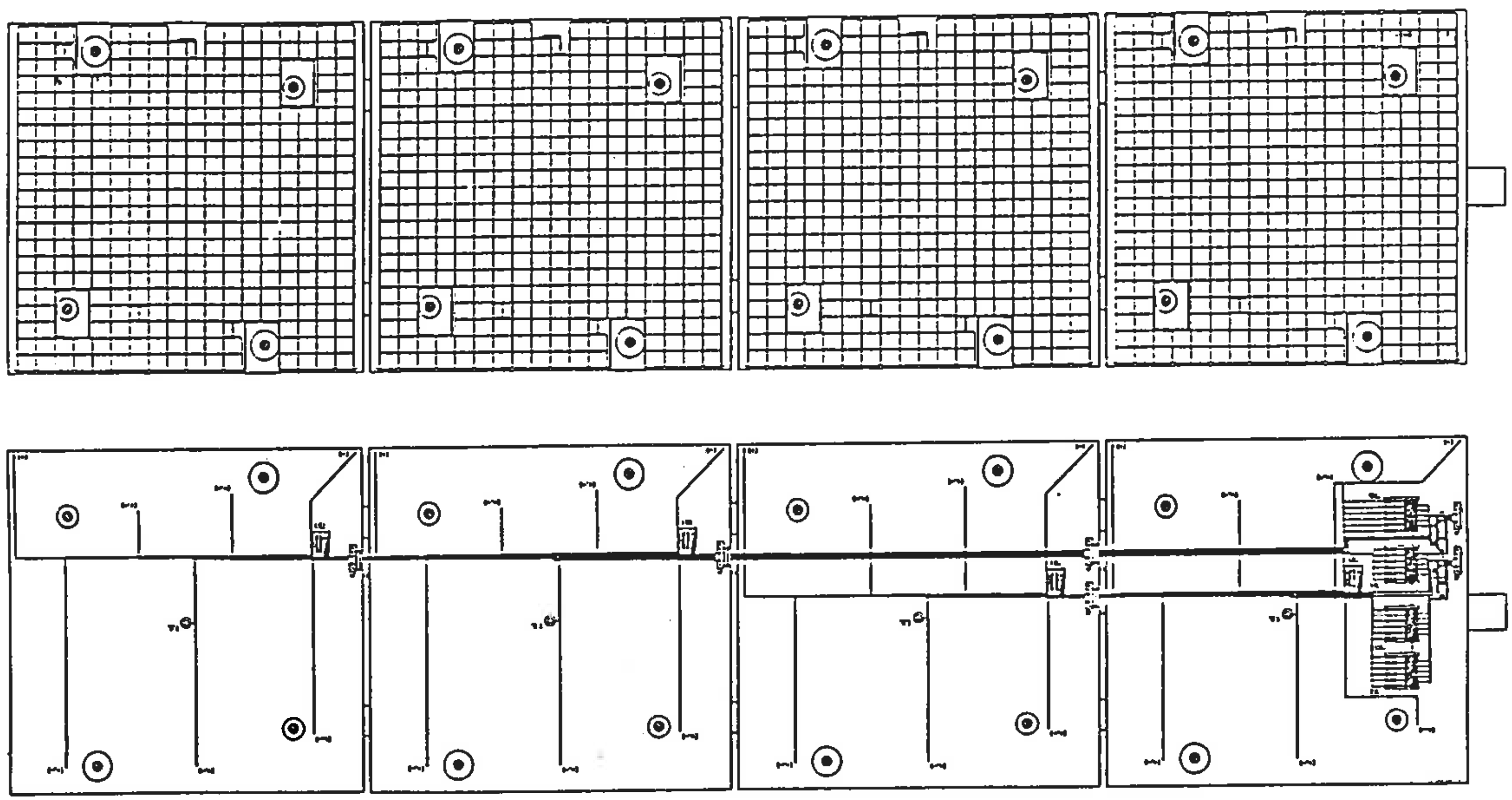
  2.69 E 14 for Voc, Pmp

  1.2 E 14 for Isc

	Panel	Wing
• BOL 28° normal incidence power	301 Watts	1206 Watts
• EOL 80° normal incidence power	229 Watts	916 Watts

TIMED

Preliminary TIMED Solar Array Wing



TIMED

Verification Tests on Qualification Panels

- Intermediate Sequence Defined by the Following List:
  - Visual inspection of Solar Cells, Cover Slides, Interconnects, Wiring
  - X-Ray examination (as required)
  - Adhesion check
  - Power verification
  - LAPSS test at hot temperature
  - Circuit insulation resistance
  - Ohm meter wiring verification
  - Panel weight
- Damage and repair two cells
- Intermediate Sequence
- Thermal Vacuum Bake Out
- TV Cycles (8)
- Intermediate Sequence
- Rapid Temperature Cycles 1 Through 500

TIMED

Verification Tests on Qualification Panels (cont'd)

- Intermediate Sequence
- Rapid Temperature Cycles 501 Through 1000
- Intermediate sequence
- Rapid Temperature Cycles 1001 to 7000
- Intermediate sequence
- Rapid Temperature Cycles 7000 to 12000
- Intermediate sequence

Verification Tests on Flight Panels

- Intermediate Sequence
- Bend Test
- Intermediate Sequence
- Thermal Vacuum Bake Out
- Eight Thermal Vacuum Cycles
- Intermediate Sequence

Battery

TIMED

Battery

- The battery consists of two - eleven individual pressure vessel NiH2 cell stacks in series
- Battery halves are placed on the +x and -x panels
- The worst case cell to cell temperature gradient is controlled to 3 °C
- Thermal sleeves are designed to maintain cell top to sleeve bottom temperature gradient to less than 5 °C
- The flight and flight spare batteries are designed, built, and tested at APL
- Maximum predicted orbital depth of discharge (DOD): 22%
- Orbital operating temperature range: -5 °C to +10 °C
- Launch to Sun Aquisition DOD: 62%
- Battery Launch Temperature: ≤ 25 °C

TIMED

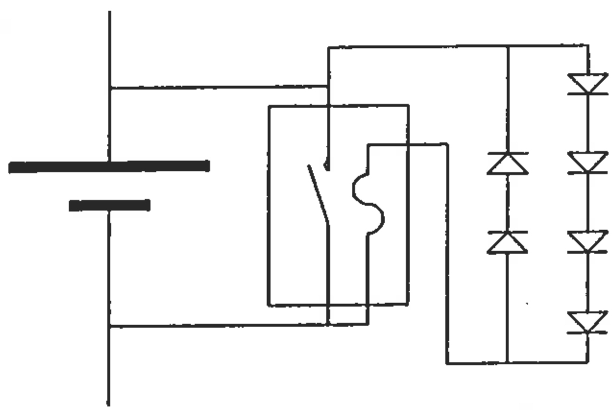
Battery Cells

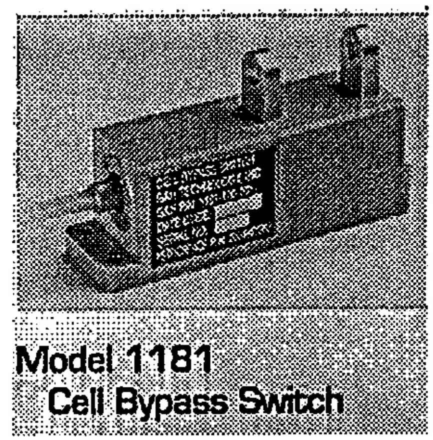
- 50 AHr Individual Pressure Vessel (IPV) cells from Eagle Picher Ind., Joplin, Missouri
- Construction type: Rabbit-Ear Terminals
- Fill tube is through negative electrode
- Positive Electrode sinter: Slurry, Aerospace Qualified
- Separator: Double Zircar
- Negative Electrode: Platinized Hydrophobic Gas Diffusion Membrane
- Electrolyte concentration: 31%
- Electrolyte Management: Catalized Wall Wick
- Length: 8.2", Diameter: 3.5"
- Weight: 1.52 kg
- Maximum operating pressure: 800 psi
- Safety factor: 3:1
- Heritage EOS-AM spacecraft (modified to eliminate separate fill tube)

TIMED

Battery (cont'd)

- Battery cell by pass contactor across each cell to eliminate open cell single point failure



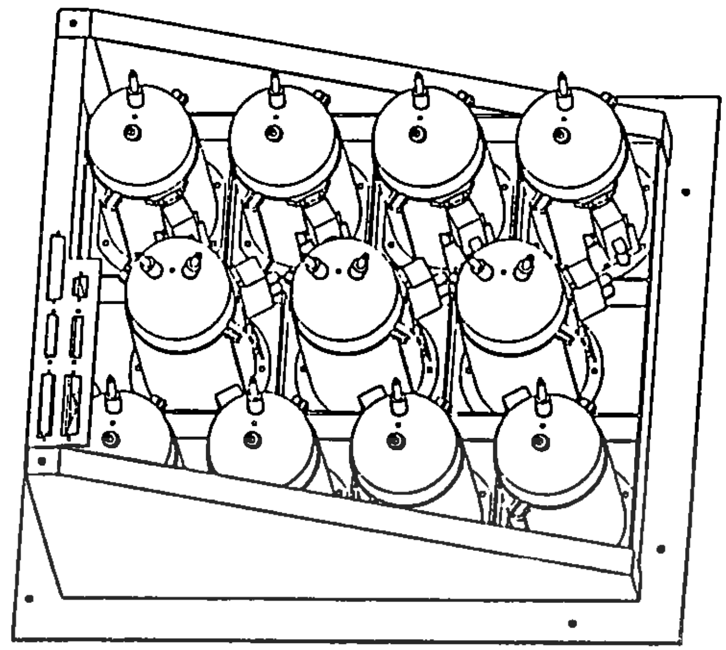


- G & H Technologies cell bypass switch assembly Model 1181
- Heritage qualified and is used on EOS-AM spacecraft batteries
  - Size = 2.925" x 0.850" x 1.50"
  - Weight = 85 grams
- Diodes used to steer current in fusing element

TIMED

Battery (cont'd)

- **Battery half Size/Mass**
  - Mass: 28.15 kg
  - LxWxH 19.3" x 17.7" x 10"

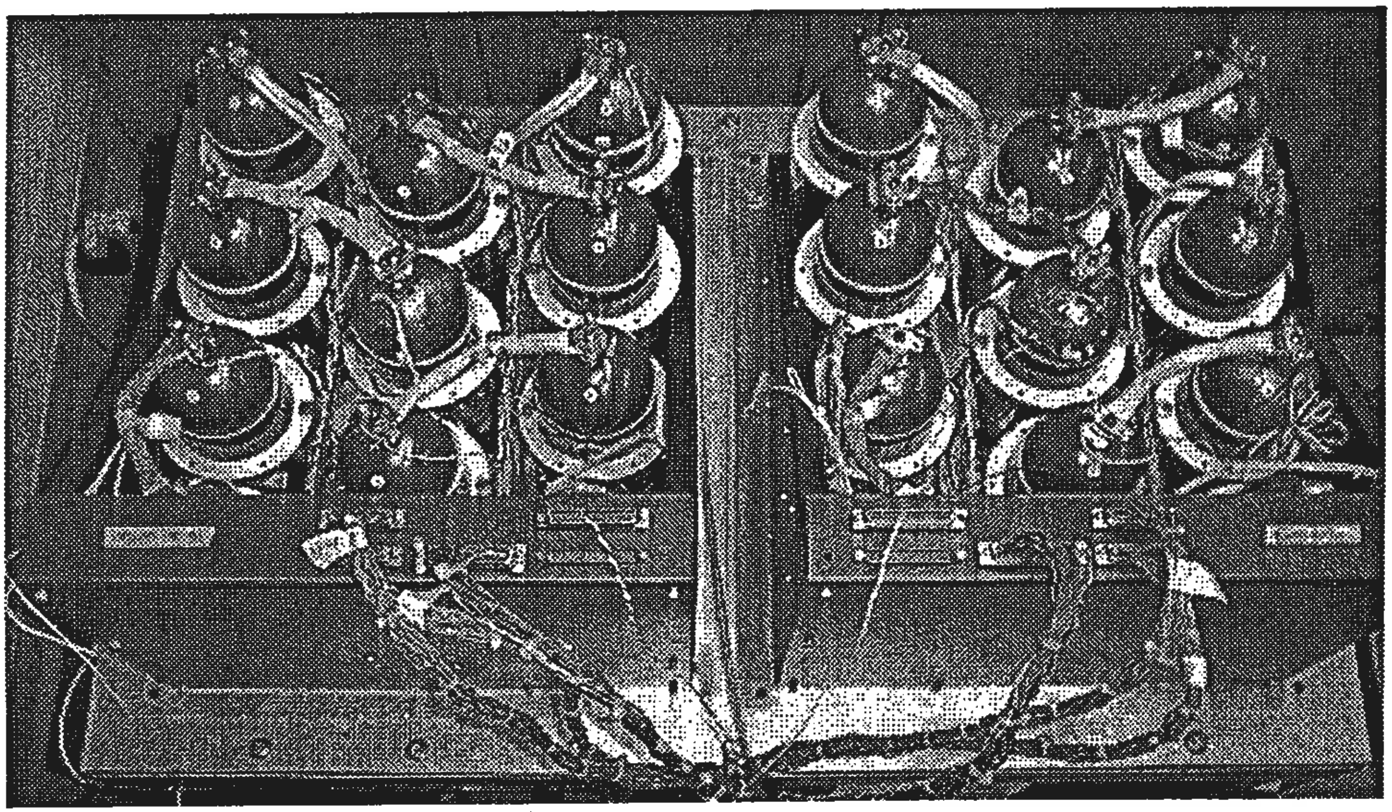


TIMED

TIMED Battery Plan

- One flight and one flight spare batteries
- Test battery: modified MSX test battery. 50 AH IPV cells from Yardney, axial terminals configuration

Photo of Test Battery



Life Test of Cells

- Five cells will be life cycled to simulate TIMED on orbit operation
- Life cycling to start about six months before S/C launch

TIMED

Battery Functional and Performance Verification Tests

Description	Proto-Flight Acceptance
Physical Measurements	X
Visual Inspection	X
Functional Tests	X
Temperature Sensor Operation	@ -5 °, 10 °, 20 °C
Insulation Resistance	X
Electrical Conditioning	X
Electrolyte Leak Test	X
20°C Capacity	X
Charge Retention	X
Vibration	
Sine Survey	X
Sine Sweep Vibration	X
Random Vibration	X
Thermal Vacuum	X
Capacity Tests	@ -5 °, 0 °, 10 °, 20 °C

TIMED

Battery I & T Considerations

- It is desirable to avoid integration of flight and spare batteries for as long as possible.
- Repackaged MSX battery will serve as the TIMED test battery.
- Once integrated maintenance handling requirements defined in handling specifications.
- Open circuit when spacecraft is unattended
- Maximum of 30 days open circuit stand (full) with minimum of weekly top-off charges.
- Thermal considerations
  - Temperature to be maintained below 30°C at all times
  - Typical temperature not to exceed 20°C
  - I & T cooling requirement to be determined from thermal analysis
- Jason Spacecraft Fueling Operations
  - Battery charged and open circuit

TIMED

Battery I & T Considerations (cont'd)

- Shipping
  - Battery empty and open circuit
  - Reconditioning implemented upon arrival
- In the fairing
  - Final reconditioning as close to closing up in fairing as schedule will allow (two weeks to launch, four weeks maximum before reconditioning)
  - Top off within 24 hour of launch, maintain on trickle charge till T-3
  - Desired temperature $\leq 20°C$

TIMED

Procurement Status

Battery

• Contract awarded to Eagle Picher	August 1997
• Cell design review meeting conducted	October 2, 1997
• Plates buy-off review is scheduled	December 11, 1997
• Cell assembly meeting is scheduled	March 1998
• Pre-shipment review is scheduled	October 9, 1998
• Cell shipment to APL	October 29, 1998

Solar Array Cell Lay Down

• Preliminary Design Review	January 1998
• Critical Design Review	March 1998
• Manufacturing Readiness and qual panel test results	May 1998
• Pre-shipment Review	October 30, 1998

PSE - Power System Electronics

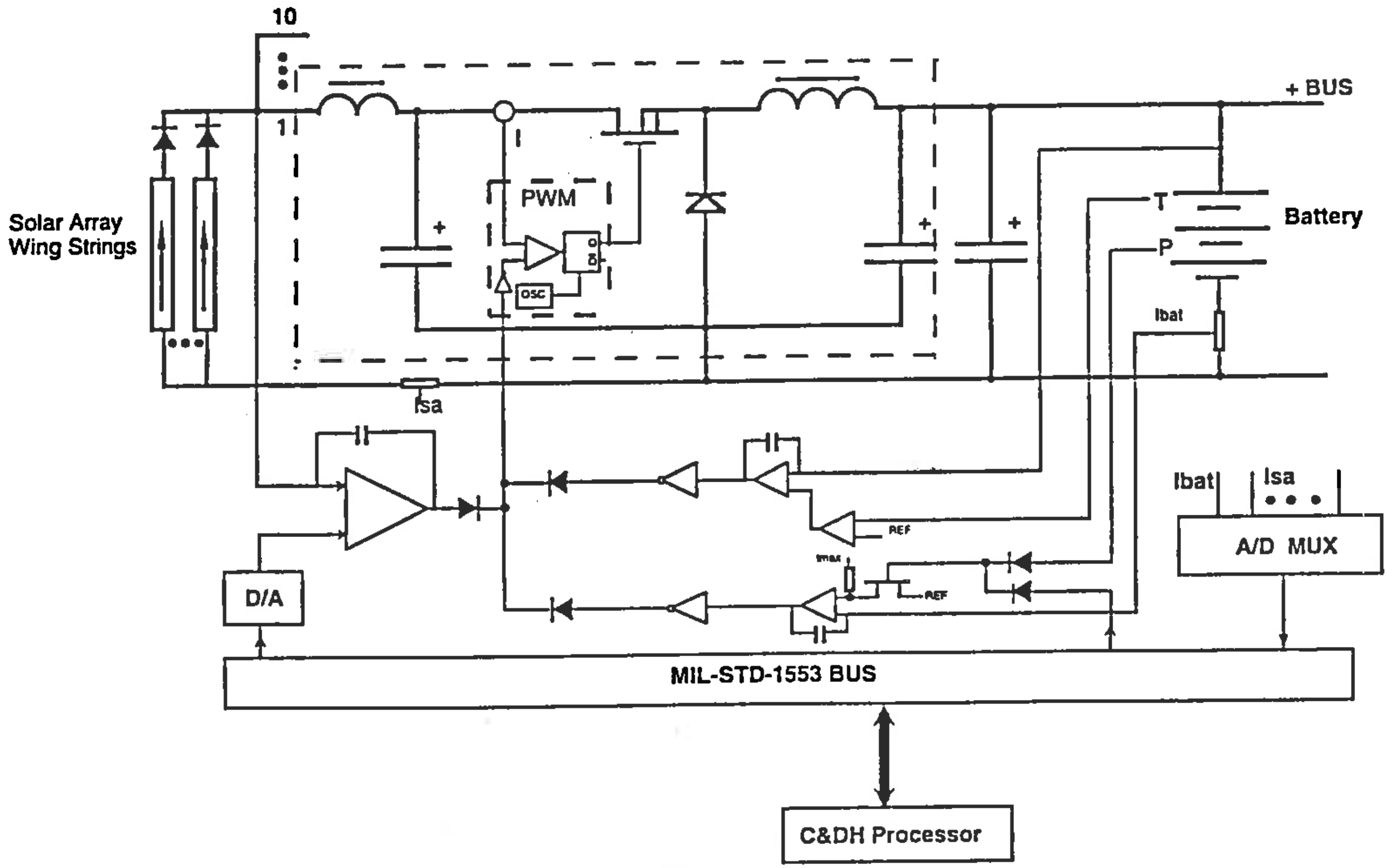
TIMED

Peak Power Tracking Electronics

- Extracts maximum solar array power at all operating conditions (efficiency > 95%)
- Follows the peak within < 1%
- 20 buck converter modules with majority voted controller (10 per wing)
- Independent peak power tracking for each wing
- PPT algorithm in C & DH computer
  (PPT-mode, full State of Charge mode and Search mode)
- Preset hardware back-up operating point
- Majority voted V/T, pressure and constant current controllers
  (reduced power, non peak power tracking)
- V/T and Icc charge control over-ride the C&DH peak power operation and move the S/A operation point toward Voc of S/A IV curve away from peak power point
- Battery charges with maximum available power, the current tapers when V/T is reached. Pressure control places the charge at trickle when pressure limit is reached.
- Maximum battery current limited to C/1.25
- Mention S/A PPT Advantage
- The peak power tracking topology decouples the solar array from the battery and allows extracting all the solar array power.

TIMED

Peak Power Tracker Simplified Circuit Diagram



Power Switching and Distribution

TIMED

Power Switching and Distribution

- Requirements
  - Provide fused power to RCVRs, SAD, IRU, Torque Rods, AIU Relay MATRIX and PSE internal circuitry
  - Provide fused 28V switched power to subsystems
  - Provide pulsed relay outputs for switching relays in other subsystems
  - Provide redundant relay coil drivers and relay telemetry status
  - Provide current monitors for each subsystem
  - Provide fire circuits for pyros
- Electrical Characteristics
  - Redundant Serial Interface
    - » Each serial cmd decoder receives commands from dedicated Critical Command Decoder
    - » Optically coupled interface
    - » Can decode 128 on/off cmds with parity check, (88 on/off cmds used)

TIMED

Power Switching and Distribution (cont'd)

- » Excluding the spare relay card there are seven spare relays
  Spare relays: five 10A, two 2A
- » Separate clock, data, en, and relay gate lines
  - 16 bit data word (8 bit cmd, 8 bit parity check)
    - 3 bits = relay card select
    - 2 bits = row select
    - 2 bits = column select
    - 1 bit = relay state (on/off)
- » Relay pulse approx 100mS

- Electrical Characteistics
  - Redundant relay pulse shaper / current limiter
  - Redundant fusing provided via redundant fuse plugs

1553 INTERFACE

- **Primary and Redundant interface:**
  - **Peak Power Tracker data and control @ 16 Hz rate**
  - **Ahr integration Data @ 16 Hz rate**
  - **Housekeeping Telemetry:**
    - » **S/C Currents (54)**
    - » **Voltages, Temperatures, Pressures (21)**
    - » **Distribution Relay status (105)**
    - » **Solar Array Wing Deployment Status (2)**

This Page Intentionally Left Blank

Breadboard Test Results

TIMED

Breadboard Test Circuit

- The Breadboard of the Power System Electronics was built:
  - Four PPT modules (4x125W) with majority voted controllers for Vsa, V/T, Icc
  - Solar Array simulator
    - » Modified NEAR solar array simulator
    - » Labview on PC and GBIB - interface
    - » Adjustable orbit time (10 to 100 min.)
  - C&DH simulator with PPT - and Ahr - algorithms written C++ on PC and use National Instrument - DAC card
    - » Adjustable sample rate up to 50 Hz (16 Hz used during breadboard testing)
  - Data logging / display / performance measurements with HP-DAC
    - » Labview on PC and GBIB - interface
  - Modified NEAR battery simulators used

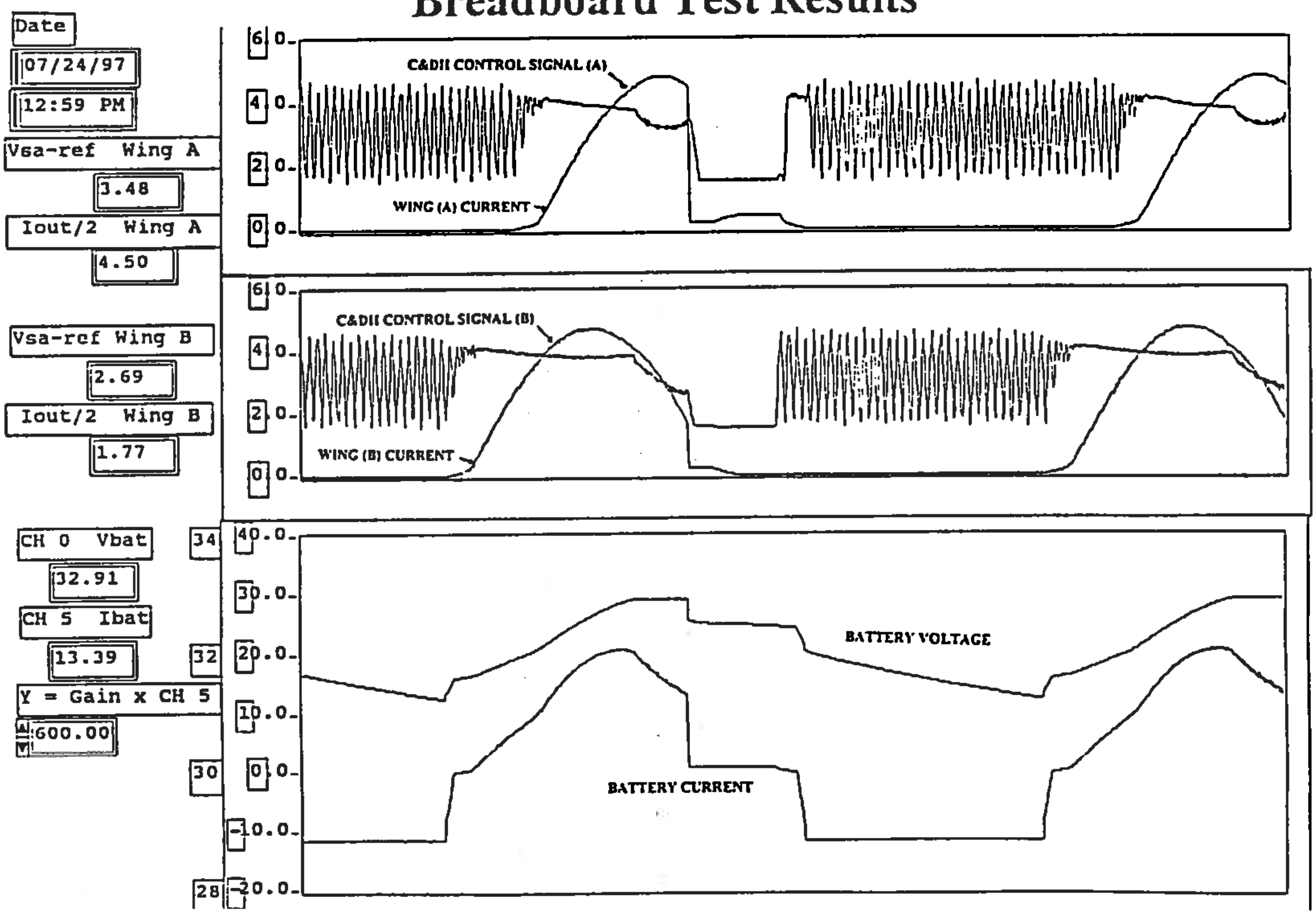
TIMED

Breadboard Performance Tests

- Real time orbit simulations have been performed to evaluate the Peak Power - tracking and Amper -hour integration algorithms during battery charge/discharge with the Vsa,Vt, Icc controllers
- The measured controller bandwidth
  - Vsa loop 200 - 300 Hz
  - V/T loop 200 - 500 Hz
  - Icc loop 250 - 350 Hz
- Measured peak power module:
  - Full load efficiency > 96%
  - PPT tracking accuracy 0.7%

TIMED

Breadboard Test Results



This Page Intentionally Left Blank

Power System Mechanical

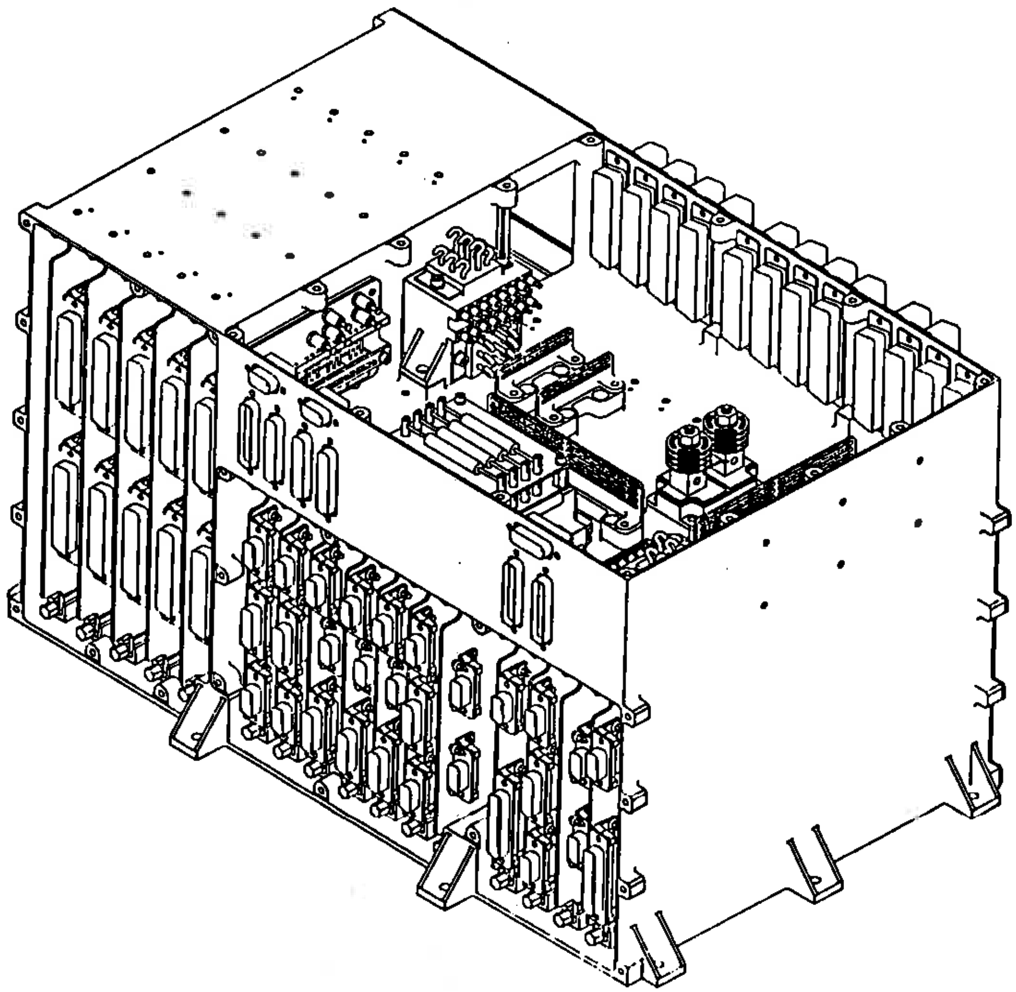
TIMED

The Power System Mechanical Design

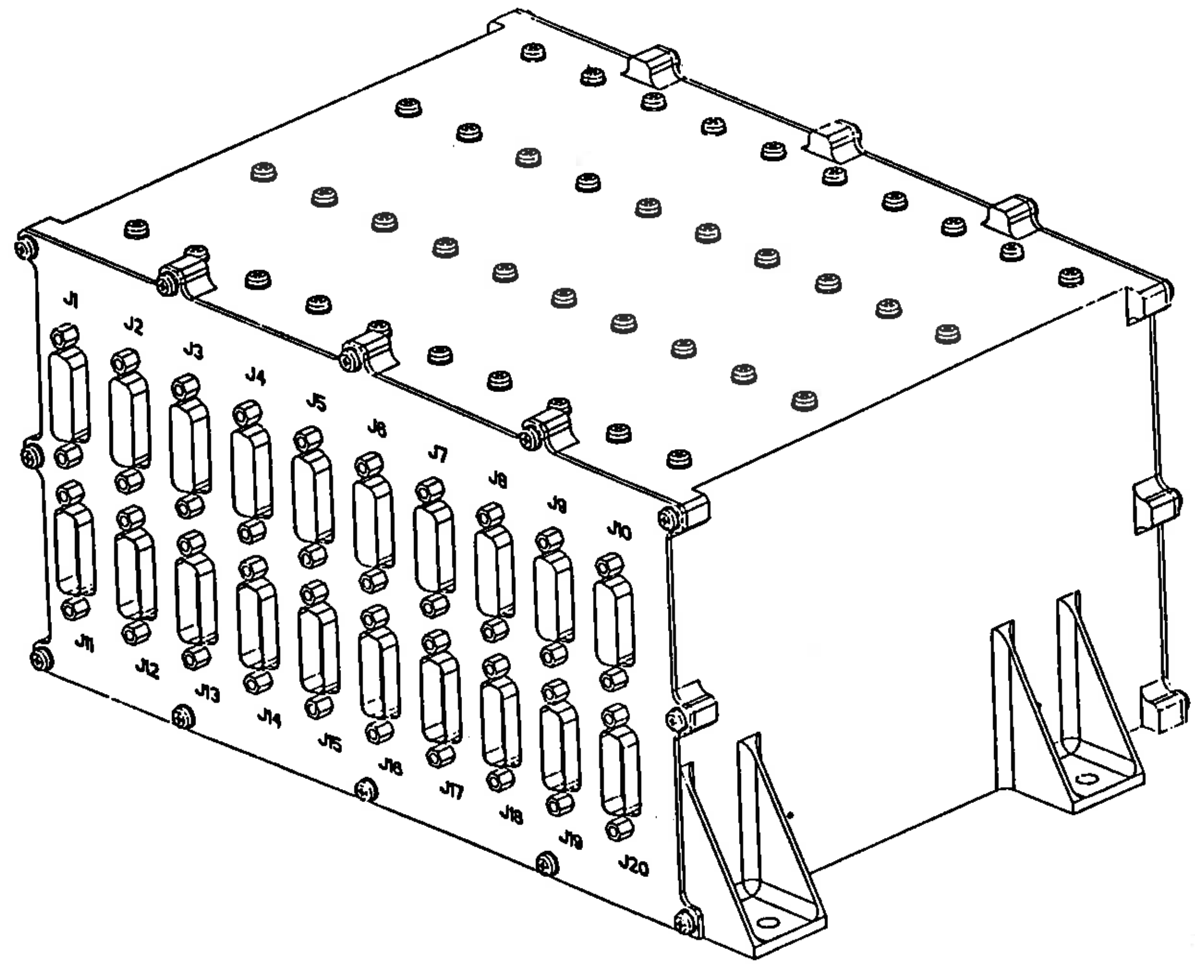
	L x W x H	Weight
Power System Electronics and Distribution: (PSE/DIST)	18.1" x 11.5" x 9.6"	20.6 Kg
(2) Peak Power Tracker Converter Units: (PPTC)	11.1" x 6.8" x 4.9"	5.6 Kg
(2) Solar Array Fuse and Current Sense Assemblies:	2.5" x 3.0" x 2.5"	0.5 Kg

TIMED

Power System Electronics/Distribution Unit



Peak Power Tracker Unit

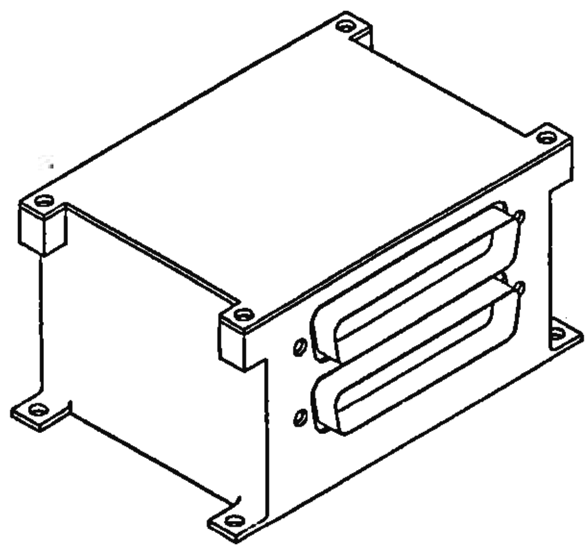


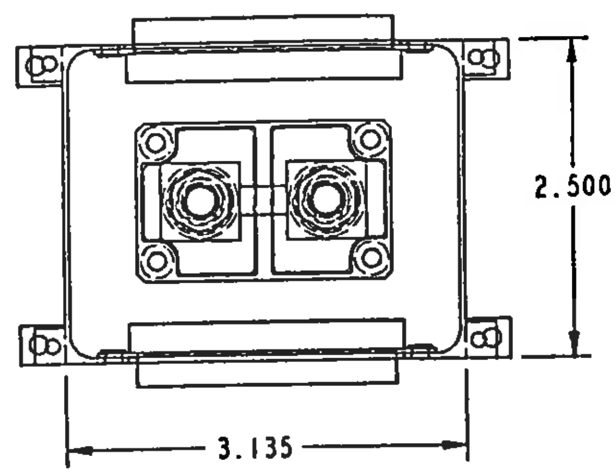
Solar Array - Fuse / Junction Box

One box per Solar Array wing

Fuses to isolate failed PPT module

Solar Array current shunt





Appendix

PSE Relay Command List, TT Address, and Current Channel Address 11/13/97

CMD/TT Signal (Relay Card #1)	Command Byte For ON:X=1; OFF: X=0		Addresses at PSE MB Level: Bilevel Addr TT	En-TT	Current Addr CS	Tlm-Sel3210	Current Signal
1. NOOP On/Off	0000000X		1	1	1	0000	Rcvr #1
2. RIU #1 On/Off	0000001X		1	2	1	0001	RIU #1
3. GUVI On/ Off	0000010X		1	3	1	0010	GUVI
4. React Wh#1 On/Off	0000011X		1	4	1	0011	React Wh#1
5. RF Sw #1 Sel Omni/Nadir	0000100X		1	5	1	0100	Not Used
6. Mag #1 On/Off	0000101X		1	6	1	0101	Mag #1
7. GUVI Surv Ht On/Off	0000110X		1	7	1	0110	GUVI Surv Ht
8. Prim Relay AIU #1 or #2 Pwr	0000111X		1	8	1	0111	AIU #1
9. Op Hts #1 On/Off	0001000X		2	1	1	1000	Op Hts #1
10. P_Optical Bench Pyro Sel/Safe	0001001X		2	2	1	1001	Not Used
11. Btry Prim Hts On/Off	0001010X		2	3	1	1010	Btry Prim Hts
12. LVS Surv Prim Hts #1 On/Off	0001011X		2	4	1	1011	LVS Surv Prim Hts #1
13. P_Sel AIU #1/#2 Active	0001100X	no TT	2	5	1	1100	GUVI Op Htr
14. S/A Damper Prim Hts On/Off	0001101X		2	6	1	1101	S/A Damper Prim Hts
15. IEM #1 On/Off	0001110X		2	7	1	1110	IEM #1
16. Spare	0001111X		2	8	1	1111	Spare

CMDS	CS	TT
16	14	15

CMD/TT Signal (Relay Card #2)	For ON:X=1; OFF: X=0		TT	En-TT	CS	Tlm-Sel3210	Current Signal
17. Select Bus Controller	0010000X		3	1	2	0000	Rcvr #2
18. RIU #2 On/Off	0010001X		3	2	2	0001	RIU #2
19. SABER On/ Off	0010010X		3	3	2	0010	SABER
20. React Wh# 2 On/Off	0010011X		3	4	2	0011	React Wh# 2
21. RF Sw #2 Sel Omni/Nadir	0010100X		3	5	2	0100	Not Used
22. Mag #2 On/Off	0010101X		3	6	2	0101	Mag #2
23. SABER Surv Ht On/Off	0010110X		3	7	2	0110	SABER Surv Ht
24. Red Relay AIU #1 or #2 Pwr	0010111X		3	8	2	0111	AIU #2
25. Op Hts #2 On/Off	0011000X		4	1	2	1000	Op Hts #2
26. R_Optical Bench Pyro Sel/Safe	0011001X		4	2	2	1001	Not Used
27. Btry Red Hts On/Off	0011010X		4	3	2	1010	Btry Red Hts
28. LVS Safe Hts #2 On/Off	0011011X		4	4	2	1011	LVS Surv Red Hts #2
29. R_Sel AIU #1/#2 Active	0011100X	no TT	4	5	2	1100	Not Used
30. S/A Damper Red Hts On/Off	0011101X		4	6	2	1101	S/A Damper Red Hts
31. IEM #2 On/Off	0011110X		4	7	2	1110	IEM #2
32. SABER Op. Heater On/Off	0011111X		4	8	2	1111	SABER Op. Heater

CMDS	CS	TT
16	13	15

CMD/TT Signal (Relay Card #3)	Command Byte For ON:X=1; OFF: X=0	Bilevel Addr TT	En-TT	Current Addr CS	Tlm-Sel3210	Current Signal
33. XMTR #1 On/Off	0100000X	5	1	3	0000	XMTR #1
34. TIDI On/Off	0100001X	5	2	3	0001	TIDI
35. TIDI Surv Hts On/Off	0100010X	5	3	3	0010	TIDI Surv Hts
36. React Wh #3 On/Off	0100011X	5	4	3	0011	React Wh #3
37. Spare Reset	0100100X	5	5	3	0100	IRU #1
38. P_X+ S/A Pyro #1 Sel/Safe	0100101X	5	6	3	0101	SAD #1
39. P_X+ S/A Pyro #2 Sel/Safe	0100110X	5	7	3	0110	Prime Torque Rods
40. P_X- S/A Pyro #1 Sel/Safe	0100111X	5	8	3	0111	Not Used
41. Star Camera #1 On/Off	0101000X	6	1	3	1000	Star Camera #1
42. P_X- S/A Pyro #2 Sel/Safe	0101001X	6	2	3	1001	Not Used
43. P_GUVI Pyro Sel/Safe	0101010X	6	3	3	1010	Not Used
44. Spare	0101011X	6	4	3	1011	Spare
45. Flight Computer #1 On/Off	0101100X	6	5	3	1100	Flight Computer #1
46. Spare	0101101X	6	6	3	1101	Spare
47. P_TIDI Pyro #1/2 Sel/Safe	0101110X	6	7	3	1110	Spare
48. P_TIDI Pyro #3/4 Sel/Safe	0101111X	6	8	3	1111	TIDI Op Htr

CMDS	CS	TT
16	13	16

CMD/TT Signal (Relay Card #4)	For ON:X=1; OFF: X=0	TT	En-TT	CS	Tlm-Sel3210	Current Signal
49. XMTR #2 On/Off	0110000X	7	1	4	0000	XMTR #2
50. SEE On/Off	0110001X	7	2	4	0001	SEE
51. SEE Surv Hts On/Off	0110010X	7	3	4	0010	SEE Surv Hts
52. React Wh #4 On/Off	0110011X	7	4	4	0011	React Wh #4
53. Spare Reset	0110100X	7	5	4	0100	IRU #2
54. R_X+ S/A Pyro #1 Sel/Safe	0110101X	7	6	4	0101	SAD #2
55. R_X+ S/A Pyro #2 Sel/Safe	0110110X	7	7	4	0110	Red Torque Rods
56. R_X- S/A Pyro #1 Sel/Safe	0110111X	7	8	4	0111	Not Used
57. Star Camera #2 On/Off	0111000X	8	1	4	1000	Star Camera #2
58. R_X- S/A Pyro #2 Sel/Safe	0111001X	8	2	4	1001	Not Used
59. R_GUVI Pyro Sel/Safe	0111010X	8	3	4	1010	Not Used
60. Spare	0111011X	8	4	4	1011	Spare
61. Flight Computer #2 On/Off	0111100X	8	5	4	1100	Flight Computer #2
62. Spare	0111101X	8	6	4	1101	Spare
63. R_TIDI Pyro #1/2 Sel/Safe	0111110X	8	7	4	1110	Spare
64. R_TIDI Pyro #3/4 Sel/Safe	0111111X	8	8	4	1111	SEE Op Htr

CMDS	CS	TT
16	13	16

CMD/TT Signal (Relay Card #5)	Command Byte For ON:X=1; OFF: X=0	Bilevel Addr TT	En-TT	Current Addr CS	Tlm-Sel3210	Current Signal
65. spare	1000000X	9	1	5	0000	spare
66. spare	1000001X	9	2	5	0001	spare
67. spare	1000010X	9	3	5	0010	spare
68. spare	1000011X	9	4	5	0011	spare
69. spare	1000100X	9	5	5	0100	spare
70. spare	1000101X	9	6	5	0101	spare
71. spare	1000110X	9	7	5	0110	spare
72. spare	1000111X	9	8	5	0111	spare
73. spare	1001000X	10	1	5	1000	spare
74. spare	1001001X	10	2	5	1001	spare
75. spare	1001010X	10	3	5	1010	spare
76. spare	1001011X	10	4	5	1011	spare
77. spare	1001100X	10	5	5	1100	spare
78. spare	1001101X	10	6	5	1101	spare
79. spare	1001110X	10	7	5	1110	spare
80. spare	1001111X	10	8	5	1111	spare

CMD/TT Signal (Controller 1,2,3) — Cntr 1,2,3 (The three Controller cards have the same relay address, different TT addresses)

CMD/TT Signal (Controller 1,2,3)	Command Byte	Cntr 1,2,3	En-TT
81. VT Level Bit 1 Set/Reset	1010000X	11,13,15	1
82. VT Level Bit 2 Set/Reset	1010001X	11,13,15	2
83. VT Level Bit 3 Set/Reset	1010010X	11,13,15	3
84. not used	1010011X	11,13,15	4
85. Btry Press Bit 1 Set/Reset	1010100X	11,13,15	5
86. Btry Pres En/Dis	1010101X	11,13,15	6
87. Btry Press Bit 2 Set/Reset	1010110X	11,13,15	7
88. not used	1010111X	11,13,15	8
89. PSE 1553 A/B Card Sel. for PPT/AHI	1011000X	12,14,16	1
90. PPT & AHI En/Dis	1011001X	12,14,16	2
91. Battery Charge Rate Select (No relay)	1011010X	12,14,16	3
92. not used	1011011X	12,14,16	4
93. not used	1011100X	12,14,16	5
94. not used	1011101X	12,14,16	6
95. not used	1011110X	12,14,16	7
96. not used	1011111X	12,14,16	8

CMDS	CS	TT
8	0	27

CMD/TT Signal (Pwr Conv A, LVSA)	Command Byte ON:X=1; OFF: X=0	Bilevel Addr TT	En-TT
97. PSE 1553 Interf A On/Off	1100000X	17	1
98. LVS A On/Off	1100001X	17	2
99. LVS A Voltage Bit 1 Set/Reset	1100010X	17	3
100.LVS A Voltage Bit 2 Set/Reset	1100011X	17	4
101.LVS A Pressure Bit 1 Set/Reset	1100100X	17	5
102.Btry Disconnect Relay #1 En (1)	11001011	17	6
103.Prim Ordnance Relay Fire/Safe	1100110X	17	7
104.Btry Prim Diff Temp Cntr On/Off	1100111X	17	8
105.not used	1101000X	18	1
106.not used	1101001X	18	2
107.not used	1101010X	18	3
108.not used	1101011X	18	4
109.not used	1101100X	18	5
110.not used	1101101X	18	6
111.not used	1101110X	18	7
112.not used	1101111X	18	8

Current Addr CS	Tlm-Sel3210	Current Signal
6	XXXX	Prime 1553 A #1 DC/DC Converter

CMDS	CS	TT
8	1	8

CMD/TT Signal (Pwr Conv B, LVS B)	ON:X=1; OFF: X=0	TT	En-TT
113.PSE 1553 Interf B On/Off	1110000X	19	1
114.LVS B On/Off	1110001X	19	2
115.LVS B Voltage Bit 1 Set/Reset	1110010X	19	3
116.LVS B Voltage Bit 2 Set/Reset	1110011X	19	4
117.LVS B Pressure Bit 1 Set/Reset	1110100X	19	5
118.Btry Disconnect Relay #2 En (1)	11101011	19	6
119.Red Ordnance Relay Fire/Safe	1110110X	19	7
120.Btry Red Diff Temp Cntr On/Off	1110111X	19	8
121.not used	1111000X	20	1
122.not used	1111001X	20	2
123.not used	1111010X	20	3
124.not used	1111011X	20	4
125.not used	1111100X	20	5
126.not used	1111101X	20	6
127.not used	1111110X	20	7
128.not used	1111111X	20	8

CS	Tlm-Sel3210	Current Signal
7	XXXX	Redundant 1553 B #2 DC/DC Converter

CMDS	CS	TT
8	1	8

Prime Analog Card	Command Byte For ON, X=1; for OFF, X=0	Bilevel Addr TT En-TT	Current Addr Mux Sel (9:0)	Analog Signal
SA Wing A TT		21 3		
SA Wing B TT		21 4		
			000XXXXXX	BAT_I
			001XXXXXX	SA_WA_I
			010XXXXXX	SA_WB_I
			0110000XXX	SA_WA
			0110001XXX	SA_WB
			0110010XXX	MBUS
			0110011XXX	BAT_HS1
			0110100XXX	BAT_HS2
			0110101XXX	BAT_P1
			0110110XXX	BAT_P2
			0110111XXX	VREF_5V
			0111000XXX	BAT_P3
			0111001XXX	NPPTA
			0111010XXX	NPPTB
			0111100XXX	Spare1
			0111101XXX	Spare2
			0111110XXX	Spare3
			100XXXX000	CS_TLM1
			100XXXX001	CS_TLM2
			100XXXX010	CS_TLM3
			100XXXX011	CS_TLM4
			100XXXX100	CS_TLM5
			100XXXX101	CS_TLM6
			100XXXX110	CS_TLM7
			100XXXX111	CS_TLM8
			101X000XXX	BAT_T1
			101X001XXX	BAT_T2
			101X010XXX	PPTA_T
			101X011XXX	PPTB_T
			101X100XXX	PSE1_T
			101X101XXX	PSE2_T
			110X000XXX	SA_WINGA_T1
			110X001XXX	SA_WINGA_T2
			110X100XXX	SA_WINGB_T1
			110X101XXX	SA_WINGB_T2

CMDS	CS	TT
0	3	2

Relay Command Byte Decode								
Bit	MSB	b6	b5	b4	b3	b2	b1	LSB
Signal	CS2	CS1	CS0	C1	C0	R1	R0	ON/OFF*
Name	Card Select			Column Select		Row Select		ON/OFF*

POWER SYSTEM DISTRIBUTION TOTALS					
COMMANDS	S/C CURRENTS	TELLTALES	VOLTAGES	PRESSURES	TEMPERATURES
88	58	107	8	3	10