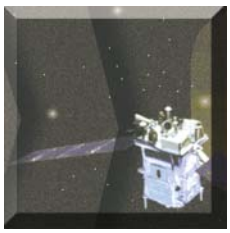

TIMED Integrated Electronics Module (IEM)

Paul C. Marth

The Thermosphere, Ionosphere, Mesosphere Energetics and Dynamics (TIMED) program is the first to use the Integrated Electronics Module (IEM) spacecraft architecture. The IEM is based on the idea of incorporating the electronics for several spacecraft subsystems into a single chassis using plug-in cards. In addition to the space and mass savings realized with this approach, the concept can be adapted to many space missions over an extended period, providing savings by building on prior configurations rather than "starting from scratch." The command and data handling, Global Positioning System Navigation, and RF communications subsystems, along with associated power converters, are packaged in the TIMED IEM. This article describes the adaptation of the IEM concept for the TIMED mission, which has been operating flawlessly since it was launched on 7 December 2001.

INTRODUCTION

In the mid-1990s, the APL Space Department formed the Advanced Satellite Technology Committee to investigate and recommend architectures for future space projects. One of the proposed concepts was an Integrated Electronics Module (IEM) that would hold core spacecraft electronics subsystems. A subcommittee was tasked to further develop this concept.[1] The basic idea was to implement, in a single chassis, multiple spacecraft subsystems that are normally constructed as stand-alone entities to achieve the overall functions needed for a spacecraft. This construction is known as the traditional "box-and-harness" approach.

Adapting the IEM concept was projected to conserve critical spacecraft commodities (i.e., mass, size, and power) at a reduced cost. Use of advanced technology components was the key to achieving these savings, estimated at 20 to 30%.

The subcommittee established three categories of requirements for the IEM: Vital, Important, and Bells and Whistles. Table 1, excerpted from the committee report, lists the essential requirements under each category. Many of these requirements have been achieved in the various IEMs for the TIMED, CONTOUR, MESSENGER, and STEREO spacecraft.[2] (Complete information on the TIMED mission, including participants, status, science, etc., may be found at http://www.timed.jhuapl.edu/mission/.) While the IEMs for each spacecraft have different configurations and complements of subsystems, the basic concept is characteristic of all.

The TIMED spacecraft was the first to embrace the IEM concept. Of the six major TIMED subsystems, four were selected for the IEM: (1) command and data handling (C&DH), (2) GPS Navigation System (GNS), (3) RF telecommunications, and (4) IEM power

Table 1. IEM requirements.

Requirement category	Requirement
Vital	Useable over at least a 10-year lifetime
	Interconnect 1–20 slots with I/O traffic
	Card design unaffected by slot position
	5–10 MB/s now, with growth potential
	Fault tolerant
	Processor independent
	Useable in a space radiation environment
	Simple bus interface hardware
	Productive and cost-effective software tools
	Commercially available breadboard equipment
Important	Low power consumption
	Error code–protected data transfers
Bells and Whistles	Compatible with industry standards
	Support multiple, tightly coupled processors
	Dynamically chosen bus master
	Burst mode and/or message-based transaction support

conditioning. Figure 1 is a block diagram of the IEM. Nine cards are used for the four subsystems. (TIMED uses two IEMs for redundancy.) Figures 2a and 2b are photographs of a TIMED flight unit with and without the front cover.

IEM CONSTRUCTION

The IEM chassis (Fig. 3) is constructed from a single block of aluminum with internal rounded corners for stiffness. The motherboard, a multilayer printed circuit board (PCB) with connectors for plug-in cards, is mounted to the frame. The frame is precisely positioned in the chassis and pinned in place to ensure accurate alignment for card installation. Card insertion guides with wedge-locking hardware hold the cards in place and provide the primary thermal conduction path for heat from the cards. The cards and motherboard connectors have insertion guide-pins that are keyed to provide card-unique locations.

The use of plug-in cards for each subsystem mentioned above (ideally one card per subsystem) is a major IEM characteristic. The motherboard, mounted to the chassis, handles the inter-card connections. An extension of the motherboard contains connectors that provide

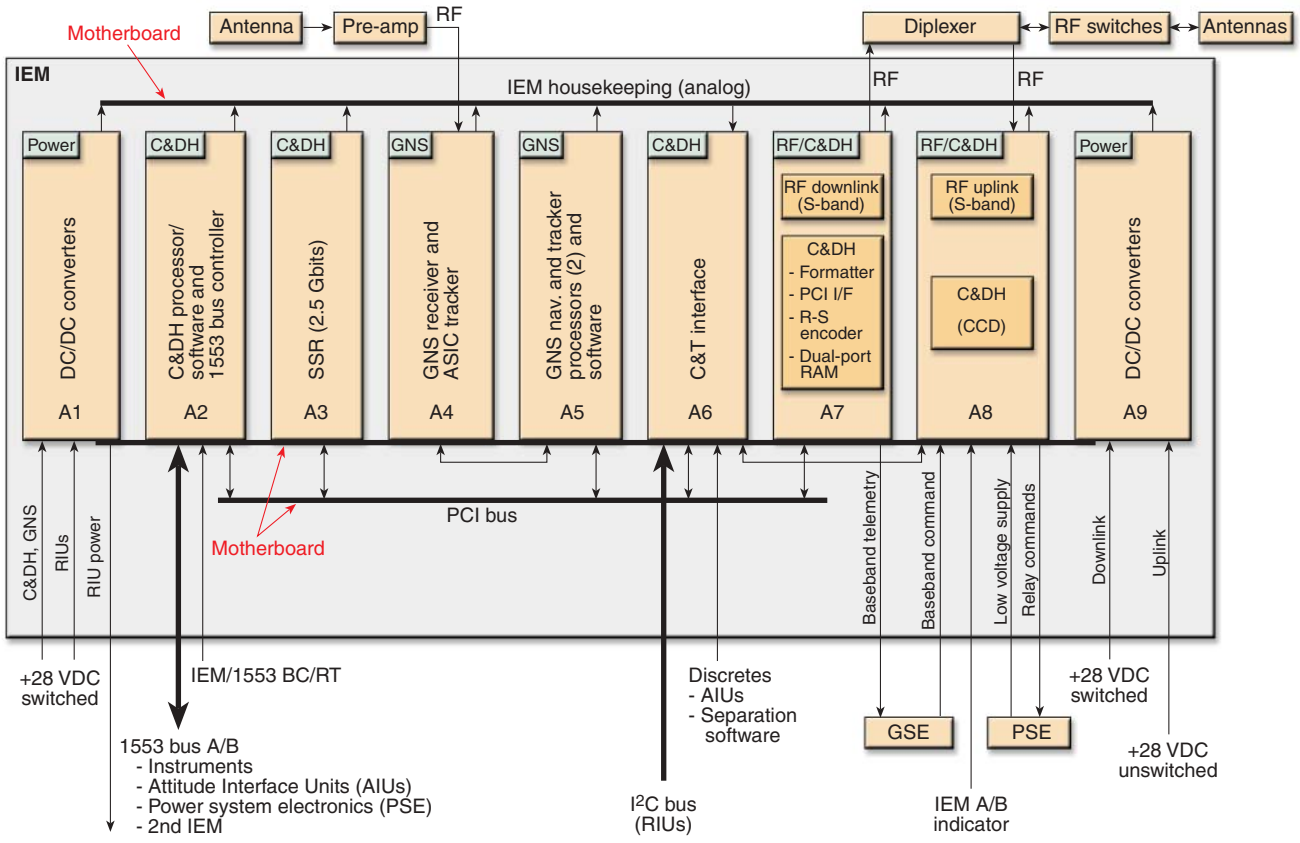

Figure 1. TIMED IEM block diagram.

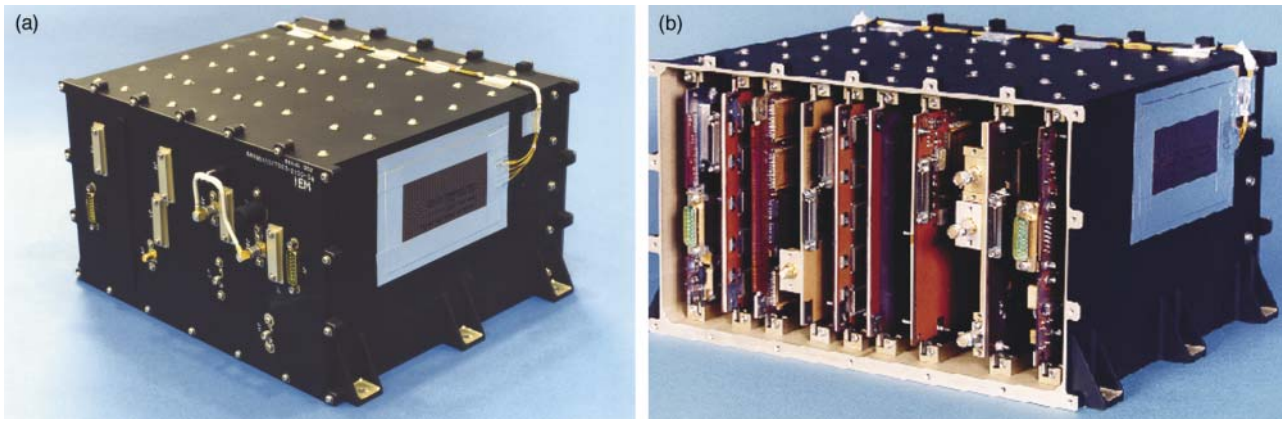

Figure 2. TIMED IEM flight unit with (a) and without (b) the front cover (size, 7.1 × 13 × 10.5 in.; weight, 25.2 lb; peak power consumption when the downlink power amplifier is on, 53.3 W).

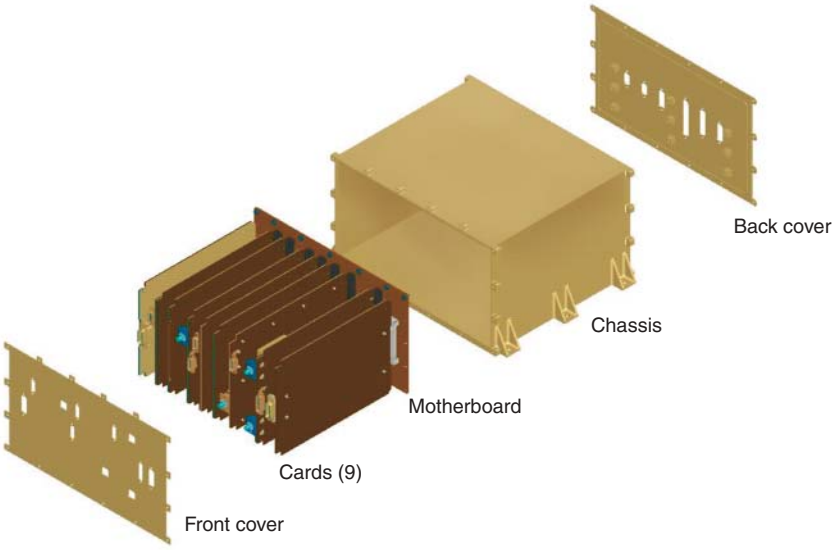

Figure 3. IEM construction.

interfaces with spacecraft subsystems external to the IEM. This extension is attached to the motherboard by a flexible section that allows folding the two parts back-to-back for a compact arrangement. Where needed, connectors at the top of a card provide for functions that are not practical to pass through the motherboard, i.e., RF signals, card test points, and main power.

Card construction is illustrated in Fig. 4, which shows digital and RF circuit elements. The core of a card is the aluminum structural member that also serves as a heat sink. Multilayer digital and RF boards or modules are mounted to the aluminum core either by a thermal bonding process or mechanically with threaded studs installed in the core. A 220-pin card-edge connector mates to the motherboard connector. Connectors for test points, RF signals, and spacecraft bus voltage inputs to the power conditioning subsystem are mounted on a card at the top edge.

The motherboard is configured with alternating ground and signal layers to reduce cross talk and to control signal path characteristics. DC power runs are removed from signal runs and are sized and duplicated to minimize voltage drop.

IEM DATA FLOW

The IEM has three data buses for communications within the TIMED spacecraft: 1553, peripheral component interface (PCI), and inter-integrated circuit (I^2C). The 1553 bus, an industry-standard serial, bidirectional bus, is redundant and is used to communicate with external subsystems, i.e., all instrument, power, and attitude control subsystems, and the other IEM. A modified version of the industry-standard PCI bus, which is bit-parallel and bidirectional, is used for communications within the IEM. The PCI is a 16-bit data bus, clocked at 2.5 MHz, and yields a peak data transfer rate of 5 Mbytes/s. The I^2C bus, also industry standard, is a serial bus used to gather temperature sensor readings from remote interface units (RIUs). The basic characteristics of each bus, as implemented for TIMED, are listed in Table 2.

The RIUs are external to the IEM and collect data from temperature sensors placed throughout the TIMED spacecraft. Each RIU handles 16 sensors. A multiplexer in the RIU time-samples each sensor, digitizes the voltage developed by each sensor, which is a nearly linear function of temperature, and supplies the results to the command and telemetry (C&T) interface card in the IEM via the I^2C bus.

TIMED C&T data are organized and encoded into packets in accordance with standards developed by the Consultative Committee for Space Data Systems (CCSDS). Protocols are established to ensure highly reliable end-to-end data delivery between the spacecraft and ground users. This includes confirmation of

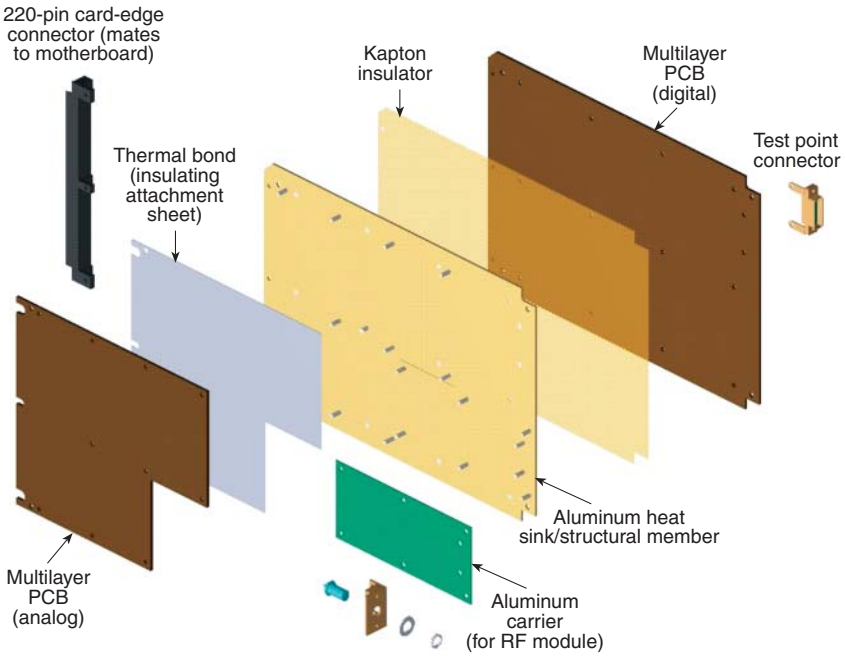

Figure 4. IEM card construction.

Table 2. IEM data bus characteristics.

Data bus	Data transfer (bit-parallel/serial)	Data rate (Mbits/s)	Use
1553	Serial (bidirectional)	1.0	Data transfer to/from subsystems external to IEM
PCI	16-bit parallel (bidirectional)	40.0	Data transfer within IEM
I^2C	Serial (unidirectional)	0.1	Transfer of digitized temperature data from RIUs to IEM

each command, tracking the receipt of each telemetry packet, and flagging detected errors.

IEM SUBSYSTEMS

Command and Data Handling

The C&DH subsystem is implemented on three cards—processor, solid-state recorder (SSR), and C&T interface. It also has elements on two other cards: a critical command decoder (CCD) on the uplink card and a downlink formatter on the downlink card, both part of the telecommunications subsystem.

The C&DH processor card contains a Mongoose V, a 32-bit RISC processor, memory, an ASIC (application-specific integrated circuit) 1553 bus controller (BC), and a PCI BC implemented in an FPGA (field-programmable gate array) with dedicated memory. The C&DH subsystem, which was developed on a PC running Windows NT, runs under the Nucleus Plus operating system. The major functions performed by the processor are to

- Deliver CCSDS telecommand packets (e.g., to instruments and power, attitude control, and navigation subsystems)
- Execute C&DH commands
- Provide spacecraft safing and autonomy
- Provide 1553 bus control (The redundant IEM is a 1553 remote terminal [RT]. Determination of which IEM is the RT is made by a relay state set by command.)
- Enable communication through the PCI bus master
- Provide peak power tracking processing for the power subsystem
- Collect telemetry data packets from instruments and subsystems
- Build instrument, subsystem status, and spacecraft housekeeping packets
- Record and downlink telemetry packets as defined by CCSDS
- Manage the SSR
- Support uploading of new code to flash memory
- Support storage of data structures (e.g., autonomy rules, command macros) to flash memory

The SSR card has a 2.5-Gbit capacity, sufficient for about 30 h of data accumulation at full spacecraft operation. Data are recorded in 244-byte Reed-Solomon (R-S) code blocks and can be stored and accessed randomly. The SSR card has simultaneous read and write capability at a combined rate of 8 Mbits/s. Memory scrubbing with 5-byte error correction and detection ensures data integrity. The card includes an FPGA PCI BC with dedicated memory through which all data and control functions are processed. The C&DH processor manages the SSR, which entails providing data for storage, directing where data are to be stored, and reading out stored data to the downlink.

The C&T card implements command, telemetry, and other data links between the C&DH processor and various entities within the IEM and TIMED spacecraft. Data flow to and from the C&DH processor is via the PCI bus. The special functions performed by the C&T card, which are listed below, are implemented with FPGA components.

- Route all uplink commands from the CCD on the IEM uplink card to the C&DH processor

- Route all relay commands generated by the C&DH processor to the CCD
- Collect temperature data from the RIUs via the I^2C bus and route to the C&DH processor
- Collect, digitize, and route internal IEM temperature and voltage data to the C&DH processor
- Collect and route "event" flags to the C&DH processor (e.g., RF time out, spacecraft separation from launch vehicle, attitude status indicators)
- Collect navigation experiment data from the uplink card and route to the C&DH processor
- Route commands from the C&DH processor to a navigation experiment on the uplink card
- Generate an IEM master reset in response to an uplink command detected by the CCD, at IEM power-on, or for specific errors detected by the C&DH processor

The core functions of the CCD on the uplink card, which are also implemented with an FPGA, are listed below.

- Receive commands from the uplink receiver and forward them to the C&T card for routing to the C&DH processor
- Detect relay commands from the uplink receiver that are labeled "Critical" and route these directly to the power-switching unit of the power subsystem (this allows bypassing the C&DH processor)
- Route C&DH processor–generated relay commands to the power-switching unit and notify the processor that each command has been sent (e.g., a relay command triggered by an autonomy rule)
- Reset the CCD and uplink receiver if a "watchdog" timer in the CCD times out. A time out occurs if an uplink command is not received within a set period. The timer is reset for each uplink command received. The C&DH processor is notified of a time-out event.
- Issue a sequence of a stored set of relay commands to the power-switching unit if a "hard" low-voltage condition is flagged by the power subsystem. The C&DH processor is notified and the command sequence implements an orderly power load reduction on the spacecraft.
- Decode and implement several of the internal CCD commands

The core functions of the CCD on the downlink formatter, implemented again with FPGAs, are to

- Gather real-time data from the C&DH processor and recorded data from the SSR, both via the PCI bus
- Organize the data into frames (real time and recorded)
- Perform R-T encoding
- Transfer the data bit serially to a modulator on the downlink card

GPS Navigation

The GPS Navigation subsystem (GNS) resides on two cards. One card contains a receiver consisting of an RF downconverter, an oscillator, a synthesizer, and a 12-channel GPS tracking ASIC (GTA) chip. An antenna is mounted on the spacecraft with a clear field of view to the GPS satellites. A low-noise amplifier, placed near the antenna to minimize signal losses, routes the signals from the GPS satellites in view to the RF downconverter. The downconverter translates the GPS signals from 1575.42 to 4.30 MHz in three steps. The frequency synthesizer on the card produces local oscillator signals used to accomplish the translation to 4.3 MHz. The oscillator provides the reference frequency for the synthesizer. Signals at 4.30 MHz are sampled and digitized. The digitized samples are transferred to the GTA, which provides acquisition and tracking of the GPS signals under control of a tracking processor on the second card. GTA output data are stored in memory on this card, which is accessed by the tracking processor.

The second GNS card contains two Mongoose V RISC processors, one for navigation, the other for acquiring and tracking GPS satellite signals. In addition to supporting the tracking function, the tracking processor also recovers the message subframes of each GPS satellite in track. Dual-port memory is used to pass data between the two processors. The "raw" tracking data and message subframes for each satellite are provided to the navigation processor. The navigation processor

- Computes the TIMED spacecraft position, velocity, and time (PVT)
  - Position uncertainty: <300 m, 3σ, each axis
  - Velocity uncertainty: <0.25 m, 3σ, each axis
  - Time to 100 μs UTC (Universal Time Coordinated), 3σ
- Estimates the spacecraft orbit parameters
- Computes the Earth–Sun vector
- Provides acquisition aids to the tracking processor
- Predicts events (e.g., ground station contact times)

The GNS provides a 1-s time mark, aligned to UTC, and an accompanying CCSDS unsegmented time code to the C&DH subsystem for spacecraft timekeeping. The navigation processor provides information to the tracking processor for maintaining the 1-s time mark aligned to UTC within 100 μs, 3σ.

Navigation data (i.e., PVT) and GNS status are provided to the C&DH system via the PCI bus every second. Commands and software updates are loaded to the GNS from the C&DH subsystem, also through the PCI bus. The GNS can be commanded to a mode that outputs "raw" tracking data in addition to the computed

navigation results for diagnostic purposes. Housekeeping telemetry points such as automatic gain control and input DC voltages are supplied to the C&T card of the C&DH subsystem for sampling, digitizing, and incorporation into spacecraft telemetry.

RF Telecommunications

As noted earlier, the electronics portion of the TIMED telecommunications subsystem comprises two cards in the IEM, uplink and downlink. Components of this subsystem external to the IEM are zenith- and nadir-facing antennas, antenna switching, and a diplexer that separates the uplink and downlink signals.

The uplink card contains a receiver for recovering the 2000 bits/s command information modulated on a 2039.65-MHz S-band carrier, using a 16-kHz subcarrier. The first operation of the receiver is to downconvert the S-band signal in two steps, first to 149.00 MHz and then to 15.30 MHz. A synthesizer on the card produces the local oscillator signals required for the two downconversions. A 30.60-MHz temperature-controlled crystal oscillator on the card is the reference frequency for the synthesizer. The receiver separates the main carrier and the 16-kHz subcarrier. A phase locked loop tracks the carrier to keep the receiver tuned to the uplink signal once acquisition is achieved. A command detector unit extracts the 2000 bits/s command data stream from the 16-kHz subcarrier. The command data stream is then routed to the CCD on the uplink card for further processing, as described previously in the C&DH section.

Major performance characteristics of the uplink are:

Acquisition threshold: −130 dBm
Noise figure: 4 dB
Dynamic range: 80 dB
Frequency tracking range: ±150 kHz about center frequency
Carrier tracking bandwidth: 400 Hz
Bit error rate: within 3 dB of theoretical at a probability of error = 1×10^{-6}
Link margin: 3 dB minimum

The downlink card modulates telemetry frames bit-serially onto a carrier at 2214.97 MHz. A power amplifier on the card boosts this signal to the transmitted power level. The amplified output is routed to the selected antenna and radiated for reception at an Earth station. A frequency synthesizer produces the carrier signal from the 30.60-MHz reference frequency provided from the downlink card. The downlink formatter on the downlink card assembles the telemetry frames.

Major performance characteristics of the downlink are:

RF output power: 3 W
Modulation format: differential quadraphase
Data rate: selectable, 4 Mbits/s (high rate) is usual
Link margin (at 4 Mbits/s): 12.2 dB, APL 60-ft antenna; 5.5 dB, 5-m antenna; 1.0 dB, 3-m antenna

Power Conditioning

Two cards in the IEM produce regulated, conditioned power from the spacecraft bus voltage (22–35 V) for operation of the IEM. One card supplies power for the C&DH and GNS and the other for the RF telecommunications subsystem. Power for the uplink card is from the spacecraft's "unswitched" bus; power for all other cards is from the "switched" bus.

Standard off-the-shelf, high-reliability DC/DC converter modules are used to produce the various regulated voltages required for the IEM cards. Custom circuitry is added on the cards to meet the following special requirements for the IEM:

- Provide inrush current control to meet electromagnetic compatibility specifications
- Provide low input voltage lockout protection
- Produce "power-on" reset to initialize subsystem
- Turn on power to the downlink power amplifier in a defined sequence
- Add circuits to provide +9.0 V used by the downlink power amplifier and +3.3 V used by the SSR

SUBSYSTEM DEVELOPMENT, INTEGRATION, AND TEST

Each subsystem was implemented separately using a development motherboard or, in the case of the C&DH subsystem, a wire-wrapped version of the motherboard interconnects. The interfaces to the other subsystems were emulated by various means to form a complete testbed for each subsystem. For the GNS, testbeds were produced for software and hardware development. This approach is directly analogous to the subsystem development process used for box-and-harness spacecraft configurations. Testbeds were implemented for card-level development as well.

The basic card design was qualified by a series of thermal and mechanical tests on a sample card that incorporated all of the assembly features of the various card configurations. Each flight card was subjected to a series of thermal shock and thermal cycling tests, with performance tests before and after the cycling. Each integrated subsystem was then thermally tested before acceptance for IEM integration.

At the IEM level, each subsystem was integrated into the chassis in an ordered sequence. First the motherboard was thoroughly checked to ensure that all connections were correct. Then the power subsystem was installed and checked to ensure that the correct voltages were supplied to each subsystem card as required. The C&DH subsystem was installed next and checked. An IEM

testbed that emulated the spacecraft data interfaces to the IEM was used at this point to provide a means of exercising the C&DH subsystem operations with other spacecraft subsystems. Ground support equipment (GSE), used to recover telemetry and generate commands, was interfaced through a baseband link to the C&DH. This arrangement of IEM testbed and GSE allowed end-to-end testing of the C&DH subsystem. The RF telecommunications subsystem was installed next. RF GSE linked to the other GSE was used to test this subsystem. Finally, the GNS was integrated into the IEM. A GPS satellite simulator was used to realistically test this subsystem.

An engineering-model IEM was fabricated and used to demonstrate the compatibility of the concept, work out any manufacturing problems, support flight software development, and exercise test procedures for flight IEM testing. It was also used for early integration of the spacecraft to verify interfaces and check the simultaneous operation of two IEMs when only one flight unit was available.

Before delivery for spacecraft integration, each flight IEM was subjected to environmental testing consisting of sine and random vibration and thermal vacuum (six thermal cycles in vacuum) testing. Performance and functional testing was conducted throughout these tests, and electromagnetic compatibility testing was performed on the first flight unit.

SUMMARY

The IEM concept was to incorporate multiple spacecraft subsystems into a singe chassis, thereby conserving critical spacecraft resources at a reduced cost. The IEM was implemented on TIMED including C&DH, GNS, RF telecommunications, and IEM power conditioning. The module underwent construction, subsystem development, and integration and testing. Since the launch of TIMED on 7 December 2001, the IEM has operated flawlessly, providing in-flight validation of the IEM concept.

REFERENCE AND NOTE

[1]Fraeman, M., Hersman, C., et al., *JHU/APL Space Department Advanced Satellite Technology Committee Integrated Electronics Module Subcommittee Final Report*, S2R-95-225, JHU/APL, Laurel, MD (19 Dec 1995).

[2]CONTOUR = COmet Nucleus TOUR; MESSENGER = MErcury Surface, Space ENvironment, GEochemistry, and Ranging; STEREO = Solar TErrestrial Relations Obseratory.

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