SUBSYSTEM ELECTRICAL

INTERFACE CONTROL DOCUMENT

FOR THE

GLOBAL ULTRAVIOLET IMAGER

(GUVI)

FLIGHT INSTRUMENT

7366-9020

Revision: c

June 12, 1998

Table of Contents

1. Scope 3
2. Interface Signal Definitions 3
   2.1 SIS Electronics 3
   2.2 FPE 7
   2.3 HVPS 7
   2.4 ECU Boards 8
3. SIS External Interface Connectors 11
   3.1 SIS Electronics Drive 11
   3.2 SIS Electronics Monitor 12
   3.3 SIS Housing Pyro 13
   3.4 SIS Housing Survival Heater Power 14
   3.5 SIS Housing Operational Heater Power 14
   3.6 SIS Housing Temperature Sensor #1 14
   3.7 SIS Housing Temperature Sensor #2 15
4. Detector External Interface Connectors 15
   4.1 FPE #1 Power 15
   4.2 HVPS #1 Power 15
   4.3 FPE #2 Power 16
   4.4 HVPS #2 Power 17
5. ECU External Interface Connectors 17
   5.1 Main Power 17
   5.2 1553 Bus A 18
   5.3 1553 Bus B 18
   5.4 SIS Electronics I/O 18
   5.5 SIS Power 20
   5.6 Detector #1 Power 21
   5.7 Detector #2 Power 21
6. ECU Backplane Connectors 22

1. Scope

This document defines the subsystem electrical interfaces for the Global Ultraviolet Imager (GUVI) flight instrument. The GUVI subsystem packages include the SIS Housing, SIS Electronics, Focal Plane Electronics (FPE) #1 and #2, High Voltage Power Supply (HVPS) #1 and #2, and the Electronics Control Unit (ECU). The document defines the electrical interface signals, and lists the connector pin assignments for all subsystem external connectors and the Electronics Control Unit backplane connectors.

2. Interface Signal Definitions

2.1 SIS Electronics

2.1.1 Scan Motor Primary Drive Phase 1 - 4

The scan motor primary drive signals activate the four scan motor windings with the primary motor drive circuitry. The signal level is +5 Volt CMOS. Logic level 0 indicates the motor winding is off, logic level 1 indicates the motor winding is activated. The signal source is the ECU I/O board.

2.1.2 Scan Motor Secondary Drive Phase 1 - 4

The scan motor secondary drive signals activate the four scan motor windings with the secondary motor drive circuitry. The signal level is +5 Volt CMOS. Logic level 0 indicates the motor winding is off, logic level 1 indicates the motor winding is activated. The signal source is the ECU I/O board.

2.1.3 Scan Motor Primary Drive Select

Scan motor primary drive select is a pulse command that switches the scan motor drive select latching relay to the primary drive position. The signal level is +5 Volt CMOS. Logic level 0 indicates the relay coil is off, logic level 1 indicates the relay coil is activated. The select signal shall remain at the logic 1 level for 500 milliseconds. The signal source is the ECU I/O board.

2.1.4 Scan Motor Secondary Drive Select

Scan motor secondary drive select is a pulse command that switches the scan motor drive select latching relay to the secondary drive position. The signal level is +5 Volt CMOS. Logic level 0 indicates the relay coil is off, logic level 1 indicates the relay coil is activated. The select signal shall remain at the logic 1 level for 500 milliseconds. The signal source is the ECU I/O board.

2.1.5 Scan Motor Current Monitor

The scan motor current monitor is an analog signal that indicates the scan motor current. The signal range is 0 to +5 Volts. The current monitor scale factor is 100 mA per Volt. The signal destination is the ECU I/O board.

2.1.6 Narrow Slit In/Out Primary Drive

Narrow slit in primary drive is a pulse command that switches the narrow slit mechanism to the in position using the primary drive circuitry. Narrow slit out primary drive is a pulse command that switches the narrow slit mechanism to the out position using the primary drive circuitry. The signal level is +5 Volt CMOS. Logic level 0 indicates the slit motor is off, logic level 1 indicates the slit motor is activated. The signal shall remain at the logic 1 level for 500 milliseconds. The signal source is the ECU I/O board.

2.1.7 Medium Slit In/Out Primary Drive

Medium slit in primary drive is a pulse command that switches the medium slit mechanism to the in position using the primary drive circuitry. Medium slit out primary drive is a pulse command that switches the medium slit mechanism to the out position using the primary drive circuitry. The signal level is +5 Volt CMOS. Logic level 0 indicates the slit motor is off, logic level 1 indicates the slit motor is activated. The signal shall remain at the logic 1 level for 500 milliseconds. The signal source is the ECU I/O board.

2.1.8 Narrow Slit In/Out Secondary Drive

Narrow slit in secondary drive is a pulse command that switches the narrow slit mechanism to the in position using the secondary drive circuitry. Narrow slit out secondary drive is a pulse command that switches the narrow slit mechanism to the out position using the secondary drive circuitry. The signal level is +5 Volt CMOS. Logic level 0 indicates the slit motor is off, logic level 1 indicates the slit motor is activated. The signal shall remain at the logic 1 level for 500 milliseconds. The signal source is the ECU I/O board.

2.1.9 Medium Slit In/Out Secondary Drive

Medium slit in secondary drive is a pulse command that switches the medium slit mechanism to the in position using the secondary drive circuitry. Medium slit out secondary drive is a pulse command that switches the medium slit mechanism to the out position using the secondary drive circuitry. The signal level is +5 Volt CMOS. Logic level 0 indicates the slit motor is off, logic level 1 indicates the slit motor is activated. The signal shall remain at the logic 1 level for 500 milliseconds. The signal source is the ECU I/O board.

2.1.10 Pop-up In/Out

Pop-up in is a pulse command that switches the pop-up mirror mechanism to the in position (backup detector position). Pop-up out is a pulse command that switches the pop-up mirror mechanism to the out position (primary detector position). The signal level is +5 Volt CMOS. Logic level 0 indicates the pop-up motor is off, logic level 1 indicates the pop-up motor is activated. The signal shall remain at the logic 1 level for 500 milliseconds. The signal source is the ECU I/O board.

2.1.11 Drive Board Temp

The drive board temperature signal is the temperature monitor for the SIS Electronics package. The drive board temp pos and neg pins are connected to an AD590 temperature sensor mounted on the SIS Electronics drive board. The temperature sensor bias circuitry will be located on the ECU I/O board. The signal destination is the ECU I/O board.

2.1.12 Cover Closed Telltale

The cover closed telltale signal indicates when the SIS cover is in the closed position. The signal level is +5 Volt CMOS. Logic level 0 indicates the cover is closed, logic level 1 indicates the cover is not closed. The signal destination is the ECU I/O board.

2.1.13 Cover Full Open Telltale

The cover full open telltale signal indicates when the SIS cover is in the full open position. The signal level is +5 Volt CMOS. Logic level 0 indicates the cover is full open, logic level 1 indicates the cover is not full open. The signal destination is the ECU I/O board.

2.1.14 Narrow Slit In Telltale

The narrow slit in telltale signal indicates when the narrow slit mechanism is in the optical path. The signal level is +5 Volt CMOS. Logic level 0 indicates the slit is in the optical path, logic level 1 indicates the slit is not in the optical path. The signal destination is the ECU I/O board.

2.1.15 Narrow Slit Out Telltale

The narrow slit out telltale signal indicates when the narrow slit mechanism is out of the optical path. The signal level is +5 Volt CMOS. Logic level 0

indicates the slit is out of the optical path, logic level 1 indicates the slit is not out of the optical path. The signal destination is the ECU I/O board.

2.1.16 Medium Slit In Telltale

The medium slit in telltale signal indicates when the medium slit mechanism is in the optical path. The signal level is +5 Volt CMOS. Logic level 0 indicates the slit is in the optical path, logic level 1 indicates the slit is not in the optical path. The signal destination is the ECU I/O board.

2.1.17 Medium Slit Out Telltale

The medium slit out telltale signal indicates when the medium slit mechanism is out of the optical path. The signal level is +5 Volt CMOS. Logic level 0 indicates the slit is out of the optical path, logic level 1 indicates the slit is not out of the optical path. The signal destination is the ECU I/O board.

2.1.18 Pop-up Out Telltale

The pop-up out telltale signal indicates when the pop-up mirror is out of the optical path (primary detector position). The signal level is +5 Volt CMOS. Logic level 0 indicates the pop-up mirror is in the out position, logic level 1 indicates the pop-up mirror is not in the out position. The signal destination is the ECU I/O board.

2.1.19 Start Position Indicator

The start position indicator is a digital signal that indicates when the scan motor is at the start of scan position. The signal level is +5 Volt CMOS. Logic level 0 indicates the motor is not at the start position, logic level 1 indicates the motor is at the start position. The signal destination is the ECU I/O board.

2.1.20 Nadir Position Indicator

The nadir position indicator is a digital signal that indicates when the scan motor is at the nadir position. The signal level is +5 Volt CMOS. Logic level 0 indicates the motor is not at the nadir position, logic level 1 indicates the motor is at the nadir position. The signal destination is the ECU I/O board.

2.1.21 Scan Mirror Temp

The scan mirror temperature signal is the temperature monitor for the SIS scan mirror. The scan mirror temp pos and neg pins are connected to an AD590 temperature sensor mounted on the back of the scan mirror. The temperature sensor bias

circuitry will be located on the ECU I/O board. The signal destination is the ECU I/O board.

2.1.22 SIS Housing Temp

The SIS housing temperature signal is the temperature monitor for the SIS housing. The SIS housing temp pos and neg pins are connected to an AD590 temperature sensor mounted on the SIS housing near the purge connector. The temperature sensor bias circuitry will be located on the ECU I/O board. The signal destination is the ECU I/O board.

2.2 FPE

2.2.1 FPE Temp

The FPE temperature signal is the temperature monitor for the FPE package. The FPE temp pos and neg pins are connected to an AD590 temperature sensor mounted in the FPE package. The temperature sensor bias circuitry will be located on the ECU I/O board. The signal destination is the ECU I/O board.

2.3 HVPS

2.3.1 HV Control

The HV control signal adjusts the output voltage level of the high voltage power supply. HV control is an analog signal that ranges from 0 to +6 Volts. It shall be adjustable in steps of 0.025 Volts or less. The high voltage output level will be 1000 times the HV control signal voltage. The signal source is the ECU I/O board.

2.3.2 HV Monitor

The HV monitor signal is the high voltage power supply output voltage monitor. HV monitor is an analog signal that ranges from 0 to +6 Volts. The HV monitor level will be the high voltage output level divided by 1000. The signal destination is the ECU I/O board.

2.3.3 HV Temp

The HV temperature signal is the temperature monitor for the HVPS package. The HV temp pos and neg pins are connected to an AD590 temperature sensor in the HVPS package. The temperature sensor bias circuitry will be located on the ECU I/O board. The signal destination is the ECU I/O board.

2.4 ECU Boards

2.4.1 Telemetry Processor to Detector Processor Interface

2.4.1.1 Detector Processor Input D0 - D15

The detector processor input bus (DPU_IN) is used to transfer data from the telemetry processor to the detector processor. The bus size is 16 bits. The MSB is bit 15 (DPU_IN_D15), the LSB is bit 0 (DPU_IN_D0). The signal level is +5 Volt CMOS. The average transfer rate shall be greater than 1 word per 50 microseconds. A timing diagram for telemetry processor to detector processor data transfers is shown in figure 1.

2.4.1.2 Telemetry Processor Data Ready

The telemetry processor data ready signal (TLM_DTR) indicates to the detector processor that a data word is available on the input bus. The input ready signal is set to logic level 1 when the telemetry processor writes to the input bus, and is reset to logic level 0 when the bus is read. The signal level is +5 Volt CMOS.

2.4.1.3 Detector Processor Data Acknowledge

The detector processor data acknowledge signal (DPU_DTACK) indicates to the telemetry processor that the input bus has been read. The data acknowledge signal is set to logic level 1 when the detector processor reads the input bus, and is reset to logic level 0 when the telemetry processor writes data to the bus. The signal level is +5 Volt CMOS.

2.4.1.4 Detector Processor Output D0 - D15

The detector processor output bus (DPU_OUT) is used to transfer data from the detector processor to the telemetry processor. The bus size is 16 bits. The MSB is bit 15 (DPU_OUT_D15), the LSB is bit 0 (DPU_OUT_D0). The signal level is +5 Volt CMOS. The average transfer rate shall be greater than 1 word per 50 microseconds. A timing diagram for detector processor to telemetry processor data transfers is shown in figure 2.

2.4.1.5 Detector Processor Data Ready

The detector processor data ready signal (DPU_DTR) indicates to the telemetry processor that a data word is available on the output bus. The data ready signal is set to logic level 1 when the detector processor writes to the output bus, and is reset to logic level 0 when the bus is read. The signal level is +5 Volt CMOS.

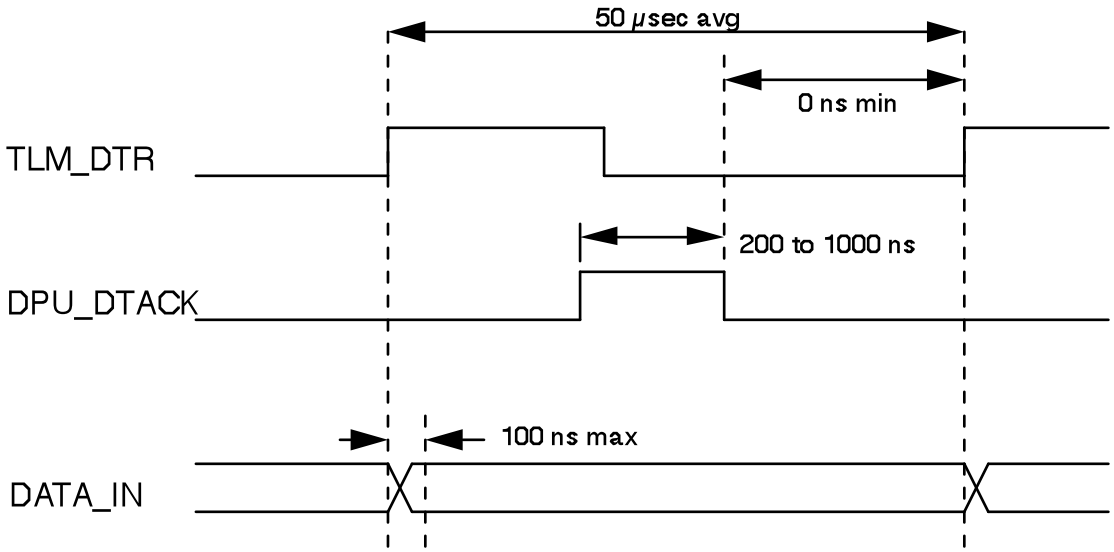
2.4.1.6 Telemetry Processor Data Acknowledge

The telemetry processor data acknowledge signal (TLM_DTACK) indicates to the detector processor that the output bus has been read. The data acknowledge signal is set to logic level 1 when the telemetry processor reads the output bus, and is reset to logic level 0 when the detector processor writes data to the bus. The signal level is +5 Volt CMOS.

2.4.1.7 Detector Processor Reset

The detector processor reset (DPU RESET) is a pulse signal to reset the microprocessor on the detector processor board. Logic level 1 indicates a reset state, logic level 0 indicates normal processor operation. The signal level is +5 Volt CMOS. The signal pulse width shall be a minimum of 1.0 microseconds.

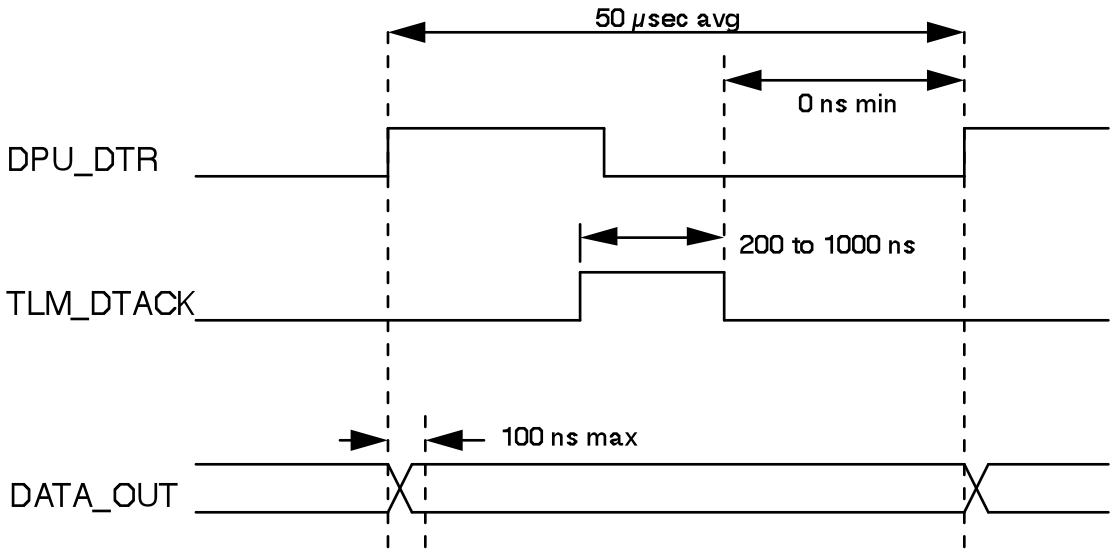
Figure 1 - Telemetry Processor to Detector Processor Data Transfer Timing



TLM_DTR to DATA_IN Valid =	100 nsec max
DPU_DTACK Pulse Width =	200 nsec min 1000 nsec max
De-assert of DPU_DTACK to	

TLM_DTR Active =	0 nsec min
Cycle Period =	50 μsec avg

Figure 2 - Detector Processor to Telemetry Processor Data Transfer Timing



DPU_DTR to DATA_OUT Valid =	100 nsec max
TLM_DTACK Pulse Width =	200 nsec min 1000 nsec max
De-assert of TLM_DTACK to DPU_DTR Active =	0 nsec min
Cycle Period =	50 μsec avg

2.4.2 Power Converter Boards

2.4.2.1 Detector #1 Power Control

Detector #1 power control (FPE1 CTRL) is a level signal that switches the detector #1 power converters on and off. The signal level is +5 Volt CMOS. Logic level 1 indicates the detector power is off, logic level 0 indicates the detector power is on. The signal minimum drive current shall be 250 microamps. The signal source is the ECU I/O board.

2.4.2.2 Detector #2 Power Control

Detector #2 power control (FPE2 CTRL) is a level signal that switches the detector #2 power converters on and off. The signal level is +5 Volt CMOS. Logic level 1 indicates the detector power is off, logic level 0 indicates the detector power is on. The signal minimum drive current shall be 250 microamps. The signal source is the ECU I/O board.

2.4.2.3 Scan Mirror Heater Control

Scan mirror heater control (SIS_MHTR_CTRL) is a level signal that switches the scan mirror heater power relay on and off. The signal level is +5 Volt CMOS. Logic level 1 indicates the heater power is off, logic level 0 indicates the heater power is on. The signal minimum drive current shall be 16 milliamps. The signal source is the ECU I/O board.

2.4.2.4 Detector #1 Power Status

The detector #1 power status signal indicates the on/off state of the detector #1 power converters. The signal level is +5 Volt CMOS. Logic level 0 indicates the detector power is off, logic level 1 indicates the detector power is on. The signal destination is the ECU I/O board.

2.4.2.5 Detector #2 Power Status

The detector #2 power status signal indicates the on/off state of the detector #2 power converters. The signal level is +5 Volt CMOS. Logic level 0 indicates the detector power is off, logic level 1 indicates the detector power is on. The signal destination is the ECU I/O board.

3. SIS External Interface Connectors

3.1 SIS Electronics Drive

A605-J01 Drive Board
Type: 50 Pin D Female

Pin	Signal	Pin	Signal
1	NAR SLIT OUT PRI	34	MED SLIT IN SEC
2	POP UP OUT	35	MED SLIT OUT SEC
3	SCAN MTR PRI PH3	36	MED SLIT OUT PRI
4	NAR SLIT IN SEC	37	MED SLIT IN PRI
5	SCAN MTR PRI PH4	38	SIS +5V RTN (NC)
6	NAR SLIT OUT SEC	39	SIS +20V RTN
7	NAR SLIT IN PRI	40	
8	SCAN MTR SEC SEL	41	
9	SCAN MTR PRI SEL	42	
10	SCAN MTR SEC PH4	43	KEY
11	SCAN MTR SEC PH2	44	
12	SCAN MTR SEC PH1	45	
13	SCAN MTR CUR MON	46	
14	SCAN MTR PRI PH2	47	
15	SCAN MTR PRI PH1	48	
16	SIS +20V PWR	49	DRIVE BD TEMP POS
17	SIS +5V PWR	50	DRIVE BD TEMP NEG
18	SIGNAL GND		
19	SIGNAL GND		
20	POP UP IN		
21			
22	SIS +5V RTN		
23	SIS +20V RTN		
24			
25			
26			
27	SCAN MTR SEC PH3		
28			
29			
30			
31			
32	SIS +20V PWR		
33	SIS +5V PWR (NC)		

3.2 SIS Electronics Monitor

A605-J02 Monitor Board
Type: 50 Pin D Female

Pin	Signal	Pin	Signal
1	START POS	34	NAR SLIT OUT TT

2	NADIR POS	35	MED SLIT OUT TT
3		36	START TEST PT (NC)
4	SIS +5V PWR	37	
5	SIS +5V PWR (NC)	38	
6	SIGNAL GND	39	NADIR TEST PT (NC)
7	SIS +5V RTN	40	KEY
8	SIGNAL GND	41	
9	SIS +5V RTN (NC)	42	SIS +20V PWR (NC)
10		43	SIS +20V RTN (NC)
11		44	SCAN MIRR TEMP NEG
12	SIGNAL GND	45	
13		46	
14		47	
15		48	
16		49	SIS DET TEMP POS
17		50	SIS DET TEMP NEG
18	COVER CLOSED TT		
19	COVER FULL OPEN TT		
20	NAR SLIT IN TT		
21	MED SLIT IN TT		
22	POP UP OUT TT		
23			
24			
25			
26			
27			
28			
29			
30			
31	SIS MIRR HTR PWR		
32	SIS MIRR HTR RTN		
33	SCAN MIRR TEMP POS		

3.3 SIS Housing Pyro

A600-J01 SIS Pyro
Type: D-SUBMINIATURE 9-PIN MALE
311P409-1P-B-15

Pin	Signal Name
1	Pyro #1 Power
2	Pyro #1 Return

3	NC
4	Pyro #2 Power
5	Pyro #2 Return
6	Pyro #1 Shield
7	Key
8	NC
9	Pyro #2 Shield

3.4 SIS Housing Survival Heater Power

A600-J02 Survival Heater Power
Type: 4-PIN Winchester JF2P-2S-AB

Pin	Signal Name
A	Survival Heater Power
B	Survival Heater Power
C	Survival Heater Return
D	Survival Heater Return

3.5 SIS Housing Operational Heater Power

A600-J05 Operational Heater Power
Type: 4-PIN Winchester JF2P-2S-AB

Pin	Signal Name
A	Operational Heater Power
B	Operational Heater Power
C	Operational Heater Return
D	Operational Heater Return

3.6 SIS Housing Temperature Sensor #1

A600-J03 Temperature Sensor #1
Type: 4-PIN Winchester JF2S-2P-AB
Temp: SIS Housing

Pin	Signal Name
A	Temp #1 PRI POS
B	Temp #1 SEC POS
C	Temp #1 PRI NEG
D	Temp #1 SEC NEG

3.7 SIS Housing Temperature Sensor #2

A600-J04 Temperature Sensor #2
Type: 4-PIN Winchester JF2S-2P-AB
Temp: SIS Scan Motor

Pin	Signal Name
A	Temp #2 PRI POS
B	Temp #2 SEC POS
C	Temp #2 PRI NEG
D	Temp #2 SEC NEG

4. Detector External Interface Connectors

4.1 FPE #1 Power

A610-J12 FPE #1 Power
Type: 15 Pin D Male

Pin	Signal
1	FPE1 +6V PWR
2	FPE1 +6V PWR
3	FPE1 -6V PWR
4	FPE1 -6V PWR
5	
6	
7	FPE1 TEMP POS
8	FPE1 TEMP NEG
9	FPE1 +6V RTN
10	FPE1 +6V RTN
11	FPE1 -6V RTN
12	FPE1 -6V RTN
13	
14	
15	CHASSIS GND (NC)

4.2 HVPS #1 Power

A620-J01 HVPS #1 Power

Type: 15 Pin D Female

Pin	Signal
1	HVPS1 +28V PWR
2	HVPS1 +28V PWR
3	
4	HV1 CONTROL
5	
6	KEY
7	HVPS1 TEMP POS
8	HV1 MONITOR
9	HVPS1 +28V RTN
10	HVPS1 +28V RTN
11	HV1 CONTROL RTN
12	
13	CHASSIS GND
14	HVPS1 TEMP NEG
15	HV1 MONITOR RTN

4.3 FPE #2 Power

A612-J12 FPE #2 Power
Type: 15 Pin D Male

Pin	Signal
1	FPE2 +6V PWR
2	FPE2 +6V PWR
3	FPE2 -6V PWR
4	FPE2 -6V PWR
5	
6	
7	FPE2 TEMP POS
8	FPE2 TEMP NEG
9	FPE2 +6V RTN
10	FPE2 +6V RTN
11	FPE2 -6V RTN
12	FPE2 -6V RTN
13	
14	
15	CHASSIS GND (NC)

4.4 HVPS #2 Power

A622-J01 HVPS #2 Power
Type: 15 Pin D Female

Pin	Signal
1	HVPS2 +28V PWR
2	HVPS2 +28V PWR
3	
4	HV2 CONTROL
5	KEY
6	
7	HVPS2 TEMP POS
8	HV2 MONITOR
9	HVPS2 +28V RTN
10	HVPS2 +28V RTN
11	HV2 CONTROL RTN
12	
13	CHASSIS GND
14	HVPS2 TEMP NEG
15	HV2 MONITOR RTN

5. ECU External Interface Connectors

5.1 Main Power

A625-J15 Main Power
Type: D-SUBMINIATURE 15-PIN MALE

Pin	Signal Name
1	NC
2	+28V Power
3	+28V Power
4	NC
5	NC
6	NC
7	NC
8	Chassis Ground
9	+28V Return
10	+28V Return
11	NC
12	Key
13	NC

14	NC
15	NC

5.2 1553 Bus A

A625-J12 1553 Bus A
Type: D-SUBMINIATURE 9-PIN FEMALE
DEMM9SD-NMB-K52

Pin	Signal Name
1	1553 A Signal
2	NC
3	NC
4	NC
5	NC
6	1553 A Return
7	NC
8	NC
9	NC

5.3 1553 Bus B

A625-J13 1553 Bus B
Type: D-SUBMINIATURE 9-PIN FEMALE
DEMM9SD-NMB-K52

Pin	Signal Name
1	1553 B Signal
2	NC
3	NC
4	NC
5	NC
6	1553 B Return
7	NC
8	NC
9	NC

5.4 SIS Electronics I/O

A625-J11 SIS Electronics I/O
Type: 50 Pin D Male

Pin	Signal Name
1	GROUND
34	GROUND
18	SCAN_MTR_PRIM_PH1
2	SCAN_MTR_PRIM_PH2
35	SCAN_MTR_PRIM_PH3
19	SCAN_MTR_PRIM_PH4
3	SCAN_MTR_SEC_PH1
36	SCAN_MTR_SEC_PH2
20	SCAN_MTR_SEC_PH3
4	SCAN_MTR_SEC_PH4
37	SCAN_MTR_PRIM_SEL
21	SCAN_MTR_SEC_SEL
5	SCAN_MTR_CUR_MON
38	GROUND
22	NAR_SLIT_IN_PRIM
6	NAR_SLIT_OUT_PRIM
39	MED_SLIT_IN_PRIM
23	MED_SLIT_OUT_PRIM
7	NAR_SLIT_IN_SEC
40	NAR_SLIT_OUT_SEC
24	MED_SLIT_IN_SEC
8	MED_SLIT_OUT_SEC
41	POP_UP_IN
25	POP_UP_OUT
9	DRIVE_BD_TEMP_P
42	DRIVE_BD_TEMP_N
26	GROUND
10	GROUND
43	CVR_CLOSED_TT
27	CVR_FOPEN_TT
11	NAR_SLIT_IN_TT
44	NAR_SLIT_OUT_TT
28	MED_SLIT_IN_TT
12	MED_SLIT_OUT_TT
45	POP_UP_OUT_TT
29	
13	START_POS
46	NADIR_POS
30	SCAN_MIROR_TEMP_P
14	SCAN_MIROR_TEMP_N
47	SIS_DET_TEMP_P
31	SIS_DET_TEMP_N
15	GROUND

48	GROUND

Pin	Signal Name
32	NC
16	NC
49	NC
33	NC
17	NC
50	KEY

5.5 SIS Power

A625-J11 SIS Power
Type: 25 Pin D Female

Pin	Signal Name
1	GROUND
14	GROUND
2	SIS_+5V
15	SIS_+5V
3	SIS_20V_RET
16	SIS_20V_RET
4	SIS_+20V
17	SIS_+20V
5	SIS_20V_RET
18	SIS_20V_RET
6	NC
19	NC
7	NC
20	NC
8	SIS_20V_RET
21	SIS_20V_RET
9	SIS_MIROR_HTR_PWR
22	SIS_MIROR_HTR_PWR
10	SIS_MIROR_HTR_RET
23	SIS_MIROR_HTR_RET
11	NC
24	NC
12	NC
25	KEY
13	NC

5.6 Detector #1 Power

A625-J17 Detector #1 Power
Type: 25 Pin D Female

Pin	Signal Name
1	KEY
14	HVPS1_+28V
2	HVPS1_+28V
15	HVPS1_+28V_RET
3	HVPS1_+28V_RET
16	CHASSIS_GND
4	CHASSIS_GND
17	NC
5	NC
18	HV1_CTRL
6	HV1_CTRL_RET
19	HV1_MON
7	HV1_MON_RET
20	HVPS1_TEMP_P
8	HVPS1_TEMP_N
21	FPE1_+6V
9	FPE1_+6V
22	FPE1_+6V_RET
10	FPE1_+6V_RET
23	FPE1_-6V
11	FPE1_-6V
24	FPE1_-6V_RET
12	FPE1_-6V_RET
25	FPE1_TEMP_P
13	FPE1_TEMP_N

5.7 Detector #2 Power

A625-J18 Detector #2 Power
Type: 25 Pin D Female

Pin	Signal Name
1	HVPS2_+28V
14	HVPS2_+28V
2	HVPS2_+28V_RET
15	HVPS2_+28V_RET
3	CHASSIS_GND

16	CHASSIS_GND
4	NC
17	NC
5	HV2_CTRL
18	HV2_CTRL_RET
6	HV2_MON
19	HV2_MON_RET
7	HVPS2_TEMP_P
20	HVPS2_TEMP_N
8	FPE2_+6V
21	FPE2_+6V
9	FPE2_+6V_RET
22	FPE2_+6V_RET
10	FPE2_-6V
23	FPE2_-6V
11	FPE2_-6V_RET
24	FPE2_-6V_RET
12	FPE2_TEMP_P
25	FPE2_TEMP_N
13	KEY

6. ECU Backplane Connectors

(see enclosed spreadsheets)