Solar Imager Radio Array (SIRA)

Command and Data Handling System

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Competition Sensitive

Overview

- **1 Single String Integrated Avionics Box**
  - Performs C&DH and ACS Data Processing
  - Precision Timing System
  - Embedded Attitude Control Electronics and Valve Drive Electronics
  - 20 Gbits (2 days) data storage capacity

Driving Requirements

• Launch Date:	2009
• Mission Life:	2 years required, 4 year goal
• Orbit:	Distant Retrograde Orbit
	Altitude 500,000 km, 20^{o} Inclination
• Constellation:	16 Microsats in sphere
• Attitude Control:	3-Axis Stabilized
• Data Storage Duration:	2 days
• Downlink Rate:	8 Mbps
• Downlink Contact Time per Spacecraft:	25 minutes / day
• Data Communication Protocol:	CCSDS
• Processing:	C&DH and ACS
• Absolute Timing Accuracy:	1 ms
• Relative Timing Accuracy between each s/c:	1 us
• Ranging:	Knowledge to 3 m
• Constraints:	Cost

Data Storage Analysis

Science data storage reverse engineered from downlink rate and time.

8 Mbps x 25 minutes = 12 Gbits with 15% CCSDS overhead
= 10 Gbits with no overhead

User Data Storage = 10 Gbits x 2 days = 20 Gbits
Actual Data Storage (20% EDAC Overhead) = 24 Gbits

Science data acquisition rate reverse engineered from data storage

10 Gbits / 24 hours = 120 kbps (original customer wish was 220 kbps)

May want to consider collecting data from fewer spacecraft and increasing the science data rate per spacecraft

For Example: 10 spacecraft would allow a science data rate of 185 kbps

Also consider a second ground station

Timing Analysis

- 1 us relative timing requirement requires a 1 Mbps timing broadcast signal
- 1 Mbps timing signal provides 1 us bit sync resolution
- 3 spacecraft will have the capability to transmit the timing broadcast signal
- Timing broadcast signal will be modulated on VHF carrier
- Timing broadcast signal will provide time sync bit plus actual time
- To maintain 1 us timing accuracy with cheap clocks (25×10^{-6} drift rate), timing sync command needs to be transmitted at about 25 Hz rate across timing broadcast signal (phase-locked loop)
- Each spacecraft calculates propagation delay error using orbit knowledge and adjusts spacecraft time accordingly

- A trade study was performed using an Ultra Stable Oscillator that only required the timing broadcast signal to be transmitted about once per day. That option was rejected due to cost of the Ultra Stable Oscillators (USO).
  - USO mass: 2 kg
  - USO power: 4 watts
  - USO drift: 1×10^{-11}
  - USO Cost: $250k

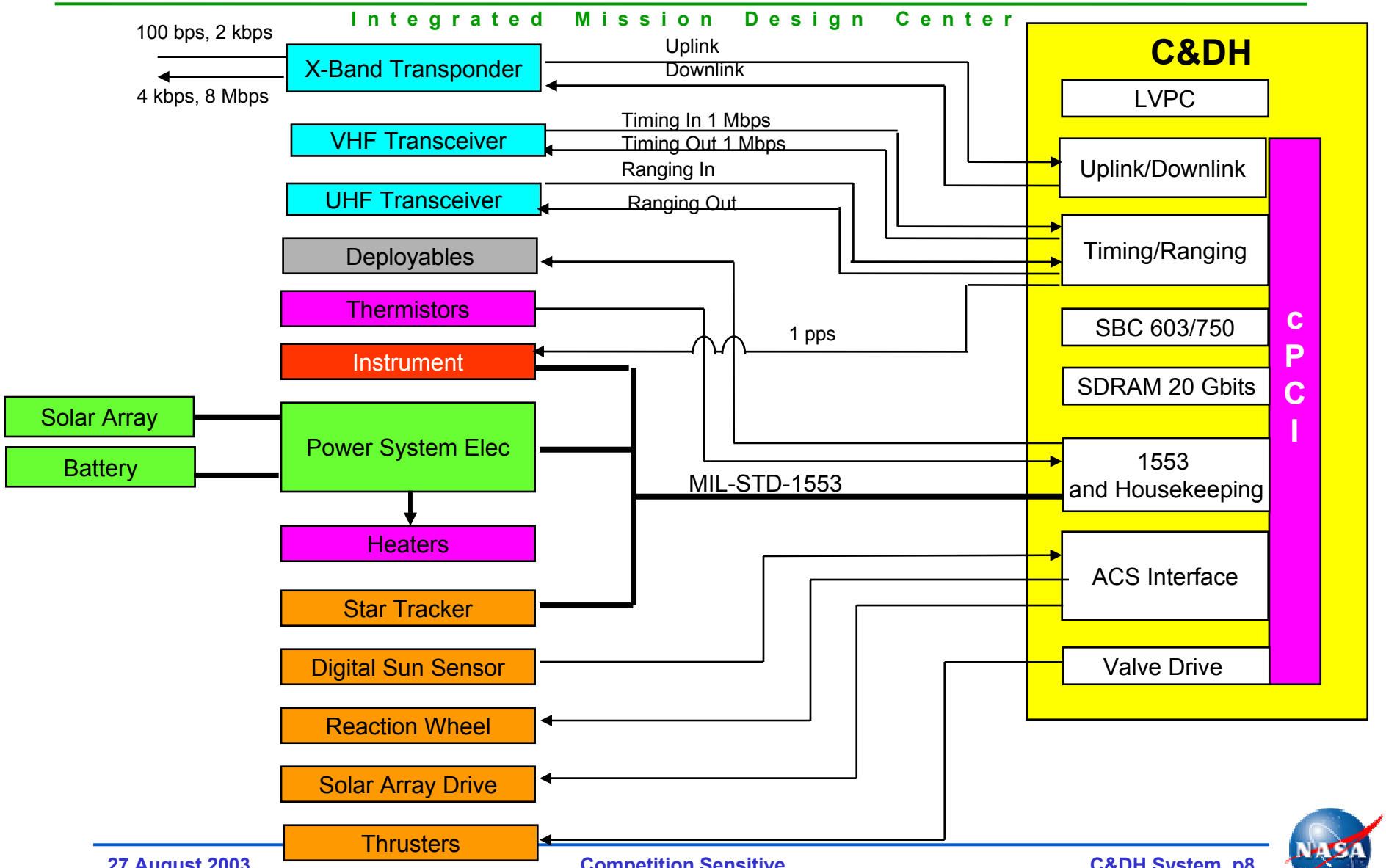
Critical Technologies

- **cPCI Data Bus (Backplane)**
  - Industry standard data bus
  - Most widely used data bus in upcoming space electronics
  - GSFC Missions: Triana, SWIFT, JWST, SDO, GPM
  - 1 Gbps peak transfer rate
  - 32 bits wide
  - 33 Mhz Operation
  - 8 cards maximum
  - 0.8” card spacing maximum
  - Processor-Independent
  - Parity checking on the address, command, and data
  - Rad-Hard implementation (Actel FPGA)

Critical Technologies

- **Power PC Single Board Computers (Processor Cards)**
  - "Standard" products
  - Manufacturers include BAE, Honeywell, Maxwell Technologies, and General Dynamics
  - GSFC missions: JWST, SDO, GPM
  - Typical specifications of latest products:
    - Power PC 603/750 microprocessor
    - 200+ MIPS
    - 1 Gbit SDRAM
    - 4 Mbyte EEPROM
    - cPCI Backplane
    - 50 krads to 100 krads total dose
    - 6U/160/220 card size
    - 1.2 kg (6U/220)
    - 13 W (full speed)

C&DH Diagram

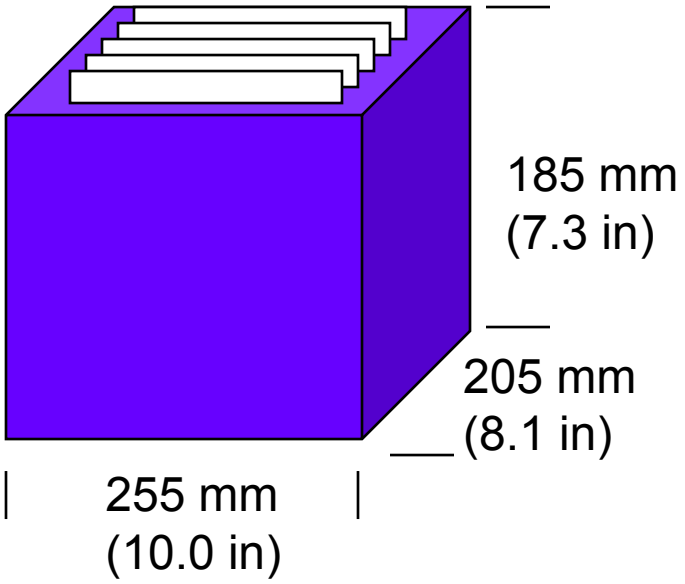

Integrated Mission Design Center
100 bps, 2 kbps
4 kbps, 8 Mbps
X-Band Transponder
Uplink
Downlink
VHF Transceiver
Timing In 1 Mbps
Timing Out 1 Mbps
Ranging In
UHF Transceiver
Ranging Out
Deployables
Thermistors
1 pps
Instrument
Solar Array
Battery
Power System Elec
MIL-STD-1553
Heaters
Star Tracker
Digital Sun Sensor
Reaction Wheel
Solar Array Drive
Thrusters
C&DH
LVPC
Uplink/Downlink
Timing/Ranging
SBC 603/750
SDRAM 20 Gbits
1553
and Housekeeping
ACS Interface
Valve Drive
cPCI

Clustered Cruise Phase

- 2 C&DH in two separate microsats powered on.
- Both microsats must have uplink, downlink, and star tracker FOV.
- The 2 C&DH have interfaces to the dispenser craft avionics unit.

C&DH Size

Card Size: 6U-160



C&DH Mass and Power

C&DH Assembly	Mass	Power	Comments
LVPC	1.2 kg	6 W	
Uplink/Downlink	0.6 kg	5 W	
Timing/Ranging	0.6 kg	3 W	
SBC 603/750	0.8 kg	7 W	Reduced Clock Rate
SDRAM Memory	0.6 kg	6 W	
1553 and Housekeeping	0.6 kg	5 W	
ACS Interface	0.6 kg	4 W	
Valve Drive	0.6 kg	2 W	
Backplane	0.2 kg	0 W	
Backplane Stiffener	0.4 kg	0 W	
Chassis (2 mm Al)	3.5 kg	0 W	
Total	9.7 kg	38 W	

C&DH Cost (1st spacecraft)

	C&DH
NRE	$1.3 M
2 S/W Breadboards	$0.3 M
Parts for 1 ETU, 1 Flight Unit	$1.5 M
Labor for 1 ETU, 1 Flight Unit	$1.2 M
S/C I&T Support	$0.4 M
Total	$4.7 M

Cost estimate assumes that spacecraft vender is developing the C&DH with heritage hardware.

Risk

- **No separate safehold processor**
  - C&DH Processor has watchdog circuit and safehold mode to protect against transient anomalies such as single-event upsets and software bugs
  - But there is no separate safehold processor to protect against a C&DH Processor anomaly such as a single event latchup which requires a power cycle to clear
  - Likelyhood: very unlikely (green), C&DH Processor is single event latchup immune
  - Ramification: very serious (red), spacecraft could lose power
  - Mitigation: Add safehold processor
    - mass, power, cost hit
    - Risk not necessarily mitigated
  - Recommendation: Acceptable risk

Items for Future Study

- Implement C&DH with 3U card size instead of 6U card size
- Potential to reduce C&DH mass from 9.7 kg to 5.7 kg (save 4 kg)
- This would probably require a large NRE cost.
- Recommendation: Only pursue this if mass is an extreme problem and money is not a problem.