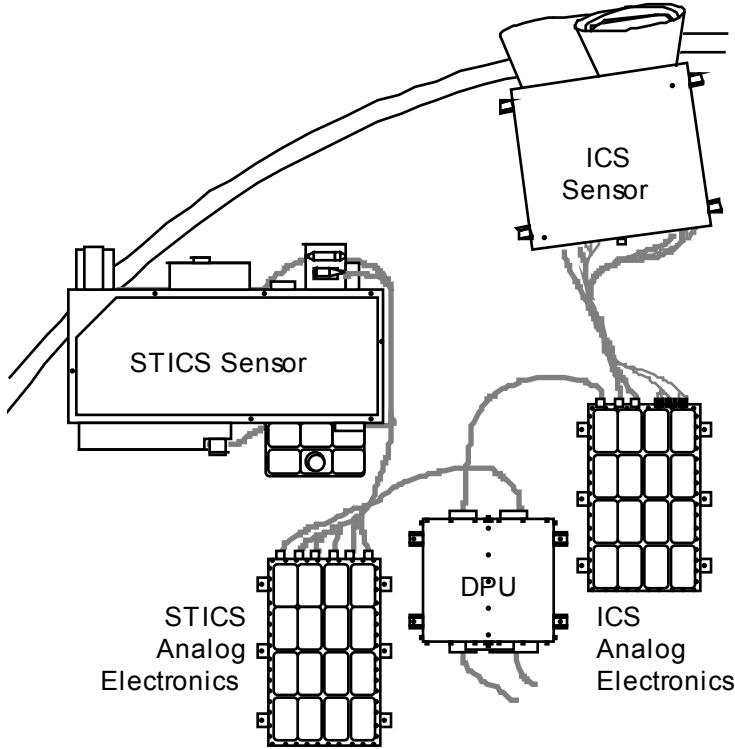


EPIC Instrument  
User's Manual



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## **Foreward**

This document is intended to be the working-document for the EPIC instrument. It is intended to be used to understand EPIC and to allow proper telemetry interpretation, and instrument control and commanding.

It contains elements of the Subsystem Control Document (SCD), the Data Definition Document (DDD), and the EPIC article in the Geotail “Yellow Book”, which were written by the contributors credited above. But it gets the Data Processing Unit (DPU) details directly from the DPU User’s Guide that was written by Andreas Hestermeyer.

The material has been checked, but typographical errors may still be present. Some sections still contain incomplete information, due to the limited amount of time the author has to examine the DPU source code. This will be made complete in future revisions of this document, as well as the inclusion of additional sections to document parameter changes as they occur and special operations, such as the making of DPU code patches.

## 1. INSTRUMENT DESCRIPTION

The EPIC instrument is actually composed of two separate sensor and processing assemblies. The STICS assembly (Supra-Thermal Ion Composition Spectrometer) uses a quadrispherical electrostatic analyzer followed by a foil/solid state detector time-of-flight (TOF) telescope to measure charge state, mass and energy of ions with energies of 30 - 230 keV/charge. It uses an electrostatic analyzer with a geometry factor of  $0.05 \text{ cm}^2 \text{ sr}$ , time of flight, and energy analysis.

The ICS assembly (Ion Composition Subsystem) measures mass and energy properties of energetic ions with energies of less than 50 keV to 3 MeV. It uses a pair of collimators with sweeping magnets to reject electrons, followed by TOF and energy analysis, with a geometry factor of  $0.2 \text{ cm}^2 \text{ sr}$ . A thin foil/solid state detector electron telescope measures electrons higher than 30 keV.

Table 1 summarizes main EPIC characteristics.

	<u>STICS</u>	<u>ICS</u>
Sensors:	Electrostatic analyzer x time-of-flight x E	Time-of-flight x E
Energy Range:	10-230 keV/e (M/Q) 30-230 keV/e (M and M/Q) $\Delta E/E = 5\%$	>10 keV (Integral) Ions >20 keV (Velocity) Ions >30 keV-3 MeV (M) Ions >30 keV and >100 keV (Integral) Electrons
Ion Species:	H through Fe	H through Fe
Resolution:		
Mass:	Resolves all major ion species Charge states of major ion species	Resolves all major ion species
Angular:	6 equal $26.7^\circ$ polar sectors ( $+80^\circ$ to $-80^\circ$ *)	2 equal $30^\circ$ polar sectors ( $-38^\circ$ to $-8^\circ$ ; $+8^\circ$ to $+38^\circ$ *) (Ions) 1 polar $60^\circ$ sector ( $-30^\circ$ to $+30^\circ$ *) (Electrons)
Time:	16 equal $22.5^\circ$ azimuthal sectors	16 equal $22.5^\circ$ azimuthal sectors
Time:	3 sec**/energy step 24 sec**/8-point spectrum	0.2 sec to 96 sec** (species dependent)
Geometry Factor:	$0.05 \text{ cm}^2 \text{ sr}$	< $0.006$ to $0.2 \text{ cm}^2 \text{ sr}$ (Ions) $0.1 \text{ cm}^2 \text{ sr}$ (Electrons)
EPIC S/C Interfaces:		
Mass:	Total mass 20.986 kg (including shielding, excluding cables)	
Power:	14.6 W electronics, <10 W thermal	
Data Rate:	2560 bps	

\* with respect to the spin plane

\*\* assumes the nominal 3 seconds/spin

Table 1 : EPIC Summary Table



## 1.1 Configuration

The EPIC instrument is comprised of 5 subassemblies: the STICS sensor, STICS analog electronics, ICS sensor, ICS analog electronics, and the Data Processing Unit (DPU). A schematic diagram of these assemblies and their mounting on the GEOTAIL spacecraft is shown in Figure 1.

The two sensors do the actual detection and measurements of the incoming particle flux; both contain microchannel plates, high voltage supplies, solid-state detectors, and preamplifier electronics. These are the only parts of the EPIC instrument that require visibility to the space environment.

Signals from the two sensors are sent to their respective analog electronics subassemblies, where the signals are further amplified, processed for timing and position information, and digitized. An inflight calibrator, voltage converter (+6V, -6V, +5.2V, -5.2V, +12V, -12V and SSD bias), interface controller, and valid-event logic are also present.

Digitized data from both of the analog sensor electronics then goes to the DPU, where the data are analyzed and accumulated over several spacecraft spins. In addition to this analysis, the DPU also handles all command decoding and processing, telemetry interface and formatting, power switching, and instrument control.

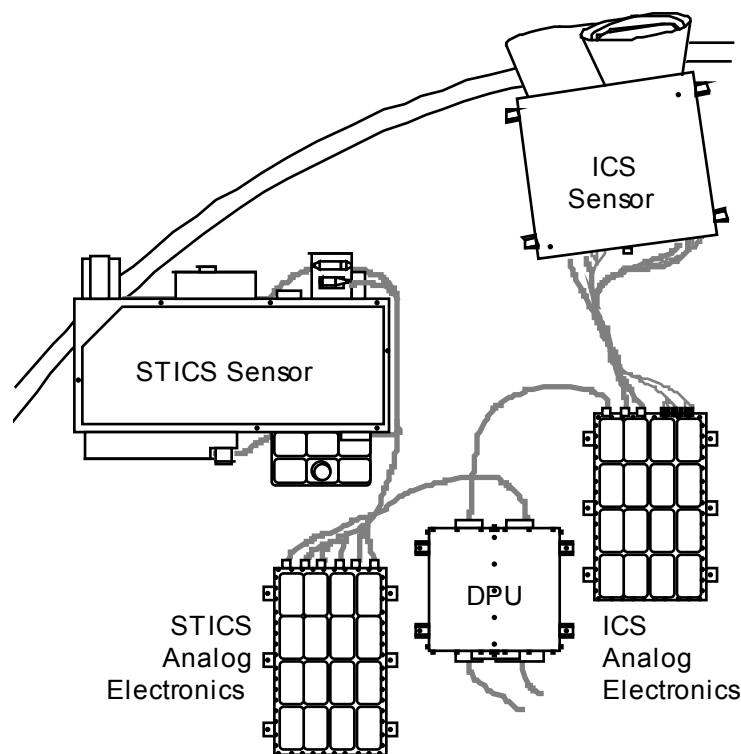


Fig 1 : EPIC Configuration Diagram

## 1.2 Spacecraft Interfaces

### 1.2.1 Mass and Size

The EPIC instrument mass allocation is 16.9 Kg, and the EPIC radiation shield mass allocation is 5.0 Kg. This 21.9 Kg allocation is exclusive of the inter-box cable mass. The mass and size allocation between subsystems is given in Table 2.

### 1.2.2 Power

The EPIC instrument uses spacecraft secondary power from the +15V, +29V, and +5.2V power busses. Of these three, the +15V and +5.2V power is used in the EPIC DPU box (for relay power and logic power, respectively), and the +29V is used in the sensors and the analog electronics (to power voltage converters, actuators, and heaters). The DPU filters, switches, and circuit-breaks the +29V supply but does not use it for circuit power. Figures 2, 3 and 4 show the DPU, ICS Sensor, and STICS Sensor power switching, respectively.

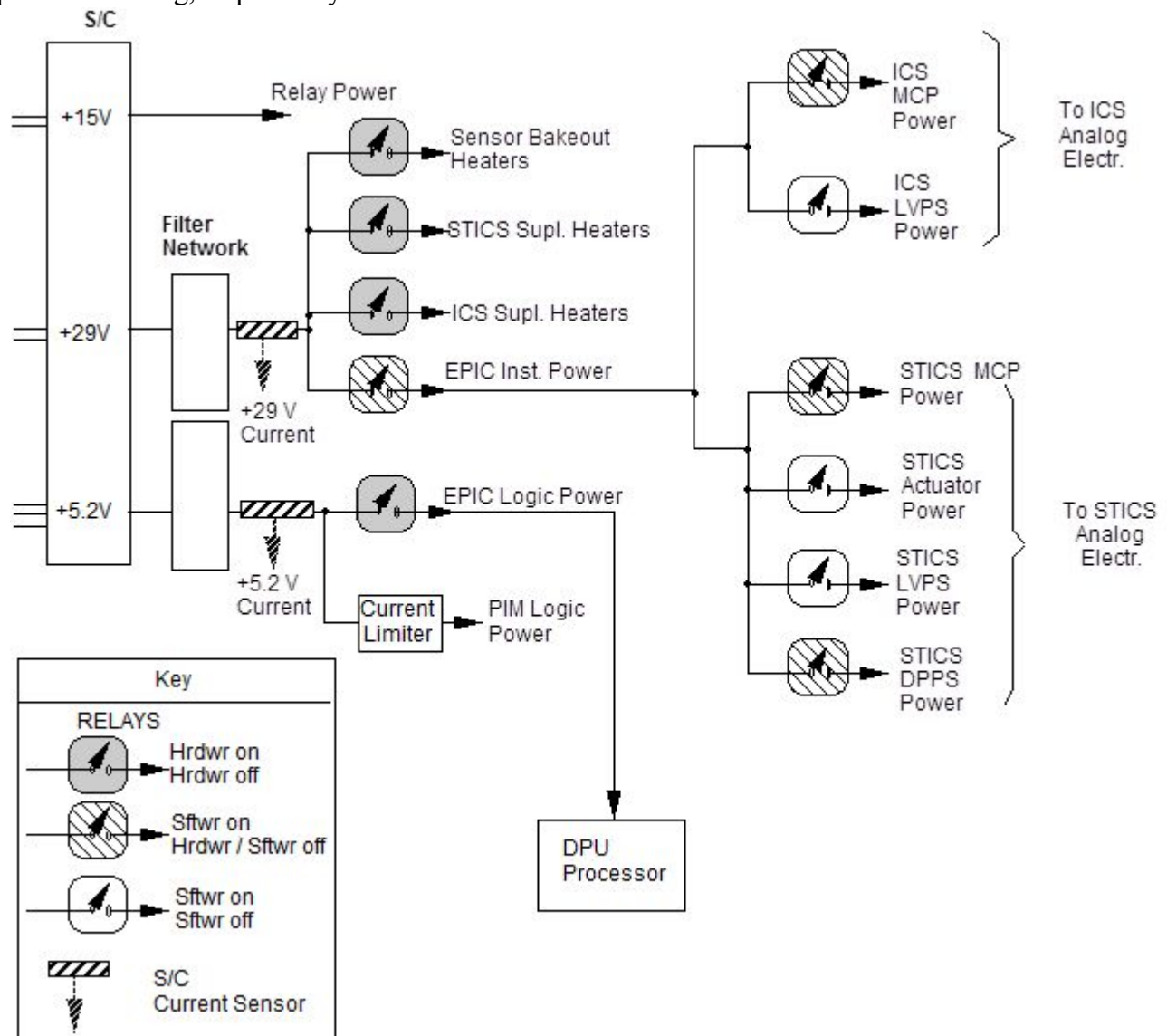


Fig 2 : EPIC Power Switching Diagram

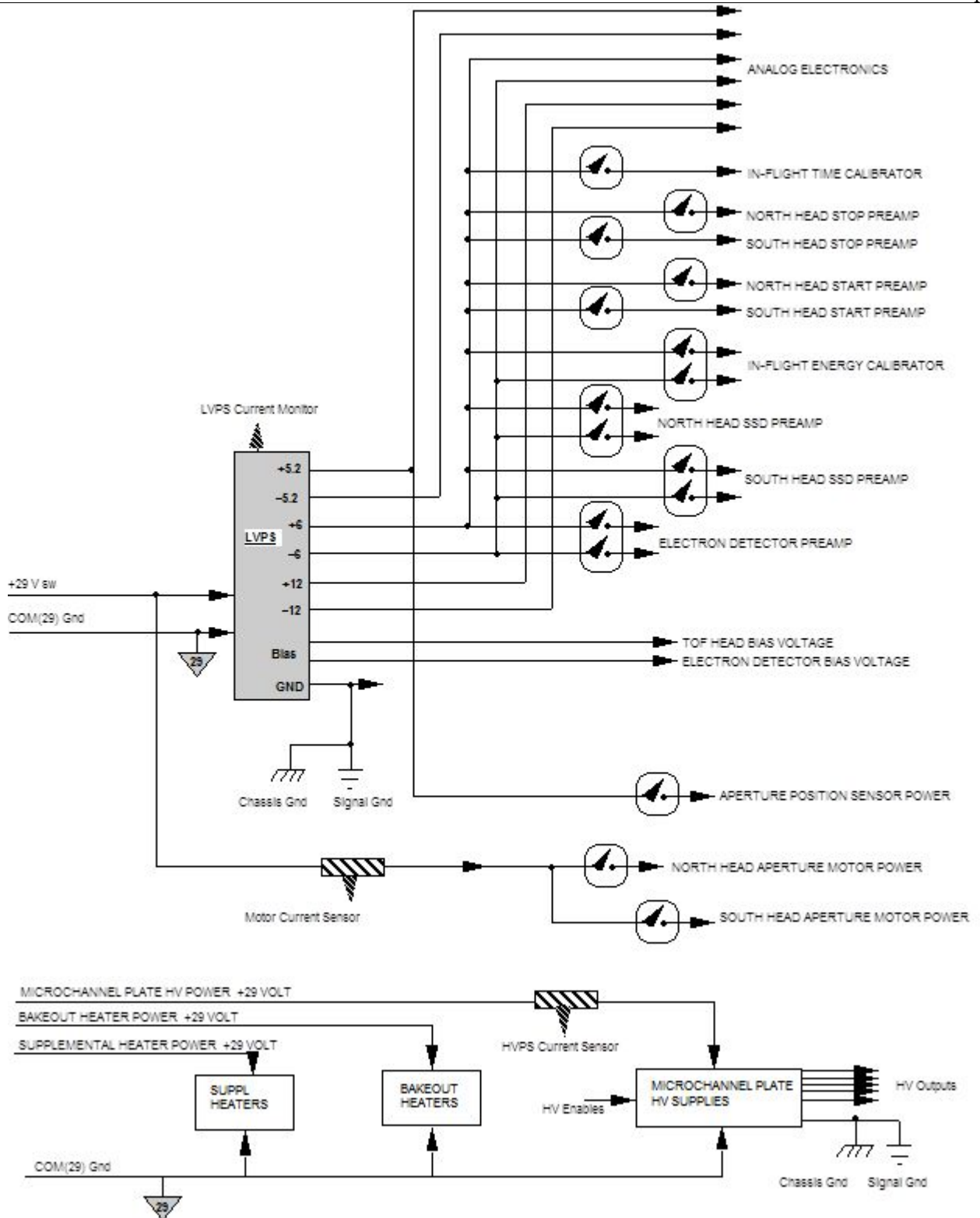


Fig 3 : ICS Switching Diagram

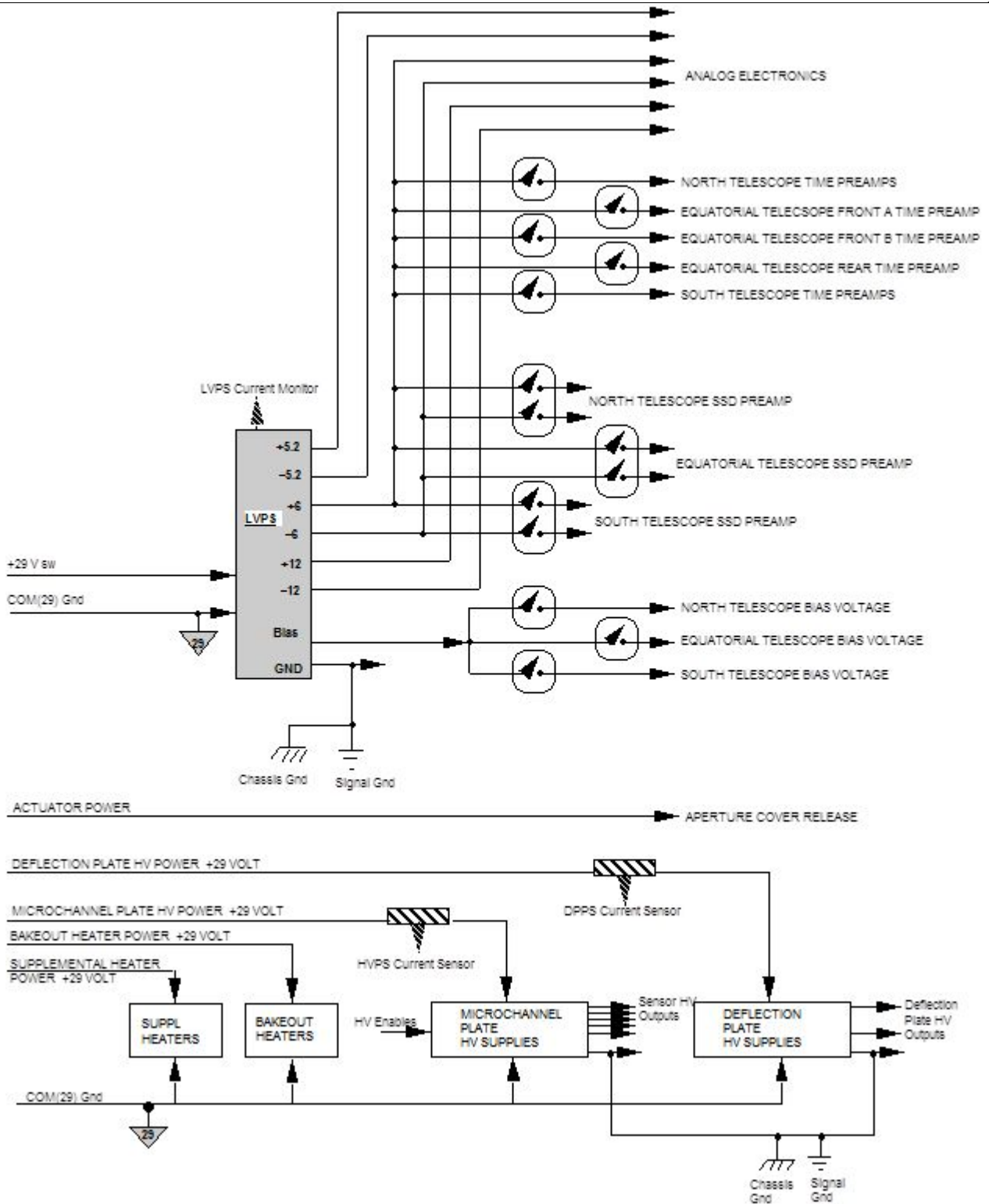


Fig 4 : STICS Power Switching Diagram

The spacecraft 5.2 volt power is not used in the analog electronics and sensors. EPIC powers the logic circuitry in those subsystems from the low voltage power converter secondaries (located in the two analog electronic boxes). This step was taken to avoid ground loops, and to allow referencing the high voltages to spacecraft chassis.

Unit Name	Mass (Kg)	Size (mm x mm x mm)
DPU	3.628	160.2 x 149.0 x 190
ICS Analog Elec	2.251	229 x 140.5 x 131
STICS Analog Elec	2.278	229 x 140.5 x 131
ICS Sensor Head	5.540	198 x 225 x 278
STICS Sensor Head	7.289	394 x 295 x 292
TOTAL EPIC INSTR.	20.986	

Table 2 : Mass and Size Allocations for EPIC Subsystems

### 1.2.3 Power Consumption per Operational Mode

The EPIC power allocation is 3.8 watts in electronics standby, 14.6 watts for full-up electronics operations, and 10 watts thermal. Power consumption in various instrument modes is shown in Table 4.

#### 1.2.3.1 Time Varying Aspects of the Power Profile

The STICS sensor contains two high voltage power supplies that are used to generate the deflection voltage on the sensor's electrostatic analyzer. Their output voltages are each stepped together from 300V to ~10 kV in a regular cyclical pattern. The output voltage is changed each spin (3 seconds nominal) and cycles every 32 spins (science record), and the pattern itself is chosen by uplink command to the instrument (e.g., 10 kV to 300 V gradually and then back directly to 10 kV; 300 V to 10 kV to 300 V where 16 spins are spent going from 300 volts to 10 kV, and 16 spins are spent returning to 300 V; or where all 32 spins are spent at a single voltage level, etc.). The power for these supplies is taken from the +29 V bus; the current on this bus will vary between ~18 mA and ~30 mA, depending on the selected voltage.

The great majority of the EPIC analog circuitry requires  $\pm 6$  volts to operate. Since this voltage is not provided by the spacecraft, it is necessary to produce it in the instrument via a voltage converter.

Each sensor analog electronics subassembly incorporates an inflight calibrator circuit. These circuits will be used approximately once per week in normal operation; only one subsystem calibrator will be used at a time. The calibrator will use ~30 mA from the +6V and ~8 mA from the -6V EPIC secondary supplies (0 mA when not in use), translating to less than 8 mA on the 29V bus.

#### 1.2.4.2 Temperature Varying Aspects of the Power Profile

The STICS and ICS sensor assemblies incorporate active thermal control circuits to maintain the solid state detectors within an allowable temperature range. The associated heaters, called the supplemental heaters, are located within both sensor assemblies, and are nominally sized at 3.0 and 7.0 watts for ICS and STICS, respectively. The heater controller's set-point (minimum temperature that the circuit tries to maintain) will be approximately  $-20^{\circ}\text{C}$  to  $-40^{\circ}\text{C}$ . The present thermal analysis indicates that the heaters will not be needed to maintain a safe temperature during the normal full operation mode of operation.

The bakeout and supplemental heaters are of the thermostatically controlled type. This means that a heater will either have full load on the supply lines, or no load. However, the supplemental heaters are arranged in two stages, the first engaging at  $<-30^{\circ}\text{C}$  as replacement heat for the sensors, and the next stage at  $<-35^{\circ}\text{C}$  as true supplemental heat. The heaters turn off  $10^{\circ}\text{C}$  above the turn-on temperature.

OPERATIONAL MODE <sup>+</sup>		Instrument Description				
		+5.2 V (mA)	+15 V (mA)	+29 V (mA)	29 V Thermal (mA)	
(1)	OFF	PEAK	20 ± 4	‡	2 ± 1	0 ± 0
		AVG	20 ± 4	‡	2 ± 1	0 ± 0
(2)	BAKEOUT	PEAK	20 ± 4	‡	2 ± 1	290 ± 20
		AVG	20 ± 4	‡	2 ± 1	290 ± 20
(3)	STANDBY (SHADOW)	PEAK	240	‡	2 ± 1	160 ± 15
		AVG	228 ± 15	‡	2 ± 1	160 ***
(4)	ICS TEST	PEAK	410	‡	145 ± 10 **	160 ± 15
		AVG	228 ± 15	‡	125 ± 10	0 ***
(5)	STICS TEST	PEAK	400	‡	150 ± 10 **	160 ± 15
		AVG	228 ± 15	‡	130 ± 10	0 ***
(6)	DUAL TEST	PEAK	470	‡	285 ± 20 **	160 ± 15
		AVG	228 ± 15	‡	270 ± 20	0 ***
(7)	ICS OPER.	PEAK	410	‡	170 ± 20 **	160 ± 15
		AVG	228 ± 15	‡	150 ± 20	0 ***
(8)	STICS OPER	PEAK	400	‡	235 ± 20 **	160 ± 15
		AVG	228 ± 15	‡	215 ± 20 *	0 ***
(9)	FULL OPER (REAL)	PEAK	470	‡	395 ± 30 **	160 ± 15
		AVG	228 ± 15	‡	375 ± 30 *	0 ***

Notes: 11 August 1993

‡ Current for this supply is 30 mA for 8 milliseconds per relay being switched, 0 mA otherwise

\* See time varying aspects of power profile - deflection plate power supply

\*\* See time varying aspects of power profile - calibrator circuits

\*\*\* See temperature varying aspects of power profile - supplemental heaters

+ The sequence of operational modes (1) through (8) represent the EPIC initialization sequence. Mode (9) represents routine operation.

Table 3 : EPIC Power Consumption

### 1.2.5 Power Line Interface Diagram

The power line interface between the spacecraft and the EPIC instrument is shown in Fig. 5.

## 1.3 Operational Modes

The EPIC instrument can be operated in a variety of modes, stemming from the fact that there are two sensor assemblies. These modes are summarized below. (Mode numbers are for reference only.)

MODE	DPU PWR (MAIN)	HEATER POWER		ANALOG POWER		HIGH VLT POWER	
		Bake	Suppl†	ICS	STICS	ICS	STICS
1	OFF	OFF	ON	OFF	OFF	OFF	OFF
2	OFF	ON	OFF	OFF	OFF	OFF	OFF
3	ON	OFF	ON	OFF	OFF	OFF	OFF
4	ON	OFF	ON*	ON	OFF	OFF	OFF
5	ON	OFF	ON*	OFF	ON	OFF	OFF
6	ON	OFF	ON*	ON	ON	OFF	OFF
7	ON	OFF	ON*	ON	OFF	ON	OFF
8	ON	OFF	ON*	OFF	ON	OFF	ON
9	ON	OFF	ON*	ON	ON	ON	ON

\* Thermal analysis and operation to date indicate that no heater power is used in these modes during normal operation, since the temperature will be above the thermostat set-point. However, EPIC may use up to the 10 watts thermal power when the temperature drops below the set-points.

† The supplemental heater is off during the first minutes of the mission, and on to maintain a safe sensor temperature during all other mission phases except bakeout.

### 1.3.1 Mode Description

MODE 1: Used immediately during and following launch or during low power modes of spacecraft operation. Solid-state detectors may become too cool if left in this mode too long.

MODE 2: Started ASAP after launch with a 2 week duration minimum prior to high voltage operation to help prevent outgassing material on sensor assembly surfaces. Sensor temperatures must be monitored in this mode. The STICS aperture will be opened in this mode. The DPU must be on approximately 10 minutes to open the aperture.

MODE 3: Used to safely store instrument in inactive state during mission. Instrument DPU will be active, but interface circuitry for the sensors may be unpowered.

MODE 4: Used to test only the ICS sensor electronics - no TOF measurements are made, but energy spectra may be available. STICS sensor is inactive.

MODE 5: Used to test only the STICS sensor electronics - no TOF or energy measurements will be available. ICS sensor is inactive.

MODE 6: Used to test both the ICS and STICS sensor electronics - no TOF measurements are made, but energy spectra may be available from ICS.

MODE 7: Used to operate the ICS sensor in its data measurement mode - full energy and TOF information available. STICS sensor is inactive.

MODE 8: Used to operate the STICS sensor in its data measurement mode - full energy and TOF information available. ICS sensor is inactive.

MODE 9: Used to operate both the ICS and STICS sensors in their data measurement mode - full energy and TOF information is available. This is the "full-up" operational mode, and will be the normal configuration of the instrument during the mission.

NOTE: Both the ICS and STICS sensors incorporate an in-flight calibrator. This calibrator can be used to augment ground testing or can be used in flight. Calibration tests may be run in any of modes 4-9.



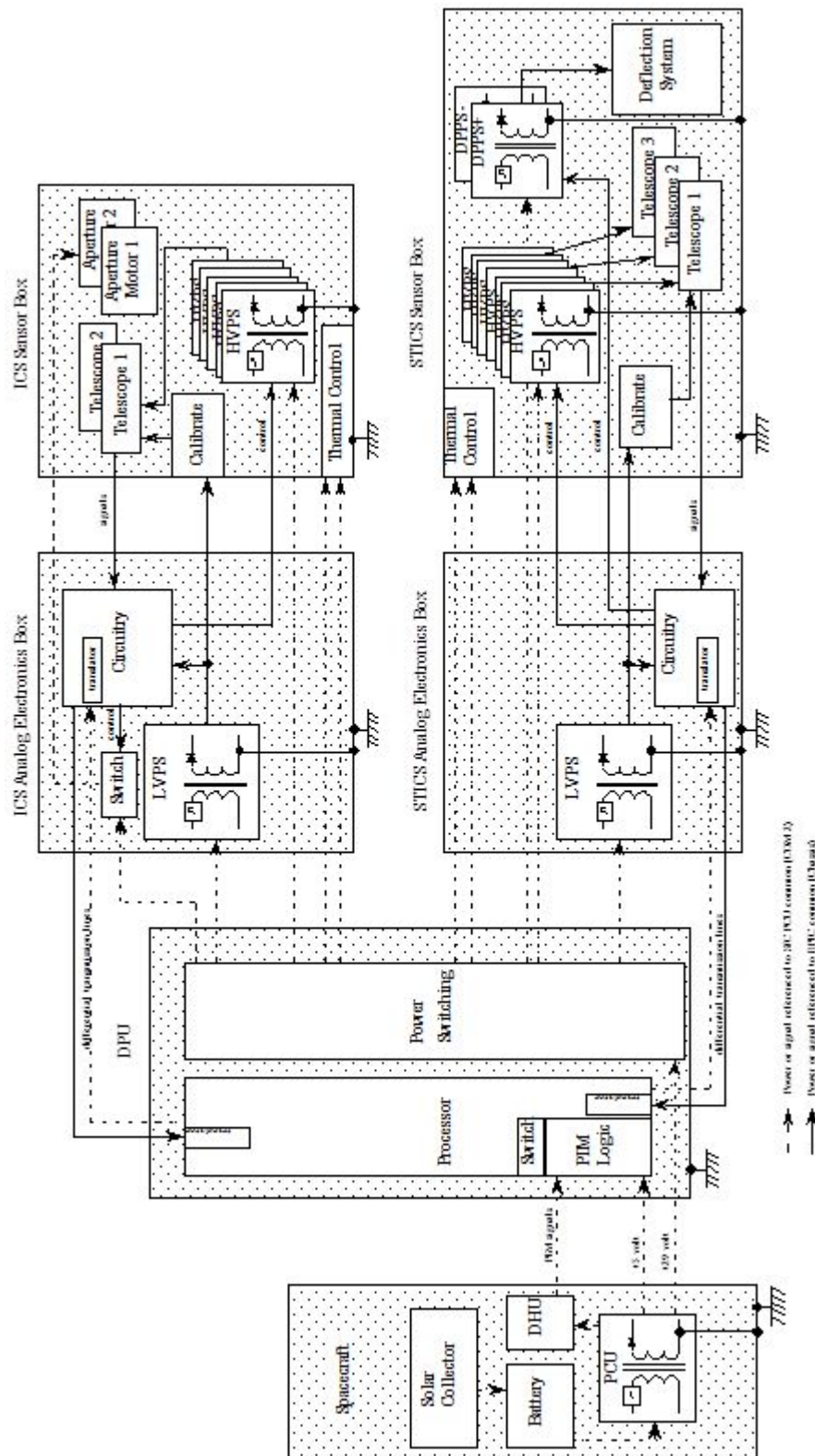


Fig 5 : EPIC High Level Power and Grounding Diagram

## 1.4 Sensor Signals and Data Processing

EPIC contains two sensor subsystems (STICS and ICS) that measure incident ions using TOF and total energy to determine ion species distribution functions and spectra over the total energy range of 10 keV to 5 MeV (including charge state from 30-230 keV/e) with large geometry factors and good angular time resolution. Each subsystem contains its own analog electronics package and feeds the common Data Processing Unit (DPU). Figures 6, 7 and 8 show the block diagrams of these subsystems.

The two sensor subsystems contain microchannel plates, high voltage supplies, solid-state detectors, and preamplifier electronics. The two analog electronics subassemblies contain analog and digital processing where the signals from the sensors are amplified, processed for timing and position information, and digitized. An in-flight calibrator, analog voltage converter, and valid-event logic also are included in the analog electronics packages. In the DPU, the data are analyzed and accumulated over several spins. In addition to analysis, the DPU handles all command decoding and processing, telemetry formatting and interface, power switching, and instrument control.

### 1.4.1 The Ion Composition Subsystem (ICS)

The ICS is designed to measure ion fluxes and ion composition above  $\sim 50$  keV with the geometry factor and angular, temporal and species resolution appropriate to the scientific requirements of the Geotail mission. The block diagram for ICS is shown in Figure 6. The ICS contains two identical sensors, oriented above and below the ecliptic plane for complete angular coverage. Each sensor head contains a thin-foil, solid-state detector TOF telescope. A front collimator with an electron sweeping magnet precedes a thin, grid-mounted foil which is the front element of the telescope. A silicon surface barrier solid-state detector is located approximately 6 cm behind the foil. Energetic ions passing through the front foil and striking the back solid detector emit low energy secondary electrons from both foil and silicon detector surfaces, and these electrons are mapped onto separate microchannel plates by electrostatic optics within the telescope. The signals produced by the microchannel plates define the ion TOF (and thus velocity) between the front foil and the rear solid state detector. Ion energy is measured in the rear detector. Since measurement of ion velocity and energy determines the ion mass, ICS is capable of measuring the spectra and dynamics of all ion species over the Geotail orbit.

Energy coverage is a function of species with a lower threshold of  $\sim 10$  keV/nucleon. The ICS produces composite ion energy spectra, composite velocity spectra, and species-resolve spectra.

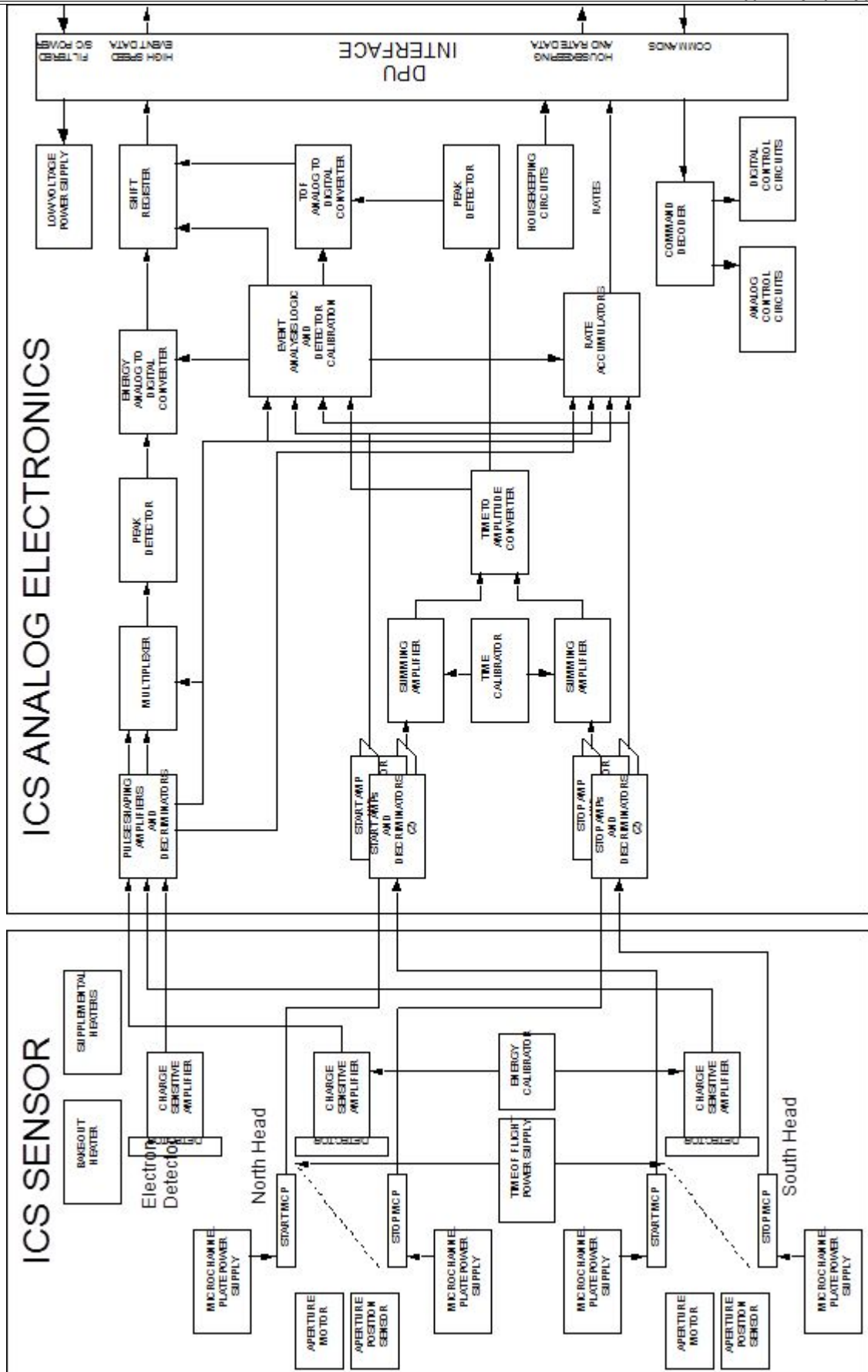


Fig 6 : EPIC ICS Sensor Block Diagram

The Geotail orbit covers a range of particle environments, from the very low-flux regions of the lobes to the substantial fluxes in the near-earth plasma sheet in active times. The geometry factor of each ICS head is therefore adaptive, from  $0.1 \text{ cm}^2 \text{ sr}$  to  $<0.01 \text{ cm}^2 \text{ sr}$  including both an electronic variation of the effective area of each microchannel plate, and an ability to mechanically vary, by command, the telescope's physical aperture. Temporal resolution ranges from 0.2 sec to 96 sec depending on the individual channel sampling frequency, and data is sectorized into 16 azimuthal angular lines. The ICS Head assembly feeds signals into the ICS Analog Electronics box which processes signals into the center EPIC DPU subsystem.

#### 1.4.2 The SupraThermal Ion Composition Spectrometer (STICS)

The STICS is designed to measure 3-dimensional distribution functions of major ion species with sufficient time resolution to determine source regions (solar wind vs. ionosphere) and acceleration processes of suprathermal ions in the near and distant geomagnetic tail. The block diagram for STICS is shown in Figure 7.

STICS separately determines the mass, energy and charge state of low energy charged particles in the range 30 to 230 keV/charge with mass per charge and velocity determinations continuing to 10 keV/charge. It comprises a quadrispherical deflection system for the selection of particles of the desired energy per charge followed by a TOF telescope for the measurement of particle velocity and energy. A position measuring system on the START TOF electrode provides information on the entrance angle of the particle into the telescope.

The sensor contains the deflection system TOF telescope, HV power supplies and detector preamplifiers. The remainder of the analog electronics, including shaping amplifiers, discriminators, TOF circuits and analog-to-digital converters (ADCs) are located in the separate Analog Electronics box. This is done to free the mechanical design of these circuits from the constraints imposed by the odd shape of the sensor package and to make possible the sharing of common layouts with ICS sensor processing. Outputs from the Analog Electronics box pass into the shared EPIC Data Processing Unit where they are processed for transmission to the spacecraft.

A schematic description of the operation of the deflection system and telescope is as follows:

1. Particles enter the Entrance Aperture through a simple collimator.
2. Particles are deflected by the E-field in the deflection system. This field is created by the voltage from a pair of high voltage power supplies (the DPPS) applied to the deflection plates. The DPPS is programmed to step the voltage on the plates once per spin. The steps are logarithmically spaced and a sequence of 32 steps takes the system from near 0 volts deflection to the maximum deflection voltage.
3. Particles of correct E/Q make it through the deflection system and strike the thin carbon foil at the entrance of the TOF telescope.
4. Secondary electrons are knocked off the inner surface of the foil.
5. The incoming particles pass undisturbed into and through the TOF telescope chamber.

6. The secondary electrons are deflected by E-fields inside the telescope and strike one of the three START MCPs. The deflection preserves the position of origin of these electrons in the position they strike the MCPs.
7. Six discrete anodes (two per MCP) lie behind the MCPs, providing position information on the incoming particles.
8. At the far end of the TOF telescope the incoming particles strike one of the three solid state detectors.
9. Secondary electrons from the front surface of the SSDs are deflected onto three STOP MCPs.
10. Energy information comes from the SSDs. Energy/charge information comes from knowledge of the voltage on the deflection system, elevation angle of the incoming particle comes from the START MCP anodes, clock angle of the incoming particle comes from the START MCP anodes, clock angle of the incoming particle comes from the S/C spin/sector clock and TOF information comes from the signals from the START and STOP MCP anodes.
11. From simultaneous measurements of the TOF ( $t$ ), the residual energy ( $E_{\text{meas}}$ ), and a knowledge of the energy per charge ( $E/Q$ ) from the deflection system, EPIC determines the mass ( $M$ ), ionic charge ( $Q$ ), and the incident energy ( $E$ ) of each ion.

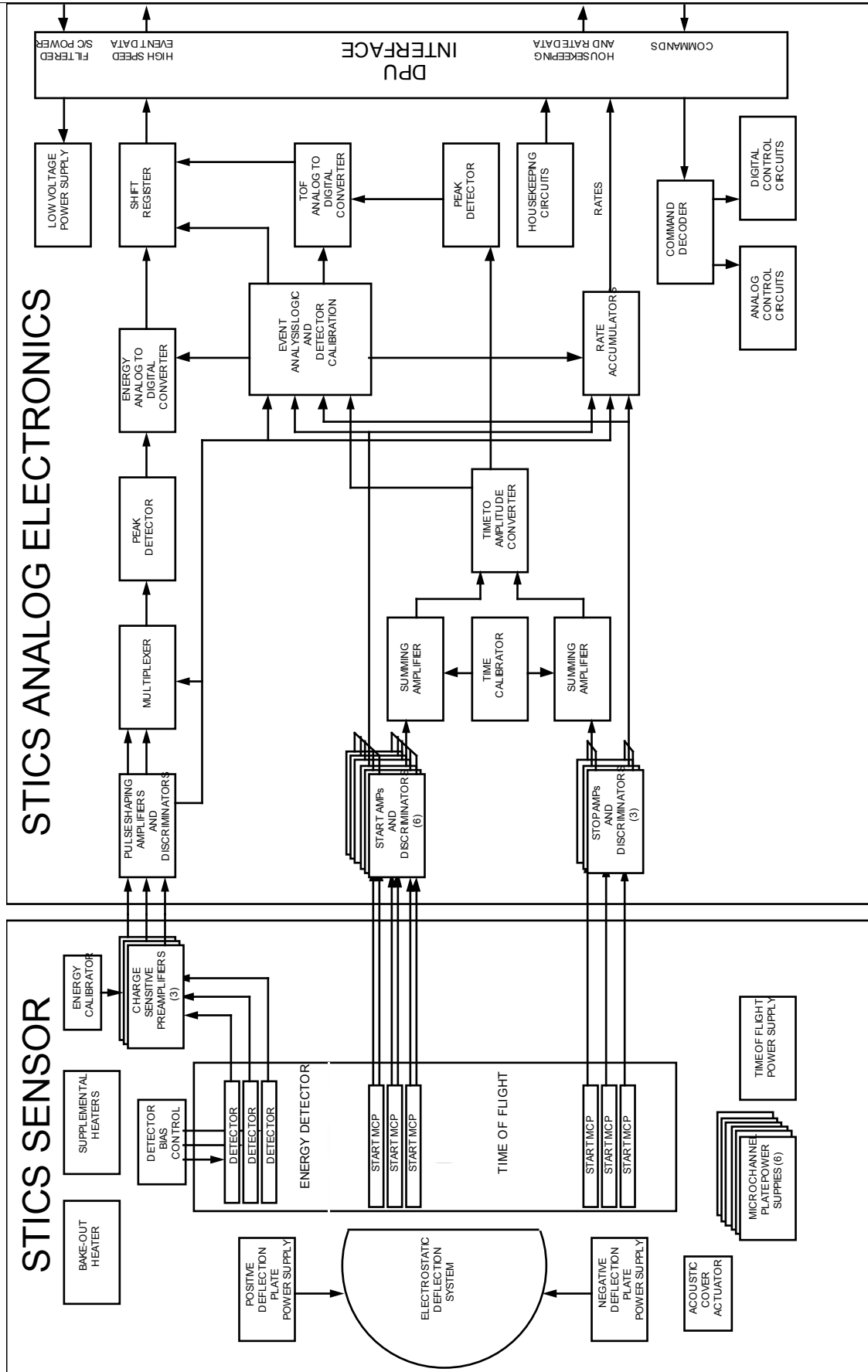


Fig 7 : EPIC STICS Sensor Block Diagram

### 1.4.3 Data Processing Unit (DPU)

The DPU is responsible for all interfaces between the spacecraft and STICS and ICS subsystems. The block diagram for the DPU is shown in Figure 8. It handles all command processing, telemetry formatting, analog interfaces, power switching, alarm monitoring, and mechanical device control for the instrument. Through the use of the spacecraft-provided timing and spin signals, the DPU periodically collects science TOF and energy pulse height data from the subsystems via serial command and data lines. This data is processed on board the instrument, sorted by category and type of event, and compressed into the available telemetry stream.

The other principal functions of the DPU are to:

- Execute the fast classification of ions analyzed in STICS according to the ion mass and mass per charge;
- Collect and store count rate and pulse-height data, determine event priority and execute appropriate event sequencing;
- Compress the contents of each counting rate register into an 8-bit floating point representation and format all data and transfer this information to the spacecraft;
- Perform all necessary control functions for the experiment, accept and execute commands, monitor the experiment status, and execute the internal calibration sequence upon command.

The DPU can be subdivided into four functional parts:

1. Sensor Interface
2. Fast data processing by means of task-dedicated hardware
3. Medium speed data processing and instrument control by means of a 80C86 microprocessor system
4. Spacecraft interface

Data flow is primarily from part (1) to part (4), while commands flow is the other way. The data rate is reduced from 6 Mbits/sec at the entrance of part (1), i.e., the sensor outputs, to the instrument telemetry rate of approximately 2.5 kbits/sec at the output of part (4). Much of this data compression and processing is performed by the dedicated hardware in part (2).

The high-speed classification is implemented through the use of direct RAM-based table looked-up techniques. This approach, made possible by new high-density RAMs, means the classification algorithms may be changed in flight if necessary. The contents of the tables will be calculated on board the instrument, based upon a limited number of uploaded parameters.

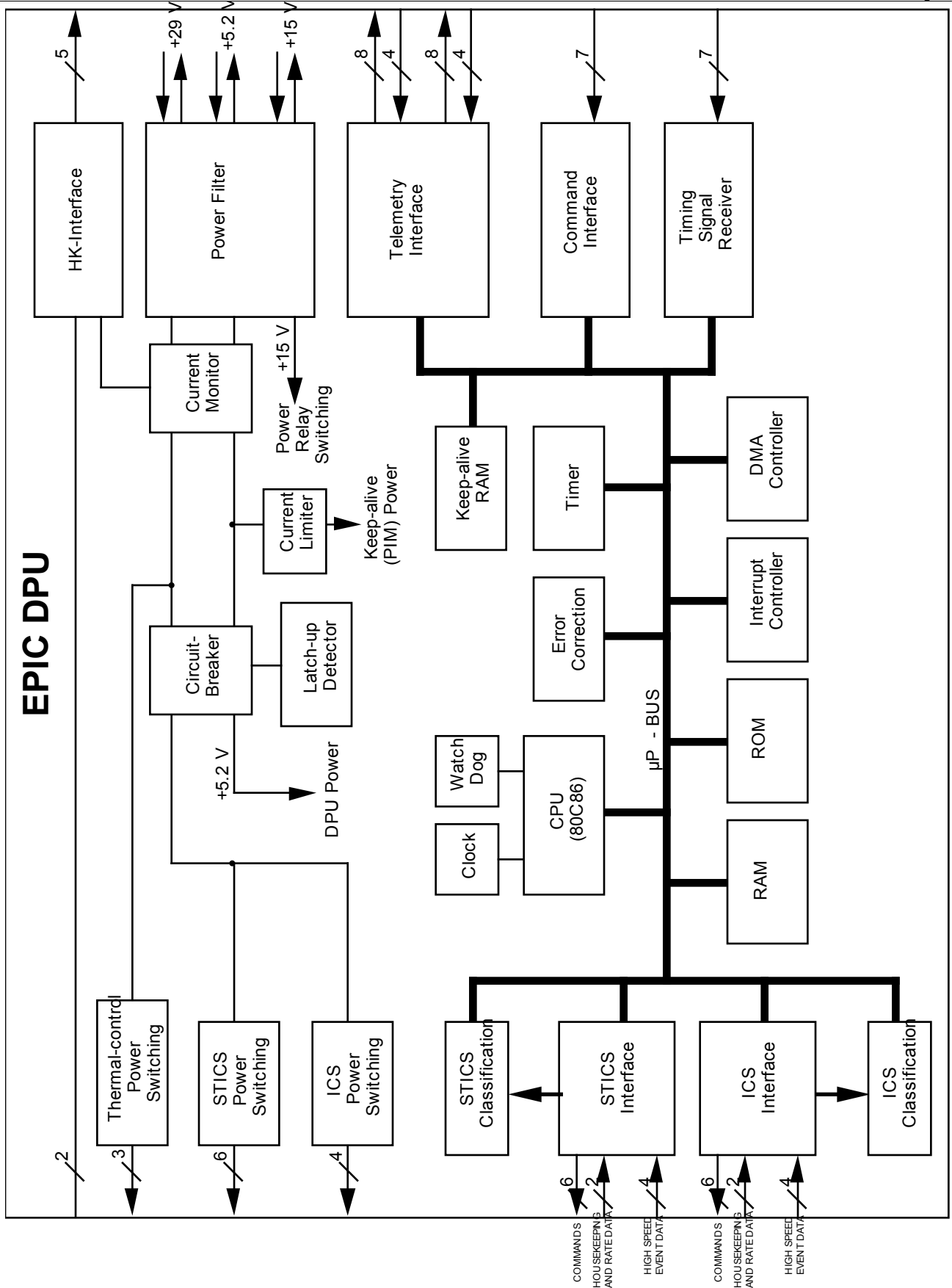


Fig 8 : EPIC DPU Block Diagram



In addition to the science data processing, the DPU also handles a number of other tasks. Command decoding is performed by two different circuits. A special command decoder, running off the unswitched 5.2 volt supply, can decode basic commands such as heater on/off and instrument on/off. This circuit allows the processing of these basic commands even when most of the instrument is off or malfunctioning. All other commands are decoded by the microprocessor hardware and software, allowing for more sophisticated command verification and sequencing.

All instrument power switching is handled in the DPU via low voltage relays. This supports power cycling of instrument subsystems (preamps, event processors, etc.), as well as basic instrument control.

The spacecraft interface is supported on both the real time and recorded mode interfaces. Other spacecraft features, such as RAM loads and verification (for program updates or parameter loads), undervoltage load management, and real time status are also supported.

Because of the limited access to real-time ground-based control, the instrument also incorporates a sophisticated housekeeping monitor. The instrument operating system continuously cycles through a number of instrument analog parameters, such as temperatures, voltages, currents, and status. If these parameters are found to be outside predetermined limits, the DPU initiates an appropriate alarm routine, and sets an alarm bit in the real-time spacecraft status.

In summary, the DPU subsystem is responsible for interfacing the science subsystems to the spacecraft. It handles the proper decoding and processing of almost all digital information in the EPIC instrument, whether the information comes in as science data from the sensor electronics or commands from the spacecraft.

### **1.5 Contamination, Purge, and Venting**

Both the STICS and ICS sensor heads are very sensitive to vapor contaminants, humidity and temperature. The microchannel plate gains may be affected by as little as 20% humidity or more; therefore dry nitrogen purge gas must be maintained at all times. The purge supply should be designed to prevent surges in pressure (such as turn-on) to avoid damage to the thin front detector foils. The detectors and microchannel plates may be physically damaged by humidity over ~55%.

Extreme care must be taken to avoid particulate matter and vapors from fuels, plastics, paint, cleaning compounds, RTV, adhesive, instant films, smoke, or volatile materials near the sensors, as such contamination will damage microchannel plates and solid state detectors, and the damage may not be detectable prior to launch.

Extreme care must also be taken to assure that the ICS and STICS sensors are not subjected to thermal environments which exceed 30° C as temperatures above this can destroy the solid state detectors. During spacecraft ground test operations, cooled conditioned air, in addition to the purge gas, may be required to prevent sensor temperatures from exceeding 30° C.

Full operation of the sensors is possible only in high vacuum (pressure below  $2 \times 10^{-6}$  torr for at least five hours). All vacuum testing performed at the spacecraft level should be performed in a clean vacuum facility (i.e., cryogenic pump or oil pump with cryogenic trap). Red tag HV safing plugs will be installed to prevent accidental high voltage supply actuation under ambient conditions. They will be temporarily removed for the thermal vacuum test and permanently replaced by a cover or blank just before shroud closure. The safing connectors will be located on the sensors at a point accessible from the outside of the spacecraft.

The sensor head assemblies vent directly to space through vent ports. Other sections vent locally, i.e. into the spacecraft interior. Venting to space for a minimum of 2 weeks after launch was required prior to EPIC high voltage turn-on.

## **2. PARTICLE CLASSIFICATION**

Once initialized by the DPU, the STICS and ICS instrument's electronics send event words to the DPU which include information about the energy, the time-of-flight and the (polar) flight direction of measured ions.

The way the DPU processes the data of both instruments is basically the same : the event words are classified by time, energy and (polar & equatorial) direction. The equatorial direction is derived from the S/C revolution, which each revolution (spin) is subdivided into 16 sectors. Each class (often referred to as a bin) is assigned a counter (the bin counter) which increments each time an event of that class is received. The bin counters are read and reset by the DPU on a cyclic basis, different bins can have different cycles. The counter values (rates) are logarithmically compressed and the resulting values are placed in the telemetry data stream.

Additionally, some event words are selected and placed into the telemetry data stream as they are. This is the direct event data, the single events are referred to as PHA words (PHA means pulse height analysis).

The classification process for STICS and ICS mainly differ in the fact that STICS has a deflection plate system and therefore is able to measure the charge state of each particle, which ICS is not able to do.

STICS classifies the particle mass into mass classes as a function of energy and time-of-flight. It also classifies the particle mass-per-charge into mass-per-charge classes as a function of time-of-flight and present deflection voltage. The mass classes and the mass-per-charge classes define a two-dimensional space in which the STICS bins are defined. Two types of bins are used : the science bins and the basic bins (the values of the assigned counters are the science rates and the basic rates). The science bins are defined such that every bin represents a particle species with a defined charge state.

The basic bins represent the areas in the mass vs. mass-per-charge class space from which the PHA words are selected. Due to the limited telemetry data rate, not every event word which falls into one of these areas can be transmitted as a PHA word. To get information about the absolute number of events in the basic bins, the DPU also counts basic rates.

Most rates for STICS are summed over all directions and get reported once per spin. Some rates are transmitted with the highest directional resolution possible (16 sectors \* 6 polar directions) and some other with half the possible directional resolution.

ICS classifies each particle by mass, energy and time-of-flight. The mass bins (areas in the energy vs. time-of-flight plane) are also used for PHA word selection. A prioritization scheme is used where the

DPU always tries to select PHA words from high priority bins. The priority is rotated between the bins every 2nd spin by means of energy level and mass.

The ICS rates are summed in a number of formats. Some rates are transmitted with a high directional resolution and a low time resolution by summing rates from the same sectors and polar directions over a couple of spins. The maximum number of spins over which the rates are summed is 32. Therefore, 32 spins were defined to be the EPIC science record.

## 2.1 STICS Instrument

The event data transmitted by the STICS instrument to the DPU has the following format. One event word is transmitted for each particle to be classified. The maximum data rate is 100,000 events/second.

9	8	7	6	5	4	3	2	1	0	9	8	7	6	5	4	3	2	1	0	1	0	3	2	1	0	1	0
TOF( $T_d$ )										Energy( $E_d$ )										SSD	START				STOP		

Fig 9 : STICS Event Word

With its knowledge about the current deflection voltage level step  $S$ , the DPU classifies each received particle into a mass class ( $N$ ) and a mass per charge class ( $NQ$ ) using the transmitted  $T_d$  and  $E_d$ . The mass and mass-per-charge class is then used to classify the event into its science and basic bin.

The SSD-, START- and STOP-identifiers are used to differentiate between 6 polar directions ( $PD_0$  -  $PD_5$ ). The START-Id has priority over the STOP id and the STOP id has priority over the SSD id. Thus, if no START id is given, the STOP id is used to determine the direction and if also no STOP id is given, the SSD id is used to determine from which direction the particle came into the telescope. Since the STOP- and SSD-Id's only have a resolution of 3 Directions, the events are assigned to directions  $PD_0$ ,  $PD_2$  and  $PD_4$ . If an invalid id information is provided, the event is classified in direction  $PD_6$ , which is an artificial "direction" defined for debugging purposes.

The next sections will give an overview about the math equations used to classify events, one other subsection will deal about how the DPU implements this.

### 2.1.1 Mass classification

The mass classification uses the equation

$$\ln(m) = A_1 + A_2 \cdot x + A_3 \cdot y + A_4 \cdot x \cdot y + A_5 \cdot x^2 + A_6 \cdot y^3 \quad (1)$$

$$x = \ln(E_m) \quad (2)$$

$$y = \ln(T_m) \quad (3)$$

$$E_m = (E_d - EOC) / EADC \quad (4)$$

$$T_m = (T_d - TOC) / TADC \quad (5)$$

where :

m	is the mass in [amu]
$E_m$	is the measured energy in [keV]
$T_m$	is the measured time-of-flight in [ns]
$E_d$	is the digital energy contained in the event word in [channel] (0..1023)
$T_d$	is the digital time-of-flight contained in the event word in [channel] (0..1023)
EOC	is the conversion offset of the energy analog-to-digital (ADC) converter of the instrument analog electronics (AE) in [channel]
EADC	is the energy A/D conversion factor of the AE ADC in [channel / keV]
TOC	is the conversion offset of the time-of-flight ADC of the instrument analog electronics in [channel]
TADC	is the time-of-flight A/D conversion factor of the AE ADC in [channel / ns]
are the polynomial coefficients with the default values follow:	
$A_1$	2.69575
$A_2$	-0.843766
$A_3$	-2.38009
$A_4$	0.385641
$A_5$	0.0513127
$A_6$	0.0690096

The mass m is mapped onto a logarithmically space mass-class axis by the relation

$$m = m_{\min} \cdot k_4(NM-1) \quad (6)$$

$$k_4 = (m_{\max}/m_{\min})^{1/NMAX} \quad (7)$$

where

m	is the mass in [amu]
NM	is the mass class [1..NMAX]
NMAX	is the highest mass class
$m_{\min}$	lower bound of mass in [amu] (0.5 amu)
$m_{\max}$	upper bound of mass in [amu] (95.0 amu)

Equations (1) and (6) can be combined to

$$NM = B_1 + B_2 \cdot x + B_3 \cdot y + B_4 \cdot x \cdot y + B_5 \cdot x^2 + B_6 \cdot y^3 \quad (8)$$

where

$$B_1 = 1 + (A_1 - \ln(m_{\min})) / \ln(k_4)$$

$$B_2 = A_2 / \ln(k_4)$$

$$B_3 = A_3 / \ln(k_4)$$

$$B_4 = A_4 / \ln(k_4)$$

$$B_5 = A_5 / \ln(k_4)$$

$$B_6 = A_6 / \ln(k_4)$$

NM is the mass class between and including 1 and NMAX

All events are checked for mass-, time-of-flight- and energy over/underflow. For these, special ‘mass classes’ are reserved :

Mass class	Event
59	mass overflow : $m \geq m_{\max}$
60	mass underflow : $m \leq m_{\min}$
61	energy overflow : $E_m \geq E_{\max}$
0	energy underflow (i.e. MASS ZERO) : $E_m \leq E_{\min}$
62	time-of-flight underflow : $T_m \leq T_{\min}$
63	time-of-flight overflow : $T_m \geq T_{\max}$

Tabl4 4 : STICS over/underflow mass classes

So, whenever an event falls into the window given by  $E_{\max}$ ,  $E_{\min}$ ,  $T_{\max}$  and  $T_{\min}$  it will be classified as given by equation 8. If this results in a mass class above 58 or below 1, the event will be classified as mass overflow (mass class 59) or mass underflow (mass class 60)

The following table gives the relations between the coefficients of the mass equations and the variables and their format in which the values are actually stored in the DPU. Also given is the parameter number for the **D\_PARLDA** command to load the variables.

Coefficient	Variable	Format	Parameter #	Default
$B_1$	rB1	signed 16.16 fix point	11	38.462073
$B_2$	rB2	signed 16.16 fix point	11	-9.327289
$B_3$	rB3	signed 16.16 fix point	11	-26.31096
$B_4$	rB4	signed 16.16 fix point	11	4.263013
$B_5$	rB5	signed 16.16 fix point	11	0.567229
$B_6$	rB6	signed 16.16 fix point	11	0.762857
EADC	rSEADK	signed 16.16 fix point	12	???
ln(EADC)	rLnEADK	signed 16.16 fix point	12	???
TADC	rSTADK	signed 16.16 fix point	12	???
ln(TADC)	rLnTADK	signed 16.16 fix point	12	???
EOC	iSNMEOC	signed 16 bit integer	13	???
TOC	iSNMTOC	signed 16 bit integer	13	???
NMAX	iSNMMaxClas	signed 16 bit integer	14	58
$E_{\min}$	rSEMin	signed 16.16 fix point	21	0.0 keV
$E_{\max}$	rSEMax	signed 16.16 fix point	21	3030 keV
$T_{\min}$	rSTMin	signed 16.16 fix point	21	0 nSec
$T_{\max}$	rSTMax	signed 16.16 fix point	21	409.2 nSec

Table 5 : STICS mass class alterable parameters

### 2.1.2 Mass per Charge classification

The mass per charge classification uses the equation

$$\ln(mq) = \ln(C_1) + \ln(D_1 \cdot D_2^S - C_2) + 2 \cdot \ln(T_m) \quad (9)$$

where

$m_q$	is the mass/charge in [amu/e]
$\ln(C_1)$	constant, see Table 6 for default
$C_2$	if $m_q < C2\_bound$ , $C2 = C2\_1$ , otherwise $C2\_2$ , see Table 6 for defaults
$T_m$	as defined for equation 5
$S$	the deflection voltage step number (0 ... 31)
$D_1$	constant, see Table 6 for default
$D_2$	constant, see Table 6 for default

The mass per charge ( $m/q$ ) is mapped onto a logarithmically spaced mass-per-charge-class axis by the equation

$$m_q = m_{q_{min}} \cdot k_2^{(NQ-1)} \quad (10)$$

$$k_2 = (m_{q_{max}}/m_{q_{min}})^{1/NQMAX} \quad (11)$$

$m_q$	is the mass per charge in [amu/e]
$NQ$	is the mass per charge class (1 .. $NQMAX$ )
$NQMAX$	is the highest mass-per-charge class (= 126)
$m_{q_{min}}$	lower bound of mass-per-charge in [amu/e] (= 0.5 amu/e)
$m_{q_{max}}$	upper bound of mass-per-charge in [amu/e] (= 60 amu/e)

Equations (9) and (10) can be combined to

$$NQ = E_1 + E_2 \cdot \ln(D_1 \cdot D_2^S - C_2) + E_3 \cdot \ln(T_m) \quad (12)$$

where

$$E_1 = 1 + (\ln(C_1) - \ln(m_{q_{min}})) / \ln(k_2)$$

$$E_2 = 1 / \ln(k_2)$$

$$E_3 = 2 / \ln(k_2)$$

The following table gives the relations between the coefficients of the mass equations and the variables and the format in which the values are actually stored in the DPU. Also given is the parameter number for the **D\_PARLDA** command to load the variables.

<b>Coefficient</b>	<b>Variable</b>	<b>Format</b>	<b>Parameter #</b>	<b>Default</b>
ln(C <sub>1</sub> )				-10.86274
E <sub>1</sub>	dwE1	signed 16.16 fix point	16	-266.649566
E <sub>2</sub>	dwE1	signed 16.16 fix point	16	26.318612
E <sub>3</sub>	dwE1	signed 16.16 fix point	16	52.637224
D <sub>1</sub>	dwD1	signed 16.16 fix point	16	7.97
D <sub>2</sub>	dwD2	signed 16.16 fix point	16	1.116
C <sub>2_1</sub>	dwC2_1	signed 16.16 fix point	15	1.5
C <sub>2_2</sub>	dwC2_2	signed 16.16 fix point	15	4.0
C <sub>2_bound</sub>	wSNQ_C2Bound	unsigned 16 bit integer	15	11

Table 6 : STICS mass/charge classification alterable parameters

Note that for the mass-per-charge classification there is no special over/underflow check.

### 2.1.3 Species classification

Table 7 gives the default definition list of the (rectangular) areas defined in the mass vs. mass-per-charge class plane for the science bins. Because the areas are rectangular, they are often also referred as boxes. The definition table can be changed by setting up an appropriate box definition with the **D\_PARLDA 30** command and copying that definition to the list using the **D\_DIGCMD 42**. Finally the new definition list can be used to overwrite the old classification scheme by the **D\_DIGCMD 17** command.

<b>Bin No.</b>	<b>Species</b>	<b>Logic</b>	<b>mass range</b>	<b>mass class range</b>	<b>m/q range</b>	<b>m/q class</b>
112	D1			3 60		0 127
113	D2			0 2		0 127
114	D3			1 18		11 26
115	D4			18 30		31 61
116	D5			32 57		32 66
117	D6			31 57		67 80
118	D7			24 58		84 99
119	D8			28 56		105 119



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						<u>Processing</u>	
22	MOVER		59	59		0	127
23	MUNDER		60	60		0	127
24	EUNDER		61	61		0	127
25	TUNDER		62	62		0	127
26	TOVER		63	63		0	127

										Processing
16	HR0	H+	0.60	2.20	3	16	0.80	1.25	13	24
17	HR1	O+	5.00	80.00	26	56	14.95	20.30	90	97
18	SMR0	He+	2.70	6.50	20	28	3.55	4.65	53	59
19	SMR1	He+2	2.70	6.50	20	28	1.70	2.30	33	40
20	SMR2	O+2	9.00	30.00	33	45	7.70	9.20	73	77
32	MR0	C+3	9.70	13.60	34	37	3.80	4.40	54	57
33	MR1	C+4	9.50	13.60	34	37	2.85	3.20	47	49
34	MR2	C+5	9.50	13.60	34	37	2.25	2.55	41	43
35	MR3	C+6	9.50	13.60	34	37	1.85	2.15	35	38
36	MR4	N+	5.00	50.00	26	51	12.50	14.95	86	89
37	MR5	N+	0.00	0.00	MASS ZERO		11.50	14.95	84	89
38	MR6	N+2	9.00	23.00	33	42	6.60	7.70	69	72
39	MR7	N+2	0.00	0.00	MASS ZERO		6.60	7.70	69	72
40	MR8	H+	0.00	0.00	MASS ZERO		0.80	1.25	13	24
41	MR9	O+	0.00	0.00	MASS ZERO		14.95	20.30	90	97
42	MR10	He+	0.00	0.00	MASS ZERO		3.55	4.65	53	59
43	MR11	O+2	0.00	0.00	MASS ZERO		7.70	9.70	73	78
44	MR12	O+3	12.70	20.00	37	41	4.95	5.95	61	65
45	MR13	O+4	13.60	20.00	38	41	3.70	4.40	54	57
46	MR14	O+5	13.60	20.00	38	41	3.00	3.40	48	50
47	MR15	O+6	11.00	20.00	35	41	2.55	2.85	44	46
48	MR16	O+7	13.90	20.00	38	41	2.15	2.45	39	42
49	MR17	O+8	13.90	20.00	38	41	1.80	2.10	35	38
50	MR18	Ne+8	17.80	22.10	40	42	2.30	2.55	41	43
51	MR19	MgSi1	22.10	39.00	43	48	2.15	3.29	39	50
52	MR20	MgSi1	22.10	39.00	43	48	3.29	5.95	51	65
53	MR21	Fe6,7	39.00	75.00	49	55	7.40	9.80	72	78
54	MR22	Fe8,9	39.00	75.00	49	55	5.83	7.40	66	71
55	MR23	Fe10,11	39.00	75.00	49	55	4.82	5.83	61	65
56	MR24	Fe12,13	39.00	75.00	49	55	4.10	4.82	56	60
57	MR25	Fe14,15	39.00	75.00	49	55	3.57	4.10	53	55
58	MR26	Fe16,17	39.00	75.00	49	55	3.06	3.57	49	52
59	MR27	NO+O2+	7.00	72.00	30	55	28.00	42.00	107	117
60	MR28	MO+O2+	0.00	0.00	MASS ZERO		28.00	60.00	107	126
61	MR29	He+2	0.00	0.00	MASS ZERO		1.60	2.30	32	40

Table 7 : STICS science rate bins in M vs. M/Q space

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The  $D_1$  to  $D_8$  “species” surround the physical species and were implemented for debugging purposes. This is the same for the MOVER, MUNDER, EOVER, TUNDER and TOVER bins which represent counting rates for mass over/underflow, energy overflow and time-of-flight over/underflow. These “diagnostic rates” are accumulated over one science record in the DPU and spilled out once per science record.

Figure 10 shows the species boxes defined in this table in the N vs NQ space.

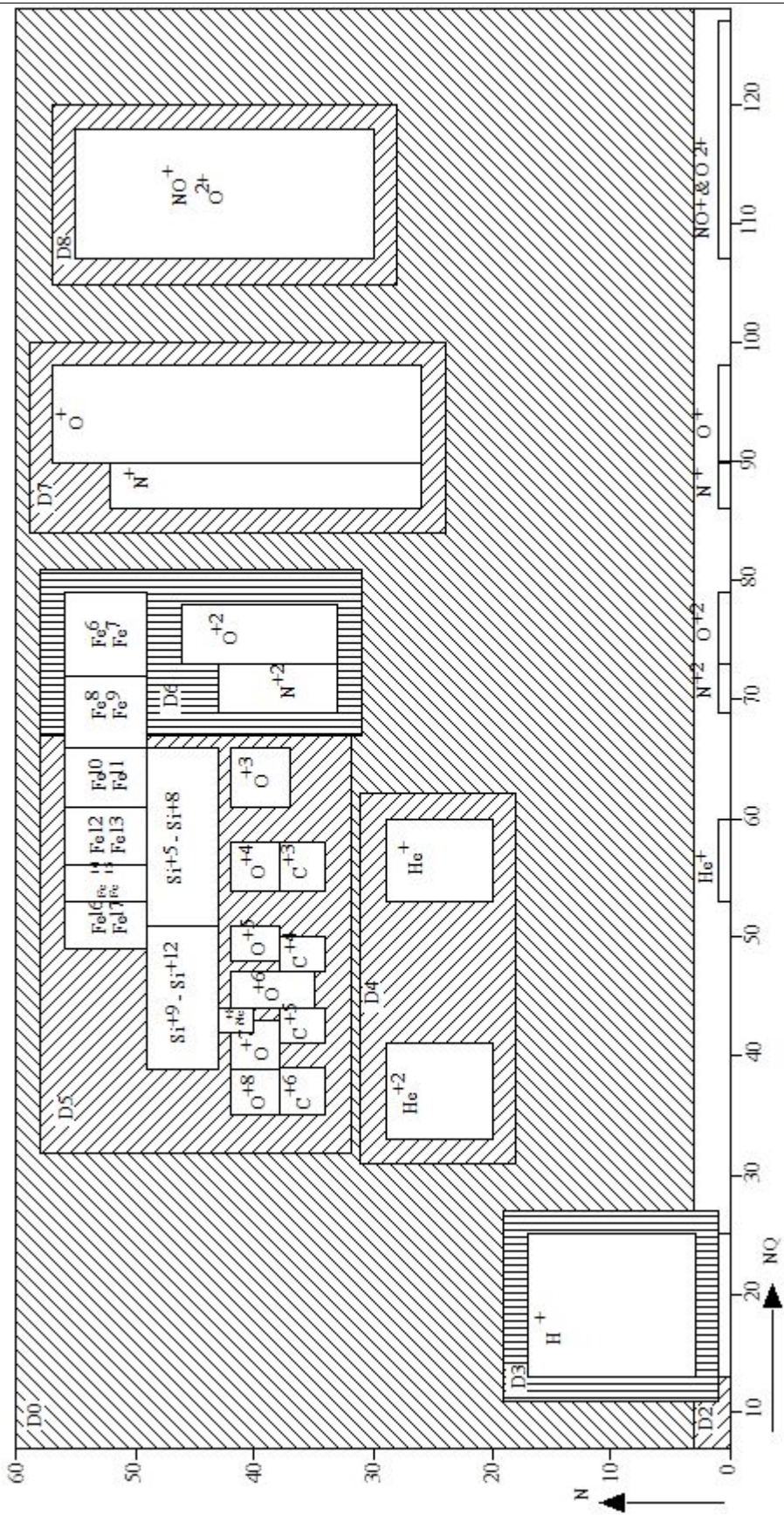


Fig 10 : STICS mass bins

### 2.1.4 PHA data collection

The DPU transmits 47 event word samples in each EDB. These event words are selected from three of four possible basic bins defined in the mass vs. mass-per-charge class plane. Each of these four bins (called “PHA ranges”) is a union of one or more rectangular areas. They are defined in a list similar to the box definition list for the science rate bins.

Since the DPU can’t transmit **every** event which falls into one of the defined PHA ranges, the total number of events which fall into each range are accumulated in the basic bins.

The following is the content of the default basic bin box definition table.

Range	Species	mass range [amu]		mass class range		m/q range [amu/e]		m/q class range	
0	P001	8.16	95.00	32	58	1.47	10.85	29	81
	P002	0.00	0.00	0	0	5.48	10.85	64	81
1	P101	1.78	8.16	15	31	1.45	10.85	29	81
	P102	0.00	0.00	0	0	1.45	5.48	29	63
2	P201	0.00	95.00	0	58	10.85	60.00	82	126
3	P301	0.00	95.00	0	58	0.50	1.45	1	28
	P302	0.50	1.78	1	14	1.45	10.85	29	81

Table 8 : STICS PHA & basic rate ranges in M vs. M/Q space

Due to limited data rate, only three of the four defined bins can be active at a given time. By default, the PHA ranges 0 - 2 are active and associated with the basic bins 0 - 2, respectively. This assignation can be changed with the **S\_RANGE** command.

The DPU will try to transmit one PHA event word from every sector and every active PHA range in a spin, leaving out the last range in sector 15, which sums up to 47 PHA event words per spin as mentioned above. If not enough PHA event words for some sector/range combination were received from the sensor, the rest is filled with event words from other sectors or ranges. Each PHA event word is 32 bits long and is coded as follows :

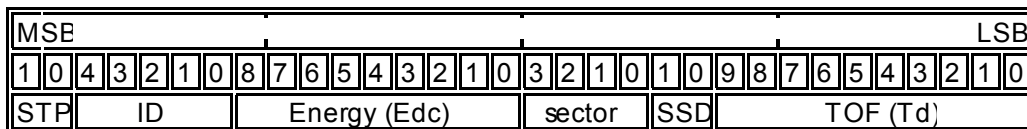


Fig 11 : STICS PHA event word format

Here,

$$ID = START * 3 + RANGE$$

where START is the START ID (0..9) and RANGE (0..2) is the basic rate bin number of the area in M vs. M/Q the event fell into.

$E_{dc}$  is obtained by compressing the 10-bit value  $E_d$  to 9 bits according to the following algorithm :

if  $E_d < 256$

$$E_{dc} = E_d$$

else

$$E_{dc} = E_d / (\text{int}(I_d(E_d)) - 6)$$

### 2.1.5 Classification implementation in the DPU

The EPIC DPU does not calculate the given formulas above each time it receives a valid event word. Instead it uses a look-up technique based on linear tables to classify the incoming events. Figure 12 shows the basic table structure implemented in the DPU.

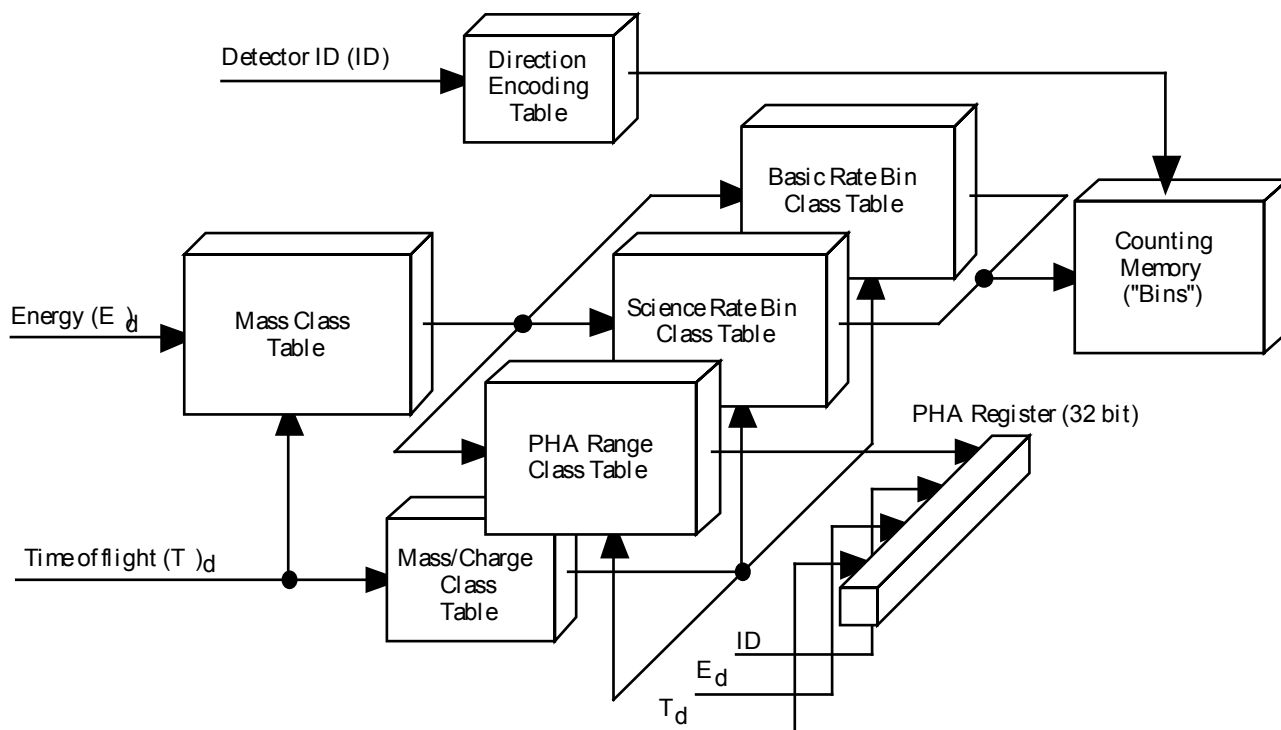


Fig 12 : Table structure for STICS event classification

The digital energy and time-of-flight values address a two-dimensional mass classification table, which delivers a mass class N at its output. This table is built during DPU initialization and by command (see **D\_DIGCMD**) using equations (2 - 6).

The time-of-flight value also addresses a one-dimensional mass-per-charge table, which delivers a mass-per-charge class NQ at its output. This table is built during DPU initialization using equations (12,5) and is updated once per spin depending on the current deflection voltage step S.

The mass class and the mass-per-charge class values address two two-dimensional tables (i.e. the mass vs. mass-per-charge space), the science bin and the basic rate bin classification table to look-up the bin numbers. A table with contents similar to the basic bin table is used to decide whether the event falls into one of the basic bins and is worth being classified as a PHA word.

These three tables are painted with rectangular areas of bin numbers which address the respective bin counters in the counting memory. Whereas the science bin table has its own defined boxes, the boxes drawn in the basic bin table are the same as in the PHA bin table.

The boxes are painted according to two box definitions lists starting with the first and ending with the last entry. Therefore, choosing a special ordering scheme in the definition lists, boxes can overlap each other. Table 7 showed the default definition list for the science bin table, Table 8 showed the definition list for the PHA ranges and basic bins.

The detector ID (containing START-, STOP- and SSD-ID, see Figure 12, addresses a one dimensional table which encodes the given information into six possible directions and one “invalid ID direction”.

Using two consecutive classification cycles, the bin numbers gained from the science bin classification table and from the basic bin classification table are used, together with the direction code, to address and increment the appropriate bin counters in the counting memory. The rates from the counting memory are read, reset and processed by the DPU processor on a cyclic basis.

It must be noted that figure 4 does not present every detail of the classification process. Especially, the energy compression table is not displayed. This one-dimensional table is used to compress the received 10 bit value for  $E_d$  to an 8 bit value. This lowers the needed size for the mass classification table to 256 kB instead of 1 MB of memory.

The logarithmic compression scheme is defined below.

$$\begin{aligned}
 &\text{if } E_d < 96 \\
 &\quad E_c = E_d \\
 &\text{else} \\
 &\quad E_c = \text{int}( E_d/2^L ) + 48 \cdot L \\
 &\quad \text{where } L = \text{int}( \log_2(E_d/48) )
 \end{aligned} \tag{13}$$

## 2.2 ICS Instrument

The event data transmitted by the ICS instrument to the DPU has the following format :

9	8	7	6	5	4	3	2	1	0	9	8	7	6	5	4	3	2	1	0	0	0	6	5	4	3	2	1	0
TOF( $T_d$ )										Energy( $E_d$ )										H								

Fig 13 : ICS event word

The DPU classifies the time-of-flight, the energy and the mass of the received events into different bins. The H identifier is used to differentiate between the north ( $H = 0$ ) and the south ( $H = 1$ ) telescope (“head”) of the ICS instrument. H is also often referred to as the ICS “head id”.

### 2.2.1 Mass classification

The mass classification uses the equation

$$\ln(m) = A_1 + A_2 \cdot x + A_3 \cdot y + A_4 \cdot x \cdot y + A_5 \cdot x^2 + A_6 \cdot y^3 \quad (14)$$

$$x = \ln(E_m) \quad (15)$$

$$y = \ln(T_m) \quad (16)$$

$$E_m = (E_d - EOC) / EADC \quad (17)$$

$$T_m = (T_d - TOC) / TADC \quad (18)$$

where :

- m is the mass in [amu]
- $E_m$  is the measured Energy in [keV]
- $T_m$  is the measured time-of-flight in [ns]
- $E_d$  is the digital energy contained in the event word in [channel] (0..1023)
- $T_d$  is the digital time-of-flight contained in the event word in [channel] (0..1023)
- EOC is the conversion offset of the energy analog-to-digital (ADC) converter of the instrument analog electronics (AE) in [channel]
- EADC is the energy A/D conversion factor of the AE ADC in [channel / keV]
- TOC is the conversion offset of the time-of-flight ADC of the instrument analog electronics in [channel]
- TADC is the time-of-flight A/D conversion factor of the AE ADC in [channel / ns]
- $A_1 - A_6$  are the polynomial coefficients with default values shown in Table 15.

The mass is classified into 4 ranges and the mass under/overflow ranges. Each of the 4 mass ranges itself is divided into several subranges (the ICS mass bins) with respect to the energy.

The mass ranges are defined as follows



mass [amu]		range
>	<	name
0	0.5	mass underflow
0.5	2.5	Protons
2.5	8	Helium
8	21	Medium
21	100	Heavies (Na - Fe)
100	$\infty$	mass overflow

Table 9 : ICS mass ranges

The Protons (Pi), Heliums (HEi), Mediums (Mi) and Heavies (Hi) are subdivided into mass bins according to the following tables.

Energy [keV]		range	bin
>	<	name	no
20.00	31.70	P1	0
31.70	50.30	P2	1
50.30	79.80	P3	2
79.80	126.50	P4	3
126.50	200.60	P5	4
200.60	318.10	P6	5
318.10	504.50	P7	6
504.50	800.00	P8	7
800.00	1550.00	P9	8
1550.00	3000.00	P10	9

Table 10 : ICS Proton bins

Energy [keV]		range	bin
>	<	name	no
20.00	31.70	HE1	10
31.70	50.30	HE2	11
50.30	79.80	HE3	12
79.80	126.50	HE4	13
126.50	200.60	HE5	14
200.60	318.10	HE6	15
318.10	504.50	HE7	16
504.50	800.00	HE8	17
800.00	1550.00	HE9	18
1550.00	3000.00	HE10	19

Table 11 : ICS Helium bins

Energy [keV]		range	bin
>	<	name	no
20.00	33.00	M1	20
33.00	55.00	M2	21
55.00	90.00	M3	22
90.00	148.00	M4	23
148.00	245.00	M5	24
245.00	404.00	M6	25
404.00	667.00	M7	26
667.00	1100.00	M8	27
1100.00	1820.00	M9	28
1820.00	3000.00	M10	29

Table 12 : ICS Medium bins

Energy [keV]		range	bin
>	<	name	no
20.00	120.00	H1	30
120.00	228.00	H2	31
228.00	435.00	H3	32
435.00	830.00	H4	33
830.00	1575.00	H5	34
1575.00	3000.00	H6	35

Table 13 : ICS Heavies bins

All events are checked for mass-, time-of-flight- and energy over/underflow. For this, special “mass” bins are reserved :

<b>bin</b>	<b>condition</b>
<b>no</b>	
36	mass underflow
37	mass overflow
42	Energy underflow ( $E_m < E_{\min}$ )
43	Energy overflow ( $E_m \geq E_{\max}$ )
44	Time-of-flight underflow ( $T_m < T_{\min}$ )
45	Time-of-flight overflow ( $T_m \geq T_{\max}$ )

Table 14 : ICS over/underflow bins

The following table gives the relations between the coefficients of the mass equations and the variables and their format in which the values are stored. Also given is the parameter number for the **D\_PARLDA** command to load the variables.

<b>Coefficient</b>	<b>Variable</b>	<b>Format</b>	<b>Parameter #</b>	<b>Default</b>
A <sub>1</sub>	rA1	signed 16.16 fix point	0	-5.70969
A <sub>2</sub>	rA2	signed 16.16 fix point	0	0.188562
A <sub>3</sub>	rA3	signed 16.16 fix point	0	0.634870
A <sub>4</sub>	rA4	signed 16.16 fix point	0	0.134778
A <sub>5</sub>	rA5	signed 16.16 fix point	0	0.0394281
A <sub>6</sub>	rA6	signed 16.16 fix point	0	0.0381063
EADC	rEADC	signed 16.16 fix point	1	???
ln(EADC)	rEADCLN	signed 16.16 fix point	1	???
TADC	rTADC	signed 16.16 fix point	2	???
ln(TADC)	rTADCLN	signed 16.16 fix point	2	???
EOC	iEOC	signed 16 bit integer	3	0.0
TOC	iTOC	signed 16 bit integer	3	???

Table 15 : ICS mass classification parameters

### 2.2.2 TOF classification

The time-of-flight is classified into 16 bins plus two over/underflow bins according to the following table.

Time-of-flight[ns]		range name	bin no	Memory Address	Memory Contents					
>	<				0 (LSB)	1	2	3 (MSB)	4 (BIN)	5
0	$T_{\min}$	T0	39	19AAh	00h	00h	00h	00h	27h	00h
$T_{\min}(= 2.0)$	3.5	T1	62	19B0h	00h	00h	02h	00h	3Eh	00h
3.5	6.0	T2	63	19B6h	00h	80h	03h	00h	3Fh	00h
6.0	7.2	T3	64	19BCh	00h	00h	06h	00h	40h	00h
7.2	8.8	T4	65	19C2h	33h	33h	07h	00h	41h	00h
8.8	10.7	T5	66	19C8h	CDh	CCh	08h	00h	42h	00h
10.7	12.9	T6	67	19CEh	33h	B3h	0Ah	00h	43h	00h
12.9	15.7	T7	68	19D4h	66h	E6h	0Ch	00h	44h	00h
15.7	19.0	T8	69	19DAh	33h	B3h	0Fh	00h	45h	00h
19.0	23.0	T9	70	19E0h	00h	00h	13h	00h	46h	00h
23.0	27.8	T10	71	19E6h	00h	00h	17h	00h	47h	00h
27.8	33.7	T11	72	19ECh	CDh	CCh	1Bh	00h	48h	00h
33.7	40.9	T12	73	19F2h	33h	B3h	21h	00h	49h	00h
40.9	49.5	T13	74	19F8h	66h	E6h	28h	00h	4Ah	00h
49.5	60.0	T14	75	19FEh	00h	80h	31h	00h	4Bh	00h
60.0	77.0	T15	76	1A04h	00h	00h	3Ch	00h	4Ch	00h
77.0	$T_{\max}$	T16	77	1A0Ah	00h	00h	4Dh	00h	4Dh	00h
$T_{\max}(= 100.0)$	$\infty$	T17	41	1A10h	00h	00h	64h	00h	29h	00h

Note: Memory Contents 0 to 3 contain the TOF boundary in keV, expressed in 16.16 format

Table 16 : ICS time of flight bins

$T_{\min}$  and  $T_{\max}$  can be calculated from  $T_{d\min}$  and  $T_{d\max}$  using equation 18.

### 2.2.3 Energy classification

The energy is classified into 16 bins plus two over/underflow bins according to the following table.

Energy [keV]		range	bin	Memory	Memory Contents					
>	<	name	no	Address	0 (LSB)	1	2	3 (MSB)	4 (BIN)	5
0	$E_{\min}$	E0	38	193Eh	00h	00h	00h	00h	26h	00h
$E_{\min}(= 20.0)$	26.5	E1	46	1944h	00h	00h	14h	00h	2Eh	00h
26.5	35.0	E2	47	194Ah	00h	80h	1Ah	00h	2Fh	00h
35.0	46.8	E3	48	1950h	00h	00h	23h	00h	30h	00h
46.8	62.0	E4	49	1956h	CDh	CCh	2Eh	00h	31h	00h
62.0	82.5	E5	50	195Ch	00h	00h	3Eh	00h	32h	00h
82.5	109.5	E6	51	1962h	00h	80h	52h	00h	33h	00h
109.5	145.4	E7	52	1968h	00h	80h	6Dh	00h	34h	00h
145.4	193.0	E8	53	196Eh	66h	66h	91h	00h	35h	00h
193.0	256.0	E9	54	1974h	00h	00h	C1h	00h	36h	00h
256.0	340.0	E10	55	197Ah	00h	00h	00h	01h	37h	00h
340.0	452.0	E11	56	1980h	00h	00h	54h	01h	38h	00h
452.0	600.0	E12	57	1986h	00h	00h	C4h	01h	39h	00h
600.0	900.0	E13	58	198Ch	00h	00h	58h	02h	3Ah	00h
900.0	1340.0	E14	59	1992h	00h	00h	84h	03h	3Bh	00h
1340.0	2006.0	E15	60	1998h	00h	00h	3Ch	05h	3Ch	00h
2006.0	$E_{\max}$	E16	61	199Eh	04h	00h	D6h	07h	3Dh	00h
$E_{\max}(= 3000.0)$	$\infty$	E17	40	19A4h	00h	00h	B8h	0Bh	28h	00h

Note: Memory Contents 0 to 3 contain the Energy boundary in keV, expressed in 16.16 format

Table 17 : ICS energy bins

### 2.2.4 PHA data collection

The EPIC DPU can collect ICS PHA data in two different modes : a (rotating) priority mode and a fifo mode. Each of these modes will be explained in detail now. The DPU can be switched between these two modes using the **I\_DIGCMD 10** command.

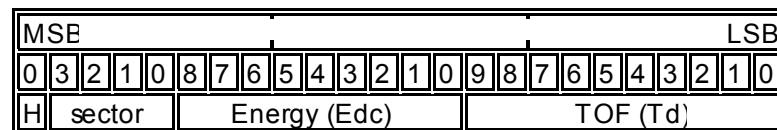


Fig 14 : ICS PHA event word format

### 2.2.4.1 Priority mode

In priority mode, the mass bins of received particles are subdivided into 4 different energy levels and four different mass levels (the P, HE, M and H ranges). There are 16 possible combinations of energy and mass levels, which are the ICS PHA ranges.

For each 2 spin period, the DPU tries to collect up to 3 event words from each PHA range and each sector, so a maximum of  $3*16*16 = 768$  PHA words are collected. To get an equal distribution over heads, the DPU will not accept more than 2 event words from either head for each sector and PHA range. The collected PHA words are stored in internal buffers.

Since only 48 PHA words can be transmitted every 2nd spin, the 4 different energy levels and the 4 mass levels are assigned different priorities in every 2nd spin and the DPU will always try to transmit high priority PHA words before others. The mass level priority rotates every 2nd spin and wraps around after 2 spins \* 4 priorities = 8 spins. Therefore, the energy level rotates every 8th spin such that all possible combinations are looped through within 8 spins \* 4 priorities = 32 spins, which is called a science record.

In every 2nd spin, the DPU tries to transmit 48 PHA words, 3 of each sector, from the presently highest priority PHA range. If there were not enough events collected in that range, events are taken from the range with the next-to-the-highest priority and so on.

Using the I\_PR\_OVR command, it is possible to stop priority rotation for mass and/or energy levels, so that high visibility can be given to any of the defined mass and/or energy levels.

The documentation for the I\_PR\_OVR command will give some additional information on this topic and shows which mass bins are assigned to the different PHA ranges.

### 2.2.4.2 Fifo mode

During fifo mode, there is no differentiation between PHA ranges. The DPU will store the first 48 event words it receives each sector, so a maximum of  $48*16 = 768$  PHA words are received during 2 spins.

Every 2nd EDB, the DPU chooses the events to place in the telemetry stream by looping through the 16 sector buffers as often as it needs to fill the available telemetry space of 48 PHA words. The first loop would choose the first event received in every sector (if one was received), the second loop the second event and so on. So, if during every sector at least 3 events were received, the events would be equally distributed over sectors.

## **2.2.5 Classification implementation in the DPU**

To classify an event by species, the EPIC DPU does not calculate equations (14-18) each time it receives a valid event word. Instead, a table-based look-up technique is used to classify the incoming events. Figure 15 shows the basic table structure implemented in the DPU.



### **3. TELEMETRY**

#### **3.1 The GEOTAIL telemetry system**

The GEOTAIL S/C provides two telemetry channels. They are called Editor A and Editor B. Editor A is the real time telemetry data link and transmits data with 64 kBit/sec. Editor B is the recorded telemetry and transmits data with 16 kBit/sec. The telemetry data is subdivided into *frames* of 128 data words (bytes) which are numbered from 0 to 255 and wrap around to 0 after 255. GEOTAIL assigns different format modes to each editor depending on the S/C Operational Mode. GEOTAIL knows 13 possible format modes for each telemetry.

The following table shows the different editor format mode used during the various S/C operational mode.

<b><u>Operational Mode</u></b>	<b><u>Editor A</u></b>	<b><u>Editor B</u></b>
Nominal mode	Format 2, 65 kbps	Format 1, 16 kbps
AOCS mode	Format 2, 65 kbps	Format 0, 16/65 kbps
RAM CHK mode	Format 4 ..13	Format 1, 16 kbps or Format 0, 16/65 kbps
Contingency mode	Format 2/3 65 kbps	off
Emergency mode	off	Format 0, 256 bps

Table 18 : Telemetry format modes

The allocated amount of data words for each experiment in every frame depends on the S/C operational mode, to speak exactly : it depends on the format mode of each telemetry. However, there are some additional data bytes which are allocated to each experiment independent of telemetry format mode. These data words reflect the coarse status of the experiments.

#### **3.2 EPIC data contained in telemetry stream**

The following tables shows how much space for scientific data was allocated for EPIC. Then the next table shows which format mode independent data words EPIC has allocated.



<u>Format Mode</u>	<u>Editor A</u>	<u>Editor B</u>
0	-	-
1	-	20 bytes/frame
2	-	-
3	5 bytes/frame	-
4 - 11	-	-
12	3 bytes/frame address data + 64 bytes/frame RAM CHECK data	-
13	-	-

Table 19 : EPIC format dependent telemetry allocation

The science data transmitted in format 1 and 3 must be concatenated by the ground software to blocks of 960 bytes. Such a block is called an experiment data block (EDB). The start of an EDB can be identified by two header bytes which contain the values 14H and 6FH.

The next table shows which format-mode-independent data bytes EPIC has allocated.

Frame #	Word #	description
$32*n+27$	8,9,10	experiment status area 1 (S/W generated), details see next subsection
$32*n+28$	8,9,10	experiment status area 2 (S/W generated), details see next subsection
$32*n+12$	10	BC answer (H/W generated), this bytes reflects the last block command code sent to the DPU.
167	8,9	program address (S/W generated), this 16 bit word reflects the lower 16 bits of the current program address (set by the D_PRDADR command). The high byte is sent in word # 8, the low byte is sent in word # 9

128*n+59	11	EPIC-D Temp (H/W generated), DPU temperature sensor, digitized by S/C, range [0..255]. Conversion factor: Degrees C = 1.3028 * value - 143.5
128*n+60	11	EPIC-S Temp (H/W generated), STICS temperature sensor, digitized by S/C, range [0..255]. Conversion factor: Degrees C = 1.3028 * value - 150.5
128*n+61	11	EPIC-I Temp (H/W generated), ICS temperature sensor, digitized by S/C, range [0..255]. Conversion factor: Degrees C = 1.3028 * value - 152.0
24	11	+5V Current (H/W generated), +5V DPU logic supply current, digitized by S/C, range [0..255]. Conversion factor: I[mA] = 4.08 * value
152	11	+29V Current (H/W generated), DPU-gated +29V instrument supply current, digitized by S/C, range [0..255]. Conversion factor: I[mA] = 4.08 * value

Table 20 : EPIC format independent telemetry allocation

### 3.3 Experiment status areas

The experiment status areas (together 6 bytes every 32 frames) are used to transmit the power status data, the subcommutated housekeeping data and the DC (discrete command) answer.

How EPIC uses these 6 bytes can be seen from the table 21.

	<b>Bit</b>	<b>ITEM</b>	<b>Source</b>
BYTE1	7	EPIC DPU POWER	MREG2(7)
	6	EPIC BAKE HEATERS	MREG2(6)
	5	STICS SUPL HEATERS	MREG2(5)
	4	ICS SUPL HEATERS	MREG2(4)
	3	ICS MCP POWER	MREG2(3)
	2	STICS MCP POWER	MREG2(2)
	1	STICS DPPS POWER	MREG2(1)
	0	INSTRUMENT POWER	MREG2(0)

BYTE2	<b>Bit</b>	<b>ITEM</b>	<b>Source</b>
	7	STICS HVPS 6	adwSTICSAnsw[0](5)
	6	STICS HVPS 5	adwSTICSAnsw[0](4)
	5	STICS HVPS 4	adwSTICSAnsw[0](3)
	4	STICS HVPS 3	adwSTICSAnsw[0](2)
	3	STICS HVPS 2	adwSTICSAnsw[0](1)
	2	STICS HVPS 1	adwSTICSAnsw[0](0)
	1	ICS ANALOG POWER	MREG2(9)
0	STICS ANALOG POWER	MREG2(8)	
BYTE3	<b>Bit</b>	<b>ITEM</b>	<b>Source</b>
	7	STICS HVPS 7	adwSTICSAnsw[0](6)
	6	STICS + DPPS	adwSTICSAnsw[2](1)
	5	STICS - DPPS	adwSTICSAnsw[2](0)
	4	ICS HVPS 5	adwICSAnsw[0](4)
	3	ICS HVPS 4	adwICSAnsw[0](3)
	2	ICS HVPS 3	adwICSAnsw[0](2)
	1	ICS HVPS 2	adwICSAnsw[0](1)
0	ICS HVPS 1	adwICSAnsw[0](0)	
BYTE4	<b>Bit</b>	<b>ITEM</b>	<b>Source</b>
7 - 0	Subcom Index	bySubcomIdxA,bySubcomIdxB	
BYTE5	<b>Bit</b>	<b>ITEM</b>	<b>Source</b>
7 - 0	subcommutated housekeeping data	abyHKA[],abyHKB[]	
BYTE6	<b>Bit</b>	<b>ITEM</b>	<b>Source</b>
7 - 0	(BYTE4 & 07h) =	DC command buffer	
	0 : DC code, HVIS Answer, contains ABh if no DC is available		
	1 : not used		
	2 : not used		
	3 : not used		
	4 : not used		
	5 : not used		
	6 : not used		
	7 : not used		

Table 21 : EPIC status area contents

### 3.4 EDB

The science data are grouped into *experiment data blocks* (EDB) of 960 bytes each. This block length was chosen such that one EDB gets transmitted within 3 seconds, which is the nominal spin duration. An EPIC *science record* (SR) is defined as 32 EDBs (or spins). Within one science record all data and most of the housekeeping data gets transmitted once, therefore after 32 spins the data is consistent (except for some parameter downloads, which are sub-subcommutated)

The EDB is divided up into 60 lines of 16 bytes each. The contents vary with the instrument mode. Three different modes are implemented :

- dual sensor mode (default)
- ICS single sensor mode
- STICS single sensor mode

However, the basic structure of each EDB is the same for all modes as depicted in Figure 16. This figure shows the EDB structure for the dual sensor mode. If EPIC operates in one of the single sensor modes, the science data area of the idle instrument is assigned to the active instrument. The DPU Common Areas, however, don't change their position in the different modes.

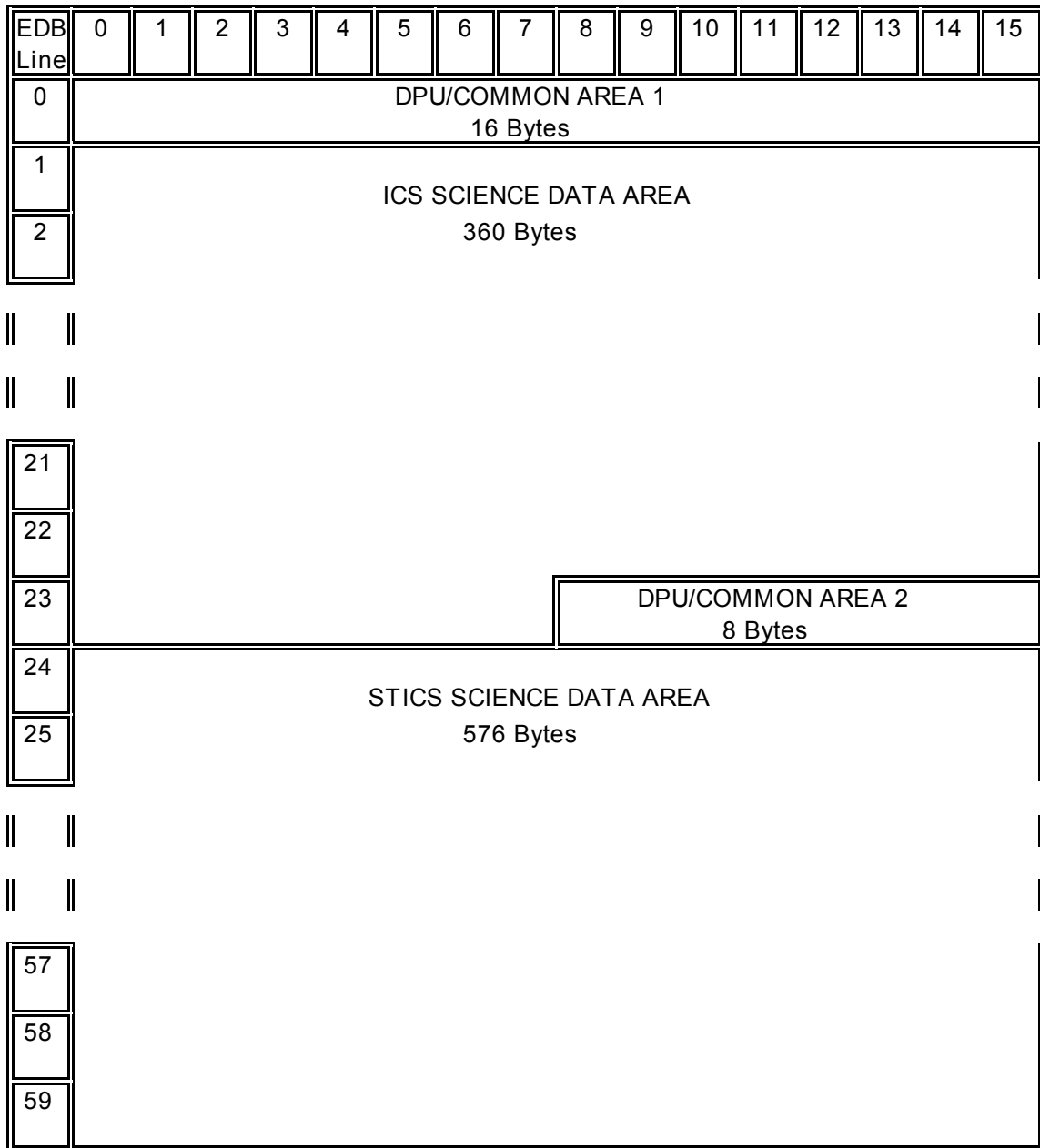


Fig 16 : General EDB layout

The following sections will document the contents of the mode independent and the mode dependent sections of the EDB in detail.

### 3.4.1 DPU common areas for all modes

EDB Line	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
0	14H	6FH														

Fig 17 : DPU common area 1

The DPU common area 1 contains the EDB identifier words, spin & EDB counters, subcommutated housekeeping data and the main power status. Some other useful items are also contained in here.

EDB Line	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	
23																	

Fig 18 : DPU common area 2

The DPU common area 2 is positioned between the data area for ICS & STICS in the dual sensor mode.

The next pages will give detailed information about the content of the DPU common areas

## DPU common area 1

## Bytes 0 and 1

Byte #	Bit #	Comment	
0	0	0	
	1	0	
	2	1	
	3	0	14 Hex Identifier
	4	1	
	5	0	
	6	0	
	7	0	
Source: ROM constant			
1	0	1	
	1	1	
	2	1	
	3	1	6F Hex Identifier
	4	0	
	5	1	
	6	1	
	7	0	
Source: ROM constant			

DPU common area 1

Bytes 2 and 3

Byte #	Bit #	Comment
0	0	LSB EDB Counter This byte increments for every EDB which was formatted in the DPU.
	1	It wraps around to 00H after FFH
	2	
	3	
	4	
	5	
	6	
	7	
Source: byEDBCount		
1	0	LSB Spin Counter This byte increments for every spin. It wraps around to 00H after FFH
	1	
	2	
	3	
	4	
	5	
	6	
	7	MSB
Source: wSpinNo.		



## DPU common area 1

## Bytes 4 and 5

Byte #	Bit #	Comment
4	0	LSB Measured Spin Counter
	1	This 5 bit item counts the measured spins of a science record. If it wraps around to 00H, a new science record starts.
	2	
	3	
	4	MSB Source: byMeasureSpinNo.
5	EPIC INSTRUMENT POWER "1" = ON "0" = OFF Source: MREG2 bit 0	
6	STICS LVPS "1" = ON "0" = OFF Source: MREG2 bit 8	
7	ICS LVPS "1" = ON "0" = OFF Source: MREG2 bit 9	
5	0	STICS STEP "1": STICS MCPPS stepping active Source: or'ed abySHVStepFlag [0..6],bit 5
	1	ICS STEP "1": ICS MCPPS stepping active Source: or'ed abyIHVStepFlag [0..4],bit 5
	2	HV ENABLE "1": HV is enabled "0": HV disabled Source: MREG2, bit 11
	3	CMD VAL "1" successful command execution Source: change of byValCmdCnt
	4	CMD ERR "1" error during command execution Source: change of byInvCmdCnt
	5	INVALID CMD "1" COI detected a command as invalid Source: change of byCOIInvCmdCnt
	6	Bit Value Bits 7,6,5 ... 0 are transmitted in this order
7	BYTE START Marks bit 7 of a long sequence data byte Source: ROM	

## DPU common area 1

## Bytes 6 and 7

Byte #	Bit #	Comment
6	0	LSB subcom index for subcommutated HK data in EDB. This byte contains the index of the HK data byte in byte 7 of the DPU common area 1.
	1	
	2	
	3	
	4	
	5	
	6	
	7	MSB
		Source: byEDBHKIdx
7	0	LSB HK data byte 0
	1	
	2	
	3	
	4	
	5	
	6	
	7	MSB
		Source: abyHKTelemBuf[byEDBHKIdx+0]

DPU common area 1

Bytes 8 and 9

Byte #	Bit #	Comment
8	0	LSB HK data byte 1
	1	
	2	
	3	
	4	
	5	
	6	
	7	MSB
Source: abyHKTelemBuf[byEDBHKIdx+1]		
9	0	LSB HK data byte 2
	1	
	2	
	3	
	4	
	5	
	6	
	7	MSB
Source: abyHKTelemBuf[byEDBHKIdx+2]		

DPU common area 1

Bytes 10 and 11

Byte #	Bit #	Comment
10	0	LSB HK data byte 3
	1	
	2	
	3	
	4	
	5	
	6	
	7	MSB
		Source: abyHKTelemBuf[byEDBHKIdx+3]
11	0	LSB HK data byte 4
	1	
	2	
	3	
	4	
	5	
	6	
	7	MSB
		Source: abyHKTelemBuf[byEDBHKIdx+4]

## DPU common area 1

## Bytes 12 and 13

Byte #	Bit #	Comment
12	0	LSB HK data byte 5
	1	
	2	
	3	
	4	
	5	
	6	
	7	MSB Source: abyHKTelemBuf[byEDBHKIdx+5]
13	0	STICS CMD STAT “0”: no errors “1”: command rejected in last spin Source: change of bySTICSCmdErr
	1	ICS CMD STAT “0”: no errors “1”: command rejected in last spin Source: change of byICSCmdErr
	2	STICS Actuator power 0 : off 1 : on
	3	Memory image 0 : disabled 1 : enabled
	4	bySensorMode LSB 0 dual sensor mode
	5	1 STICS single sensor mode MSB 2 ICS single sensor mode
	6	ICS Aperture motor 0 : still standing 1 : moving
	7	HK sync 1 : synchronized 0 : unsynchronized

## DPU common area 1

## Bytes 14 and 15

Byte #	Bit #	Comment
14	0	STICS north start MCP enable HVPS1 Source: adwSTICSAnsw[1] bit 8
	1	STICS equatorial start MCP enable HVPS2 Source: adwSTICSAnsw[1] bit 9
	2	STICS south start MCP enable HVPS3 Source: adwSTICSAnsw[1] bit 10
	3	STICS north stop MCP enable HVPS4 Source: adwSTICSAnsw[1] bit 11
	4	STICS equatorial stop MCP enable HVPS5 Source: adwSTICSAnsw[1] bit 12
	5	STICS south stop MCP enable HVPS6 Source: adwSTICSAnsw[1] bit 13
	6	STICS time of flight PS disable HVPS7 Source: adwSTICSAnsw[1] bit 14
	7	STICS negative DPPS enable Source: adwSTICSAnsw[2] bit 0
15	0	STICS positive DPPS enable Source: adwSTICSAnsw[2] bit 1
	1	STICS classification H/W Status 0 --> disabled Source: C_STAT Bit 0 1 --> running
	2	ICS classification H/W Status 0 --> disabled Source: C_STAT Bit 1 1 --> running
	3	ICS north stop MCP enable HVPS1 Source: adwICSAnsw[1] bit 0
	4	ICS north start MCP enable HVPS2 Source: adwICSAnsw[1] bit 1
	5	ICS south stop MCP enable HVPS3 Source: adwICSAnsw[1] bit 2
	6	ICS south start MCP enable HVPS4 Source: adwICSAnsw[1] bit 3
	7	ICS time of flight enable HVPS5 Source: adwICSAnsw[1] bit 4

## DPU common area 2

## Bytes 0 and 1

Byte #	Bit #	Comment
0	0	LSB Time Tag Source : byFrameCntB
	1	Time in # of frames (telemetry B) since last frame 0 on telemetry B when this EDB was started to be formatted.
	2	
	3	
	4	
	5	
	6	
	7	
1	0	STICS table calculation active 0 : not active 1 : active
	1	ICS table calculation active 0 : not active 1 : active
	2	LSB DPPS Step # of present spin (remember that the instrument data contained in this EDB is from the previous spin)
	3	
	4	
	5	
6	MSB	
7	0 Source: ROM constant	

## DPU common area 2

## Bytes 2 and 3

Byte #	Bit #	Comment
2	0	0 : no over current
		ICS A/E over current 1 : over current during last spin
	1	0 : no over current
		STICS A/E over current 1 : over current during last spin
	2	
	3	
	4	
	5	
6		
7		
3	0	
	1	
	2	
	3	
	4	
	5	
	6	
	7	



DPU common area 2

Bytes 4 and 5

Byte #	Bit #	Comment
4	0	
	1	
	2	
	3	
	4	
	5	
	6	
	7	
5	0	
	1	
	2	
	3	
	4	
	5	
	6	
	7	

DPU common area 2

Bytes 6 and 7

Byte #	Bit #	Comment
6	0	
	1	
	2	
	3	
	4	
	5	
	6	
	7	
7	0	
	1	
	2	
	3	
	4	
	5	
	6	
	7	

**3.4.2 Dual sensor mode**

In the dual sensor mode, the DPU common area 1 is followed by the ICS data area. The DPU common area 2 precedes the STICS data area.

**3.4.2.1 STICS data area**

EDE Line	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
24	HR0 0/0															HR0 0/1
25	HR0 1/0															HR0 1/1
26	HR0 2/0															HR0 2/1
27	HR0 3/0															HR0 3/1
28	HR0 4/0															HR0 4/1
29	HR0 5/0															HR0 5/1
30	HR1 0/0															HR1 0/1
31	HR1 1/0															HR1 1/1
32	HR1 2/0															HR1 2/1
33	HR1 3/0															HR1 3/1
34	HR1 4/0															HR1 4/1
35	HR1 5/0															HR1 5/1
36	SMR0 0/0							SMR0 0/7	SMR0 1/0							SMR 1/7
37	SMR0 2/0							SMR0 2/7	SMR0 0/0							SMR 0/7
38	SMR1 1/0							SMR1 1/7	SMR1 2/0							SMR 2/7
39	SMR2 0/0							SMR2 0/7	SMR2 1/0							SMR 1/7
40	SMR2 2/0							SMR2 2/7	BR0 0/0							BR0 0/7
41	BR0 1/0							BR0 1/7	BR0 2/0							BR0 2/7
42	BR1 0/0							BR1 0/7	BR1 1/0							BR1 1/7
43	BR1 2/0							BR1 2/7	BR2 0/0							BR2 0/7
44	BR2 1/0							BR2 1/7	BR2 2/0							BR2 2/7

Fig 19 : STICS data area (lines 24 – 44) in dual sensor mode

In the Figure above the HR, SMR and BR are tagged with the respective polar direction id (0..5) and the sector number (0..15). Keep in mind that the SMR and BR only differentiate between 3 polar directions and 8 sectors.

EDE Line	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
45	MR0	MR1	MR2	MR3	MR4	MR5	MR6	MR7	MR8	MR9	MR1	MR1	MR1	MR1	MR1	MR1
46	MR1	MR1	MR1	MR1	MR2	MR2	MR2	MR2	MR2	MR2	MR2	MR2	MR2	MR2	FSR	FSR
47	FSR	UFS	URS	RSR	RSR	RSR	DCR	DCR	DCR	TCR	TCR	TCR	SSD	SSD	SSD	MFS
48	MDC	MPF	MPR	DIA	PHA00			PHA01			PHA02					
49	PHA03			PHA04			PHA05			PHA06						
50	PHA07			PHA08			PHA09			PHA10						
51	PHA11			PHA12			PHA13			PHA14						
52	PHA15			PHA16			PHA17			PHA18						
53	PHA19			PHA20			PHA21			PHA22						
54	PHA23			PHA24			PHA25			PHA26						
55	PHA27			PHA28			PHA29			PHA30						
56	PHA31			PHA32			PHA33			PHA34						
57	PHA35			PHA36			PHA37			PHA38						
58	PHA39			PHA40			PHA41			PHA42						
59	PHA43			PHA44			PHA45			PHA46						

Fig 20 : STICS data area (lines 45 - 59) in dual sensor mode

3.4.2.1 ICS data area

EDB Line	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
1	A0-0/0															A0-0/1
2	A0-1/0															A0-0/1
3	A1-0/0															A1-0/1
4	A1-1/0															A1-0/1
5	B0-0/0															B0-0/7
6	B1-0/0															B1-0/7
7	C0-0/0															C0-0/1
8	C0-1/0															C0-0/1
9	C1-0/0															C1-0/1
10	C1-1/1															C1-1/1
11	C2-0/0															C2-0/1
12	C2-1/1															C2-1/1
13	C3-0/0															C3-0/1
14	C3-1/1															C3-1/1
15	C4-0/0															C4-0/1
16	C4-1/1															C4-1/1
17	C5-0/0															C5-0/1
18	C5-1/1															C5-1/1
19	C6-0/0															C6-0/1
20	C6-1/1															C6-1/1
21	C7-0/0															C7-0/1
22	C7-1/1															C7-1/1
23	"F"-Rates, "FA"-Rates, subcommutated with the Measured Spin Number															

Fig 21 : ICS data area (odd EDB) in dual sensor mode

EDB Line	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
1	PHA 0		PHA 1		PHA 2		PHA 3		PHA 4		PHA 5		PHA 6		PHA 7	
2	PHA 8		PHA 9		PHA 10		PHA 11		PHA 12		PHA 13		PHA 14		PHA 15	
3	PHA 16		PHA 17		PHA 18		PHA 19		PHA 20		PHA 21		PHA 22		PHA 23	
4	PHA 24		PHA 25		PHA 26		PHA 27		PHA 28		PHA 29		PHA 30		PHA 31	
5	PHA 32		PHA 33		PHA 34		PHA 35		PHA 36		PHA 37		PHA 38		PHA 39	
6	PHA 40		PHA 41		PHA 42		PHA 43		PHA 44		PHA 45		PHA 46		PHA 47	
7	"D"-Rates, some "F"-Rates, some "FA"-Rates, subcommutated with the Measured Spin Number															
8	-----															
9	-----															
10	-----															
11	-----															
12	-----															
13	-----															
14	-----															
15	-----															
16	-----															
17	-----															
18	-----															
19	-----															
20	-----															
21	-----															
22	"F"-Rates, "FA"-Rates, subcommutated with the Measured S															
23	-----															

Fig 22 : ICS data area (even EDB) in dual sensor mode

### 3.4.2.2 ICS formatting schemes

The counting rates from the ICS bins are accumulated in different ways. Six different **formatting schemes** (Scheme A,B,C,D,F and FA) are used in the dual sensor mode. For different schemes (schemes C,D,G,H) are used in the ICS single sensor mode. The schemes differ in time & directional resolution. Each scheme accumulates the data over one or more spins (time resolution), over one or more sectors (equatorial directional resolution) and over one or two heads (polar directional resolution). The following table describes how the different schemes work :

Scheme	# of cycles collected	time resolution (spins)	equator. dir. resolution (sectors)	polar dir. resolution (heads)
A	2	1	1	2
B	2	1	2	2
C	1	2	1	1
	2	1	1	2
	2	1	2	1
D	1	16	1	1
	2	8	2	1
	2	8	1	2
	4	4	2	2
F	1	32	1	1
	2	16	2	1
	2	16	1	2
	4	8	2	2
FA	1	32	4	1
G	1	1	1	1
H	8	1	1	1

Table 22 : ICS formatting schemes

For formatting schemes C,D and F, the time resolution can be increased to the disadvantage of directional resolution (see **I\_DIGCMD**).

Example : The “C” rates would normally be accumulated over two spins, and have full sector and head resolution. They would only be formatted into every 2nd EDB, so one EDB would contain data of 1 accumulation cycles.

If “head summation” would be turned on, the data of the two heads would be accumulated into the same bins. The time resolution would increase, i.e. the data would no longer be accumulated over two spins and the measurement cycle period would be one spin instead of two before. Still, “C” data is only transmitted in every 2nd EDB, so each 2nd EDB will contain data of 2 measurement cycles.

The following table shows how the bins are assigned to the formatting schemes in the dual sensor mode and at which positions the data of the respective bins can be found in the EDB.

<b>Scheme</b>	<b>Rate Bin</b>	<b>EDB</b>	<b>Line</b>	<b>Pos</b>	D11	<b>T8</b>	2,18	20,21	0..15
					D12	<b>T9</b>	4,20	10,11	0..15
A0	<b>E2</b>	odd	1,2	0..15	D13	<b>T10</b>	4,20	12,13	0..15
A1	<b>E5</b>	odd	3,4	0..15	D14	<b>T12</b>	4,20	14,15	0..15
B0	<b>T14</b>	odd	5	0..15	D15	<b>T13</b>	4,20	16,17	0..15
B1	<b>ED1</b>	odd	6	0..15	D16	<b>T15</b>	4,20	18,19	0..15
C0	<b>E1</b>	odd	7,8	0..15	D17	<b>P1</b>	4,20	20,21	0..15
C1	<b>E3</b>	odd	9,10	0..15	D18	<b>P3</b>	6,22	10,11	0..15
C2	<b>E4</b>	odd	11,12	0..15	D19	<b>P4</b>	6,22	12,13	0..15
C3	<b>T11</b>	odd	13,14	0..15	D20	<b>P5</b>	6,22	14,15	0..15
C4	<b>P2</b>	odd	15,16	0..15	D21	<b>P6</b>	6,22	16,17	0..15
C5	<b>HE2</b>	odd	17,18	0..15	D22	<b>P7</b>	6,22	18,19	0..15
C6	<b>M2</b>	odd	19,20	0..15	D23	<b>P8</b>	6,22	20,21	0..15
C7	<b>FSR0,1</b>	odd	21,22	0..15	D24	<b>HE1</b>	8,24	10,11	0..15
					D25	<b>HE3</b>	8,24	12,13	0..15
D0	<b>E2</b>	0,16	10,11	0..15	D26	<b>HE4</b>	8,24	14,15	0..15
D1	<b>E5</b>	0,16	12,13	0..15	D27	<b>HE5</b>	8,24	16,17	0..15
D2	<b>E6</b>	0,16	14,15	0..15	D28	<b>HE6</b>	8,24	18,19	0..15
D3	<b>E7</b>	0,16	16,17	0..15	D29	<b>HE7</b>	8,24	20,21	0..15
D4	<b>E8</b>	0,16	18,19	0..15					
D5	<b>E9</b>	0,16	20,21	0..15	D30	<b>HE8</b>	10,26	10,11	0..15
D6	<b>E10</b>	2,18	10,11	0..15	D31	<b>M1</b>	10,26	12,13	0..15
D7	<b>E11</b>	2,18	12,13	0..15	D32	<b>M3</b>	10,26	14,15	0..15
D8	<b>E12</b>	2,18	14,15	0..15	D33	<b>M4</b>	10,26	16,17	0..15
D9	<b>E13</b>	2,18	16,17	0..15	D34	<b>M5</b>	10,26	18,19	0..15
D10	<b>T6</b>	2,18	18,19	0..15	D35	<b>M6</b>	10,26	20,21	0..15



									Processing
D36	<b>RSR0,1</b>	12,28	10,11	0..15	F13	<b>HE9</b>	14	22	0..15
D37	<b>DCR0,1</b>	12,28	12,13	0..15			14	23	0..7
D38	<b>TCR0,1</b>	12,28	14,15	0..15			15	23	0..7
D39	<b>SSD0,1</b>	12,28	16,17	0..15	F14	<b>HE10</b>	16	22	0..15
D40	<b>UFSR</b>	12,28	18	0..15			16	23	0..7
D41	<b>URSR</b>	12,28	19	0..15			17	23	0..7
D42	<b>MFSR</b>	12,28	20	0..15	F15	<b>M7</b>	18	22	0..15
D43	<b>ED2</b>	12,28	21	0..15			18	23	0..7
							19	23	0..7
F0	<b>E14</b>	0	22	0..15	F16	<b>M8</b>	20	22	0..15
		0	23	0..7			20	23	0..7
		1	23	0..7			21	23	0..7
F1	<b>E15</b>	2	22	0..15	F17	<b>M9</b>	22	22	0..15
		2	23	0..7			22	23	0..7
		3	23	0..7			23	23	0..7
F2	<b>E16</b>	4	22	0..15	F18	<b>M10</b>	24	22	0..15
		4	23	0..7			24	23	0..7
		5	23	0..7			25	23	0..7
F3	<b>T1</b>	6	22	0..15	F19	<b>H1</b>	26	22	0..15
		6	23	0..7			26	23	0..7
		7	23	0..7			27	23	0..7
F4	<b>T2</b>	8	22	0..15	F20	<b>H2</b>	28	22	0..15
		8	23	0..7			28	23	0..7
		9	23	0..7			29	23	0..7
F5	<b>T3</b>	10	22	0..15	F21	<b>H3</b>	30	10,11	0..15
		10	23	0..7	F22	<b>H4</b>	30	12,13	0..15
		11	23	0..7	F23	<b>H5</b>	30	14,15	0..15
F6	<b>T4</b>	12	22	0..15	F24	<b>H6</b>	30	16,17	0..15
		12	23	0..7	F25	<b>MDCR</b>	30	18	0..15
		13	23	0..7					
F7	<b>T5</b>	14	10,11	0..15	FA0	<b>ZM</b>	30	19	0..7
F8	<b>T7</b>	14	12,13	0..15	FA1	<b>SM</b>	30	19	8..15
F9	<b>T14</b>	14	14,15	0..15	FA2	<b>E0</b>	30	20	0..7
F10	<b>T16</b>	14	16,17	0..15	FA3	<b>E17</b>	30	20	8..15
F11	<b>P9</b>	14	18,19	0..15	FA4	<b>T0</b>	30	21	0..7
F12	<b>P10</b>	14	20,21	0..15	FA5	<b>T17</b>	30	21	8..15

Table 23 : ICS rates dual sensor mode ( sorted by formatting scheme)

					Processing				
Scheme	Rate Bin	EDB	Line	Pos			5	23	0..7
					FA3	<b>E17</b>	30	22	0..15
D37	<b>DCR0,1</b>	12,28	12,13	0..15					
C7	<b>FSR0,1</b>	odd	21,22	0..15	FA4	<b>T0</b>	30	23	0..7
D36	<b>RSR0,1</b>	12,28	10,11	0..15			31	23	0..7
D39	<b>SSD0,1</b>	12,28	16,17	0..15	F3	<b>T1</b>	6	22	0..15
D38	<b>TCR0,1</b>	12,28	14,15	0..15			6	23	0..7
F25	<b>MDCR</b>	30	18	0..15			7	23	0..7
D42	<b>MFSR</b>	12,28	20	0..15	F4	<b>T2</b>	8	22	0..15
D40	<b>UFSR</b>	12,28	18	0..15			8	23	0..7
B1	<b>ED1</b>	odd	6	0..15			9	23	0..7
D43	<b>ED2</b>	12,28	21	0..15	F5	<b>T3</b>	10	22	0..15
D41	<b>URSR</b>	12,28	19	0..15			10	23	0..7
							11	23	0..7
FA2	<b>E0</b>	30	21	0..15	F6	<b>T4</b>	12	22	0..15
C0	<b>E1</b>	odd	7,8	0..15			12	23	0..7
A0	<b>E2</b>	odd	1,2	0..15			13	23	0..7
D0	<b>E2</b>	0,16	10,11	0..15	F7	<b>T5</b>	14	10,11	0..15
C1	<b>E3</b>	odd	9,10	0..15	D10	<b>T6</b>	2,18	18,19	0..15
C2	<b>E4</b>	odd	11,12	0..15	F8	<b>T7</b>	14	12,13	0..15
A1	<b>E5</b>	odd	3,4	0..15	D11	<b>T8</b>	2,18	20,21	0..15
D1	<b>E5</b>	0,16	12,13	0..15	D12	<b>T9</b>	4,20	10,11	0..15
D2	<b>E6</b>	0,16	14,15	0..15	D13	<b>T10</b>	4,20	12,13	0..15
D3	<b>E7</b>	0,16	16,17	0..15	C3	<b>T11</b>	odd	13,14	0..15
D4	<b>E8</b>	0,16	18,19	0..15	D14	<b>T12</b>	4,20	14,15	0..15
D5	<b>E9</b>	0,16	20,21	0..15	D15	<b>T13</b>	4,20	16,17	0..15
D6	<b>E10</b>	2,18	10,11	0..15	B0	<b>T14</b>	odd	5	0..15
D7	<b>E11</b>	2,18	12,13	0..15	F9	<b>T14</b>	14	14,15	0..15
D8	<b>E12</b>	2,18	14,15	0..15	D16	<b>T15</b>	4,20	18,19	0..15
D9	<b>E13</b>	2,18	16,17	0..15	F10	<b>T16</b>	14	16,17	0..15
F0	<b>E14</b>	0	22	0..15	FA5	<b>T17</b>	12	21	7..15
		0	23	0..7			28	21	7..15
		1	23	0..7					
F1	<b>E15</b>	2	22	0..15	F19	<b>H1</b>	26	22	0..15
		2	23	0..7			26	23	0..7
		3	23	0..7			27	23	0..7
F2	<b>E16</b>	4	22	0..15	F20	<b>H2</b>	28	22	0..15
		4	23	0..7			28	23	0..7

									Processing
		29	23	0.7	F15	<b>M7</b>	18	22	0..15
F21	<b>H3</b>	30	10,11	0.15			18	23	0.7
F22	<b>H4</b>	30	12,13	0.15			19	23	0.7
F23	<b>H5</b>	30	14,15	0.15	F16	<b>M8</b>	20	22	0..15
F24	<b>H6</b>	30	16,17	0.15			20	23	0.7
							21	23	0.7
D24	<b>HE1</b>	8,24	10,11	0.15	F17	<b>M9</b>	22	22	0..15
C5	<b>HE2</b>	odd	17,18	0.15			22	23	0.7
D25	<b>HE3</b>	8,24	12,13	0.15			23	23	0.7
D26	<b>HE4</b>	8,24	14,15	0.15	F18	<b>M10</b>	24	22	0..15
D27	<b>HE5</b>	8,24	16,17	0.15			24	23	0.7
D28	<b>HE6</b>	8,24	18,19	0.15			25	23	0.7
D29	<b>HE7</b>	8,24	20,21	0.15					
D30	<b>HE8</b>	10,26	10,11	0.15	D17	<b>P1</b>	4,20	20,21	0..15
F13	<b>HE9</b>	14	22	0.15	C4	<b>P2</b>	odd	15,16	0..15
		14	23	0.7	D18	<b>P3</b>	6,22	10,11	0..15
		15	23	0.7	D19	<b>P4</b>	6,22	12,13	0..15
F14	<b>HE10</b>	16	22	0.15	D20	<b>P5</b>	6,22	14,15	0..15
		16	23	0.7	D21	<b>P6</b>	6,22	16,17	0..15
		17	23	0.7	D22	<b>P7</b>	6,22	18,19	0..15
					D23	<b>P8</b>	6,22	20,21	0..15
D31	<b>M1</b>	10,26	12,13	0.15	F11	<b>P9</b>	14	18,19	0..15
C6	<b>M2</b>	odd	19,20	0.15	F12	<b>P10</b>	14	20,21	0..15
D32	<b>M3</b>	10,26	14,15	0.15					
D33	<b>M4</b>	10,26	16,17	0.15	FA1	<b>SM</b>	30	20	0..15
D34	<b>M5</b>	10,26	18,19	0.15	FA0	<b>ZM</b>	30	19	0..15
D35	<b>M6</b>	10,26	20,21	0.15					

Table 24 : ics rates dual sensor mode (sorted by rate type)

3.4.3 STICS single sensor mode

EDB Line	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
0	DPU / COMMON AREA 1															
1	HR0 0 / 0															HR0 0 / 1
2	HR0 1 / 0															HR0 1 / 1
3	HR0 2 / 0															HR0 2 / 1
4	HR0 3 / 0															HR0 3 / 1
5	HR0 4 / 0															HR0 4 / 1
6	HR0 5 / 0															HR0 5 / 1
7	HR1 0 / 0															HR1 0 / 1
8	HR1 1 / 0															HR1 1 / 1
9	HR1 2 / 0															HR1 2 / 1
10	HR1 3 / 0															HR1 3 / 1
11	HR1 4 / 0															HR1 4 / 1
12	HR1 5 / 0															HR1 5 / 1
13	HR2 0 / 0															HR2 0 / 1
14	HR2 1 / 0															HR2 1 / 1
15	HR2 2 / 0															HR2 2 / 1
16	HR2 3 / 0															HR2 3 / 1
17	HR2 4 / 0															HR2 4 / 1
18	HR2 5 / 0															HR2 5 / 1

Fig 23 : STICS single sensor mode EDB (lines 0 -18)

EDB Line	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
19	BR0 0/0							BR0 0/7	BR0 1/0							BR0 1/7
20	BR0 2/0							BR0 2/7	BR1 0/0							BR1 0/7
21	BR1 1/0							BR1 1/7	BR1 2/0							BR1 2/7
22	BR2 0/0							BR2 0/7	BR2 1/0							BR2 1/7
23	BR2 2/0							BR2 2/7	DPU / COMMON AREA 2							
24	HR3 0/0															HR3 0/1
25	HR3 1/0															HR3 1/1
26	HR3 2/0															HR3 2/1
27	HR3 3/0															HR3 3/1
28	HR3 4/0															HR3 4/1
29	HR3 5/0															HR3 5/0
30	HR4 0/0															HR4 0/1
31	HR4 1/0															HR4 1/1
32	HR4 2/0															HR4 2/1
33	HR4 3/0															HR4 3/1
34	HR4 4/0															HR4 4/1
35	HR4 5/0															HR4 5/1
36	MR0 4/0							MR7	MR8							MR1 4/1

Fig 24 : STICS single sensor mode EDB (lines 19 - 35)

EDB Line	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	
37	MR1	MR1						MR2	MR2							MR3	
38	MR3	MR3	FSR	FSR	FSR	UFS	URS	RSR	RSR	RSR	DCR	DCR	DCR	TCR	TCR	TCR	
39	SSD	SSD	SSD	MFS	MDC	KMPF	MPR	DIA					PHA00			PHA01	
40		PHA02			PHA03				PHA04			PHA05					
41		PHA06			PHA07				PHA08			PHA09					
42		PHA10			PHA11				PHA12			PHA13					
43		PHA14			PHA15				PHA16			PHA17					
44		PHA18			PHA19				PHA20			PHA21					
45		PHA22			PHA23				PHA24			PHA25					
46		PHA26			PHA27				PHA28			PHA29					
47		PHA30			PHA31				PHA32			PHA33					
48		PHA34			PHA35				PHA36			PHA37					
49		PHA38			PHA39				PHA40			PHA41					
50		PHA42			PHA43				PHA44			PHA45					
51		PHA46			PHA47				PHA48			PHA49					
52		PHA50			PHA51				PHA52			PHA53					
53		PHA54			PHA55				PHA56			PHA57					
54		PHA58			PHA59				PHA60			PHA61					
55		PHA62			PHA63				PHA64			PHA65					
56		PHA66			PHA67				PHA68			PHA69					
57		PHA70			PHA71				PHA72			PHA73					
58		PHA74			PHA75				PHA76			PHA77					
59		PHA78			PHA79				PHA80			PHA81					

Fig 25: STICS single sensor mode EDB (lines 36 - 59)

3.4.4 ICS single sensor mode

EDB Line	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
0	DPU / COMMON AREA 1															
1	PHA 0		PHA 1			PHA 2			PHA 3			PHA 4			PHA 5	
2	PHA 5		PHA 6			PHA 7			PHA 8			PHA 9			PHA 10	
3	PHA 10	PHA 11			PHA 12			PHA 13			PHA 14			PHA 15		
4	PHA 16			PHA 17			PHA 18			PHA 19			PHA 20			PHA 21
5	PHA 21		PHA 22			PHA 23			PHA 24			PHA 25			PHA 26	
6	PHA 26	PHA 27			PHA 28			PHA 29			PHA 30			PHA 31		
7	PHA 32			PHA 33			PHA 34			PHA 35			PHA 36			PHA 37
8	PHA 37		PHA 38			PHA 39			PHA 40			PHA 41			PHA 42	
9	PHA 42	PHA 43			PHA 44			PHA 45			PHA 46			PHA 47		
10	PHA 48			PHA 49			PHA 50			PHA 51			PHA 52			PHA 53
11	PHA 53		PHA 54			PHA 55			PHA 56			PHA 57			PHA 58	
12	PHA 58	PHA 59			PHA 60			PHA 61			PHA 62			PHA 63		
13																
14																
15																
16																
17																
18																
19																
21																
22																

Fig 26: ICS single sensor mode EDB (lines 0 -22)

EDB Line	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
23	unused								DPU / COMMON AREA 2							
24																
25																
26																
27																
28																
29								█	█	█						
30							█				█					
31							█									
32							█		█	█	█					
33							█		█		█					
34							█				█					
35								█	█	█						
36																
37																
38																
39																
40																
41																

Fig 27: ICS single sensor mode EDB (lines 23 - 41)



EDB Line	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
42																
43																
44																
45																
46																
47																
48																
49																
50																
51																
52																
53																
54																
55																
56																
57																
58																
59																

Fig 28: ICS single sensor mode EDB (lines 42 - 59)

					Processing				
<b>Scheme</b>	<b>Rate</b>	<b>EDB</b>	<b>Line</b>	<b>Pos</b>	D29	<b>MFSR</b>	14,30	58	0..15
					D30	<b>MDCR</b>	14,30	59	0..15
	<b>Bin</b>								
C0	<b>E1</b>	even	42,43	0..15					
C1	<b>E3</b>	even	44,45	0..15	G0	<b>E2</b>	every	13,14	0..15
C2	<b>E4</b>	even	46,47	0..15	G1	<b>E5</b>	every	15,16	0..15
C3	<b>T8</b>	odd	42,43	0..15	G2	<b>E8</b>	every	17,18	0..15
C4	<b>P1</b>	odd	44,45	0..15	G3	<b>E11</b>	every	19,20	0..15
C5	<b>P3</b>	odd	46,47	0..15	G4	<b>T6</b>	every	21,22	0..15
					G5	<b>T11</b>	every	24,25	0..15
D0	<b>E15</b>	0,16	56,57	0..15	G6	<b>T14</b>	every	26,27	0..15
D1	<b>E16</b>	0,16	58,59	0..15	G7	<b>P2</b>	every	28,29	0..15
D2	<b>T1</b>	1,17	56,57	0..15	G8	<b>P4</b>	every	30,31	0..15
D3	<b>T2</b>	1,17	58,59	0..15	G9	<b>He2</b>	every	32,33	0..15
D4	<b>T3</b>	2,18	56,57	0..15	G10	<b>He4</b>	every	34,35	0..15
D5	<b>T15</b>	2,18	58,59	0..15	G11	<b>FSR</b>	every	36,37	0..15
D6	<b>T16</b>	3,19	56,57	0..15	G12	<b>SSD</b>	every	38,39	0..15
D7	<b>P9</b>	3,19	58,59	0..15	G13	<b>ED1</b>	every	40	0..15
D8	<b>P10</b>	4,20	56,57	0..15	G14	<b>ED2</b>	every	41	0..15
D9	<b>He7</b>	4,20	58,59	0..15					
D10	<b>He8</b>	5,21	56,57	0..15	H0	<b>E6</b>	0,8,16,24	48,49	0..15
D11	<b>He9</b>	5,21	58,59	0..15	H1	<b>E7</b>	0,8,16,24	50,51	0..15
D12	<b>He10</b>	6,22	56,57	0..15	H2	<b>E9</b>	0,8,16,24	52,53	0..15
D13	<b>M1</b>	6,22	58,59	0..15	H3	<b>E10</b>	0,8,16,24	54,55	0..15
D14	<b>M8</b>	7,23	56,57	0..15	H4	<b>E12</b>	1,9,17,25	48,49	0..15
D15	<b>M9</b>	7,23	58,59	0..15	H5	<b>E13</b>	1,9,17,25	50,51	0..15
D16	<b>M10</b>	8,24	56,57	0..15	H6	<b>E14</b>	1,9,17,25	52,53	0..15
D17	<b>H1</b>	8,24	58,59	0..15	H7	<b>T4</b>	1,9,17,25	54,55	0..15
D18	<b>H2</b>	9,25	56,57	0..15	H8	<b>T5</b>	2,10,18,26	48,49	0..15
D19	<b>H3</b>	9,25	58,59	0..15	H9	<b>T7</b>	2,10,18,26	50,51	0..15
D20	<b>H4</b>	10,26	56,57	0..15	H10	<b>T9</b>	2,10,18,26	52,53	0..15
D21	<b>H5</b>	10,26	58,59	0..15	H11	<b>T10</b>	2,10,18,26	54,55	0..15
D22	<b>H6</b>	11,27	56,57	0..15	H12	<b>T12</b>	3,11,19,27	48,49	0..15
D23	<b>E0</b>	11,27	58,59	0..15	H13	<b>T13</b>	3,11,19,27	50,51	0..15
D24	<b>E17</b>	12,28	56,57	0..15	H14	<b>P5</b>	3,11,19,27	52,53	0..15
D25	<b>T0</b>	12,28	58,59	0..15	H15	<b>P6</b>	3,11,19,27	54,55	0..15
D26	<b>T17</b>	13,29	56,57	0..15	H16	<b>P7</b>	4,12,20,28	48,49	0..15
D27	<b>MS</b>	13,29	58,59	0..15	H17	<b>P8</b>	4,12,20,28	50,51	0..15
D28	<b>MZ</b>	14,30	56,57	0..15	H18	<b>He1</b>	4,12,20,28	52,53	0..15

H19	<b>He3</b>	4,12,20,28	54,55	0..15	H26	<b>M6</b>	6,14,22,30	52,53	0..15
H20	<b>He5</b>	5,13,21,29	48,49	0..15	H27	<b>M7</b>	6,14,22,30	54,55	0..15
H21	<b>He6</b>	5,13,21,29	50,51	0..15	H28	<b>RSR</b>	7,15,23,31	48,49	0..15
H22	<b>M2</b>	5,13,21,29	52,53	0..15	H29	<b>DCR</b>	7,15,23,31	50,51	0..15
H23	<b>M3</b>	5,13,21,29	54,55	0..15	H30	<b>TCR</b>	7,15,23,31	52,53	0..15
H24	<b>M4</b>	6,14,22,30	48,49	0..15	H31	<b>UFSR</b>	7,15,23,31	54	0..15
H25	<b>M5</b>	6,14,22,30	50,51	0..15	H32	<b>URSR</b>	7,15,23,31	55	0..15

Table 25 : ICS rates single sensor mode (sorted by format scheme)

<b>Rate</b>	<b>Scheme</b>	<b>EDB</b>	<b>Line</b>	<b>Pos</b>	<b>He5</b>	H20	5,13,21,29	48,49	0..15
<b>Bin</b>									
<b>DCR</b>	H29	7,15,23,31	50,51	0..15	<b>He6</b>	H21	5,13,21,29	50,51	0..15
<b>FSR</b>	G11	every	36,37	0..15	<b>He7</b>	D9	4,20	58,59	0..15
<b>RSR</b>	H28	7,15,23,31	48,49	0..15	<b>He8</b>	D10	5,21	56,57	0..15
<b>SSD</b>	G12	every	38,39	0..15	<b>He9</b>	D11	5,21	58,59	0..15
<b>TCR</b>	H30	7,15,23,31	52,53	0..15	<b>He10</b>	D12	6,22	56,57	0..15
<b>MDCR</b>	D30	14,30	59	0..15	<b>M1</b>	D13	6,22	58,59	0..15
<b>MFSR</b>	D29	14,30	58	0..15	<b>M2</b>	H22	5,13,21,29	52,53	0..15
<b>UFSR</b>	H31	7,15,23,31	54	0..15	<b>M3</b>	H23	5,13,21,29	54,55	0..15
<b>URSR</b>	H32	7,15,23,31	55	0..15	<b>M4</b>	H24	6,14,22,30	48,49	0..15
<b>ED1</b>	G13	every	40	0..15	<b>M5</b>	H25	6,14,22,30	50,51	0..15
<b>ED2</b>	G14	every	41	0..15	<b>M6</b>	H26	6,14,22,30	52,53	0..15
					<b>M7</b>	H27	6,14,22,30	54,55	0..15
<b>P1</b>	C4	odd	44,45	0..15	<b>M8</b>	D14	7,23	56,57	0..15
<b>P2</b>	G7	every	28,29	0..15	<b>M9</b>	D15	7,23	58,59	0..15
<b>P3</b>	C5	odd	46,47	0..15	<b>M10</b>	D16	8,24	56,57	0..15
<b>P4</b>	G8	every	30,31	0..15					
<b>P5</b>	H14	3,11,19,27	52,53	0..15	<b>H1</b>	D17	8,24	58,59	0..15
<b>P6</b>	H15	3,11,19,27	54,55	0..15	<b>H2</b>	D18	9,25	56,57	0..15
<b>P7</b>	H16	4,12,20,28	48,49	0..15	<b>H3</b>	D19	9,25	58,59	0..15
<b>P8</b>	H17	4,12,20,28	50,51	0..15	<b>H4</b>	D20	10,26	56,57	0..15
<b>P9</b>	D7	3,19	58,59	0..15	<b>H5</b>	D21	10,26	58,59	0..15
<b>P10</b>	D8	4,20	56,57	0..15	<b>H6</b>	D22	11,27	56,57	0..15
					<b>T0</b>	D25	12,28	58,59	0..15
<b>He1</b>	H18	4,12,20,28	52,53	0..15	<b>T1</b>	D2	1,17	56,57	0..15
<b>He2</b>	G9	every	32,33	0..15	<b>T2</b>	D3	1,17	58,59	0..15
<b>He3</b>	H19	4,12,20,28	54,55	0..15	<b>T3</b>	D4	2,18	56,57	0..15
<b>He4</b>	G10	every	34,35	0..15	<b>T4</b>	H7	1,9,17,25	54,55	0..15

					Processing				
<b>T5</b>	H8	2,10,18,26	48,49	0..15	<b>E4</b>	C2	even	46,47	0..15
<b>T6</b>	G4	every	21,22	0..15	<b>E5</b>	G1	every	15,16	0..15
<b>T7</b>	H9	2,10,18,26	50,51	0..15	<b>E6</b>	H0	0,8,16,24	48,49	0..15
<b>T8</b>	C3	odd	42,43	0..15	<b>E7</b>	H1	0,8,16,24	50,51	0..15
<b>T9</b>	H10	2,10,18,26	52,53	0..15	<b>E8</b>	G2	every	17,18	0..15
<b>T10</b>	H11	2,10,18,26	54,55	0..15	<b>E9</b>	H2	0,8,16,24	52,53	0..15
<b>T11</b>	G5	every	24,25	0..15	<b>E10</b>	H3	0,8,16,24	54,55	0..15
<b>T12</b>	H12	3,11,19,27	48,49	0..15	<b>E11</b>	G3	every	19,20	0..15
<b>T13</b>	H13	3,11,19,27	50,51	0..15	<b>E12</b>	H4	1,9,17,25	48,49	0..15
<b>T14</b>	G6	every	26,27	0..15	<b>E13</b>	H5	1,9,17,25	50,51	0..15
<b>T15</b>	D5	2,18	58,59	0..15	<b>E14</b>	H6	1,9,17,25	52,53	0..15
<b>T16</b>	D6	3,19	56,57	0..15	<b>E15</b>	D0	0,16	56,57	0..15
<b>T17</b>	D26	13,29	56,57	0..15	<b>E16</b>	D1	0,16	58,59	0..15
					<b>E17</b>	D24	12,28	56,57	0..15
<b>E0</b>	D23	11,27	58,59	0..15					
<b>E1</b>	C0	even	42,43	0..15	<b>MS</b>	D27	13,29	58,59	0..15
<b>E2</b>	G0	every	13,14	0..15	<b>MZ</b>	D28	14,30	56,57	0..15
<b>E3</b>	C1	even	44,45	0..15					

Table 26 : ICS rates single sensor mode (sorted by rate type)

### 3.5 Subcommutated housekeeping

There are 192 subcommutated housekeeping channels defined, each of which gets transmitted once during one science record in editor A status and during four science records in editor B status. However, the subcommutated HK data is also redundantly transmitted in the EDBs (each EDB contains 6 HK data bytes,  $6 \times 32 = 192$ ). Note that fixed cycle housekeeping (see **D\_PARLDA** and **D\_DIGCMD 13**) only effects the housekeeping readout in the editor A and editor B status; the housekeeping in the EDBs retains the normal full cycle.

The contents of the 192 subcommutated housekeeping bytes follow, preceded by the index:

<u>Housekeeping Item Name</u>	<u>High Bit</u>			<u>Page</u>
	<u>Byte</u>	<u>Bit</u>	<u>Quan.</u>	<u>No.</u>
STICS HVPS1 (North Start) Limit.....	0	7	8	84
STICS HVPS2 (Equatorial Start) Limit.....	1	7	8	84
STICS HVPS3 (South Start) Limit.....	2	7	8	85
STICS HVPS4 (North Stop) Limit.....	3	7	8	85
STICS HVPS5 (NEquatorial Stop) Limit.....	4	7	8	86
STICS HVPS6 (South Stop) Limit.....	5	7	8	86
STICS HVPS7 (TOF) Limit.....	6	7	8	87
STICS HVPS1 (North Start) Level.....	7	7	8	87
STICS HVPS2 (Equatorial Start) Level.....	8	7	8	88
STICS HVPS3 (South Start) Level.....	9	7	8	88
STICS HVPS4 (North Stop) Level.....	10	7	8	89
STICS HVPS5 (Equatorial Stop) Level.....	11	7	8	89
STICS HVPS6 (South Stop) Level.....	12	7	8	90
STICS HVPS7 (TOF) Level.....	13	7	8	90
STICS positive DPPS target status.....	14	7	1	91
STICS HVPS7 (TOF PS) target status.....	14	6	1	91
STICS HVPS6 (S St MCP) target status.....	14	5	1	91
STICS HVPS5 (E St MCP) target status.....	14	4	1	91
STICS HVPS4 (N St MCP) target status.....	14	3	1	91
STICS HVPS3 (S Sp MCP) target status.....	14	2	1	91
STICS HVPS2 (E Sp MCP) target status.....	14	1	1	91
STICS HVPS1 (N Sp MCP) target status.....	14	0	1	91
STICS BR2 selected range.....	15	7	2	91
STICS BR1 selected range.....	15	5	2	91
STICS BR0 selected range.....	15	3	2	91
STICS negative DPPS target status.....	15	0	1	91
STICS LVPS over-current.....	16	7	1	92
STICS I/F error check.....	16	6	1	92
STICS test logic enable.....	16	5	1	92
STICS south SSD preamp power.....	16	4	1	92
STICS equatorial SSD preamp power.....	16	3	1	92
STICS north SSD preamp power.....	16	2	1	92
STICS valid event mode.....	17	7	3	92
STICS south time disable.....	17	4	1	92
STICS equatorial stop time disable.....	17	3	1	92
STICS equatorial start B disable.....	17	2	1	92
STICS equatorial start A disable.....	17	1	1	92
STICS north time disable.....	17	0	1	92
STICS time calibrate enable.....	18	5	1	93
STICS slow PHA analysis mode.....	18	4	1	93
STICS multiple stop enable.....	18	3	1	93
STICS multiple start enable.....	18	2	1	93
STICS main bias power.....	18	0	1	93
STICS Group 2 compression.....	19	6	1	93
STICS Group 1 compression.....	19	5	1	93

<u>Housekeeping Item Name</u>	<u>High Bit</u>			<u>Page</u>
	<u>Byte</u>	<u>Bit</u>	<u>Quan.</u>	<u>No.</u>
STICS south bias disable.....	19	4	1	93
STICS equatorial bias disable.....	19	3	1	93
STICS north bias disable.....	19	7	1	93
STICS active stepping sequence.....	19	1	2	93
STICS aperture status.....	20	0	1	94
STICS HVPS1 voltage monitor.....	21	7	8	94
STICS HVPS2 voltage monitor.....	22	7	8	95
STICS HVPS3 voltage monitor.....	23	7	8	95
STICS HVPS4 voltage monitor.....	24	7	8	96
STICS HVPS5 voltage monitor.....	25	7	8	96
STICS HVPS6 voltage monitor.....	26	7	8	97
STICS HVPS7 voltage monitor.....	27	7	8	97
STICS MCPPS & TOFPS current.....	28	7	8	98
STICS GROUND.....	29	7	8	98
STICS DPPS current.....	30	7	8	99
STICS Analog Electronics Thermistor.....	31	7	8	99
STICS unused Thermistor.....	32	7	8	100
STICS Sensor Backpanel Thermistor.....	33	7	8	100
STICS Sensor Detector Thermistor.....	34	7	8	101
STICS LVPS +6 Voltage.....	35	7	8	101
STICS LVPS -6 Voltage.....	36	7	8	102
STICS LVPS +5.2 Voltage.....	37	7	8	102
STICS LVPS -5.2 Voltage.....	38	7	8	103
STICS LVPS +12 Voltage.....	39	7	8	103
STICS LVPS SSD Bias Voltage (unused).....	40	7	8	104
STICS LVPS Current.....	41	7	8	104
STICS LVPS -12 Voltage.....	42	7	8	105
STICS accum. latch count.....	43	7	8	105
STICS north energy threshold.....	44	7	5	106
STICS equatorial energy threshold.....	44	1	5	106
STICS south energy threshold.....	45	3	5	106
STICS TOF calibration level.....	46	5	4	107
STICS energy calibration level.....	47	7	8	107
STICS +DPPS level.....	48	3	12	108
STICS -DPPS level.....	50	3	12	109
STICS +DPPS discharge count.....	52	7	8	110
STICS -DPPS discharge count.....	53	7	8	110
DPU MREG2 H/W register.....	54	7	16	111
DPU C_COM H/W register.....	56	7	16	112
ICS HVPS1 (North Stop) Limit.....	64	7	8	116
ICS HVPS2 (North Start) Limit.....	65	7	8	116
ICS HVPS3 (South Stop) Limit.....	66	7	8	117
ICS HVPS4 (North Start) Limit.....	67	7	8	117
ICS HVPS5 (TOF) Limit.....	68	7	8	118
ICS HVPS1 (North Stop) Level.....	69	7	8	118
ICS HVPS2 (North Start) Level.....	70	7	8	119
ICS HVPS3 (South Stop) Level.....	71	7	8	119
ICS HVPS4 (South Start) Level.....	72	7	8	120
ICS HVPS5 (TOF) Level.....	73	7	8	120
ICS energy calibration level.....	74	7	8	121
ICS I/F error check.....	75	7	1	121
ICS Calibration Readout enable.....	75	4	1	121
ICS frozen mass PHA range.....	75	3	2	121
ICS frozen energy PHA range.....	75	1	2	121
ICS LVPS over current.....	76	7	1	122
ICS energy calibrate power.....	76	6	1	122
ICS test logic enable.....	76	5	1	122
ICS south SSD preamp power.....	76	4	1	122
ICS ED preamp power.....	76	3	1	122
ICS north SSD preamp power.....	76	2	1	122

<u>Housekeeping Item Name</u>	<u>Byte</u>	<u>High Bit</u>		<u>Page</u>
		<u>Bit</u>	<u>Quan.</u>	<u>No.</u>
ICS PHA mass freeze enable.....	76	1	1	122
ICS PHA energy freeze enable.....	76	0	1	122
ICS valid event mode.....	77	7	3	122
ICS south stop time disable.....	77	4	1	122
ICS south start disable.....	77	2	1	122
ICS north start disable.....	77	1	1	122
ICS north stop time disable.....	77	0	1	122
ICS PHA FIFO mode.....	78	7	1	123
ICS position sensor power.....	78	6	1	123
ICS time calibration power.....	78	5	1	123
ICS slow PHA analysis mode.....	78	4	1	123
ICS multiple stop enable.....	78	3	1	123
ICS multiple start enable.....	78	2	1	123
ICS SSD bias high enable.....	78	1	1	123
ICS auto-aperture enable.....	78	0	1	123
ICS F-format sector summation enable.....	79	7	1	123
ICS F-format head summation enable.....	79	6	1	123
ICS D-format sector summation enable.....	79	5	1	123
ICS D-format head summation enable.....	79	4	1	123
ICS C-format sector summation enable.....	79	3	1	123
ICS C-format head summation enable.....	79	2	1	123
ICS south motor power.....	80	7	1	124
ICS south position sensor status.....	80	6	3	124
ICS north motor power.....	80	3	1	124
ICS north position sensor status.....	80	2	3	124
ICS HVPS1 (N Sp) voltage monitor.....	81	7	8	124
ICS HVPS2 (N St) voltage monitor.....	82	7	8	125
ICS HVPS3 (S Sp) voltage monitor.....	83	7	8	125
ICS HVPS4 (S St) voltage monitor.....	84	7	8	126
ICS HVPS5 (TOF) voltage monitor.....	85	7	8	126
ICS MCPPS & TOFPS current.....	86	7	8	127
ICS TOF calibration level.....	87	7	4	127
ICS GROUND.....	87	3	4	127
ICS motor current.....	88	7	8	128
ICS Analog Electronic Thermistor.....	89	7	8	128
ICS Sensor Backpanel Thermistor.....	90	7	8	129
ICS Sensor South Head Thermistor.....	91	7	8	129
ICS Sensor ED Thermistor.....	92	7	8	130
ICS LVPS +6 Voltage.....	93	7	8	130
ICS LVPS -6 Voltage.....	94	7	8	131
ICS LVPS +5.2 Voltage.....	95	7	8	131
ICS LVPS -5.2 Voltage.....	96	7	8	132
ICS LVPS +12 Voltage.....	97	7	8	132
ICS LVPS SSD Bias Voltage.....	98	7	8	133
ICS LVPS Current.....	99	7	8	133
ICS LVPS -12 Voltage.....	100	7	8	134
ICS north energy threshold.....	101	7	5	134
ICS ED1 threshold.....	101	1	5	134
ICS south energy threshold.....	102	3	5	135
ICS ED2 threshold.....	103	5	5	135
ICS Group 2 compression.....	104	7	1	136
ICS Group 1 compression.....	104	6	1	136
ICS HVPS5 target status.....	104	5	1	136
ICS HVPS4 target status.....	104	4	1	136
ICS HVPS3 target status.....	104	3	1	136
ICS HVPS2 target status.....	104	2	1	136
ICS HVPS1 target status.....	104	1	1	136
ICS reduced motor movement enable.....	104	0	1	136
ICS accum. latch count.....	106	7	8	137
STICS science boundary table #1.....	107	7	8	137

<u>Housekeeping Item Name</u>	<u>High Bit</u>		<u>Page</u>
	<u>Byte</u>	<u>Bit Quan.</u>	<u>No.</u>
STICS science boundary table #2.....	108	7...8	138
STICS science boundary table #3.....	109	7...8	138
STICS science boundary table #4.....	110	7...8	139
STICS science boundary table #5.....	111	7...8	139
STICS science boundary table #6.....	112	7...8	140
STICS science boundary table #7.....	113	7...8	140
STICS science boundary table #8.....	114	7...8	141
STICS science boundary table #9.....	115	7...8	141
STICS science boundary table #10.....	116	7...8	142
STICS science rate corner table #1.....	117	7...8	142
STICS science rate corner table #2.....	118	7...8	143
STICS science rate corner table #3.....	119	7...8	143
STICS science rate corner table #4.....	120	7...8	144
STICS science rate corner table #5.....	121	7...8	144
DPU valid commands executed count.....	122	7...8	145
DPU valid BC identifier #2.....	123	7...8	145
DPU valid BC identifier #1.....	124	7...8	146
DPU valid BC identifier #1.....	124	7...8	146
DPU invalid command count.....	126	7...8	147
DPU last invalid BC identifier.....	127	7...8	147
DPU last invalid command error code.....	128	7...8	148
DPU watchdog enable.....	129	7...1	148
DPU last reset cause.....	129	6...2	148
DPU NVRAM error.....	129	4...1	148
DPU D_PLDBAD segment address.....	129	3...4	148
DPU D_PLDBAD address.....	130	7...16	149
DPU snapshot config. load error.....	133	5...1	150
DPU current config. load error.....	133	4...1	150
ICS snapshot config. load error.....	133	3...1	150
ICS current config. load error.....	133	2...1	150
STICS snapshot config. load error.....	133	1...1	150
STICS current config. load error.....	133	0...1	150
DPU reset counter.....	134	6...7	151
DPU test tables status.....	134	0...1	151
DPU latch-up monitor configuration.....	135	7...8	151
DPU D_PRGADR program load address.....	136	7...20	152
DPU alarm monitor status.....	138	2...1	153
DPU internal sector clock.....	138	1...1	153
DPU internal clock active.....	138	0...1	153
DPU STICS class. parity errors.....	139	7...8	153
DPU ICS class. parity errors.....	140	7...8	154
DPU STICS irreparable class. errors.....	141	7...8	154
DPU ICS irreparable class. errors.....	142	7...8	155
DPU alarm channel 0 (STICS AE temp).....	143	7...2	155
DPU alarm channel 1 (STICS unused temp).....	143	5...2	155
DPU alarm channel 2 (STICS BP temp).....	143	3...2	155
DPU alarm channel 3 (STICS sensor temp).....	143	1...2	155
DPU alarm channel 4 (ICS AE temp).....	144	7...2	156
DPU alarm channel 5 (ICS BP temp).....	144	5...2	156
DPU alarm channel 6 (ICS SH temp).....	144	3...2	156
DPU alarm channel 7 (ICS ED temp).....	144	1...2	156
DPU alarm channel 8 (STICS +6 volt).....	145	7...2	156
DPU alarm channel 9 (STICS N St MCP volt).....	145	5...2	156
DPU alarm channel 10 (STICS N Sp MCP volt).....	145	3...2	156
DPU alarm channel 11 (STICS E St MCP volt).....	145	1...2	156
DPU alarm channel 12 (STICS E Sp MCP volt).....	146	7...2	157
DPU alarm channel 13 (STICS S St MCP volt).....	146	5...2	157
DPU alarm channel 14 (STICS S Sp MCP volt).....	146	3...2	157
DPU alarm channel 15 (STICS TOF volt).....	146	1...2	157
DPU alarm channel 16 (ICS +6 volt).....	147	7...2	157



<u>Housekeeping Item Name</u>	<u>High Bit</u>		<u>Page</u>
	<u>Byte</u>	<u>Bit Quan.</u>	<u>No.</u>
DPU alarm channel 17 (ICS N Sp MCP volt).....	147	5...2	157
DPU alarm channel 18 (ICS N St MCP volt).....	147	3...2	157
DPU alarm channel 19 (ICS S Sp MCP volt).....	147	1...2	157
DPU alarm channel 20 (ICS N Sp MCP volt).....	148	7...2	158
DPU alarm channel 21 (ICS TOF volt).....	148	5...2	158
DPU alarm channel 22 (STICS LVPC current).....	148	3...2	158
DPU alarm channel 23 (STICS MCPPS current).....	148	1...2	158
DPU alarm channel 24 (STICS DPPS current).....	149	7...2	158
DPU alarm channel 25 (ICS LVPS current).....	149	5...2	158
DPU alarm channel 26 (ICS MCPPS current).....	149	3...2	158
DPU alarm channel 27 (ICS motor current).....	149	1...2	158
DPU alarm channel 28 (STICS LVPS over-curr)....	150	7...2	159
DPU alarm channel 29 (ICS LVPS over-curr)....	150	5...2	159
DPU alarm channel 30 (unused).....	150	3...2	159
DPU alarm channel 31 (unused).....	150	1...2	159
DPU sun sector.....	151	7...4	159
DPU parameter index.....	151	3...12	159
DPU parameter byte 1.....	153	7...8	160
DPU parameter byte 2.....	154	7...8	161
DPU parameter byte 3.....	154	7...8	161
DPU parameter byte 4.....	156	7...8	162
DPU parameter byte 5.....	157	7...8	162
DPU parameter byte 6.....	158	7...8	163
DPU parameter byte 7.....	159	7...8	163
DPU parameter byte 8.....	160	7...8	164
DPU parameter byte 9.....	161	7...8	164
DPU parameter byte 10.....	162	7...8	165
DPU parameter byte 11.....	163	7...8	165
DPU parameter byte 12.....	164	7...8	166
DPU parameter byte 13.....	165	7...8	166
DPU parameter byte 14.....	166	7...8	167
DPU parameter byte 15.....	167	7...8	167
DPU parameter byte 16.....	168	7...8	168
DPU parameter byte 16??.....	169	7...8	168
DPU Science Record counter.....	170	7...24	169
DPU Sunpulse subsector offset.....	173	7...8	170
DPU D_SENCMD answer.....	174	7...32	171
STICS class. double errors.....	178	7...8	173
ICS class. double errors.....	178	7...8	173
DPU P-RAM single errors.....	180	7...8	174
DPU P-ROM single errors.....	181	7...8	174
DPU auto-reconfigs remaining.....	182	7...16	175
DPU alarm lower limit 1.....	184	7...8	176
DPU alarm upper limit 1.....	185	7...8	176
DPU alarm lower limit 2.....	186	7...8	177
DPU alarm upper limit 2.....	187	7...8	177
DPU alarm lower limit 3.....	188	7...8	178
DPU alarm upper limit 3.....	189	7...8	178
DPU alarm lower limit 4.....	190	7...8	179
DPU alarm upper limit 4.....	191	7...8	179

## EPIC Subcommutated HK

Bytes 0,1

Byte #	Bit #	Comments
0 00h	7	MSB STICS commanded HV Limit #1 (north start MCP)
	6	
	5	
	4	
	3	
	2	
	1	
	0	LSB
		Source: abySHVLim[0]
1 01h	7	MSB STICS commanded HV Limit #2 (equatorial start MCP)
	6	
	5	
	4	
	3	
	2	
	1	
	0	LSB
		Source: abySHVLim[1]

## EPIC Subcommutated HK

## Bytes 2,3

Byte #	Bit #	Comments
2 02h	7	MSB STICS commanded HV Limit #3 (south start MCP)
	6	
	5	
	4	
	3	
	2	
	1	
	0	LSB
		Source: abySHVLim[2]
3 03h	7	MSB STICS commanded HV Limit #4 (north stop MCP)
	6	
	5	
	4	
	3	
	2	
	1	
	0	LSB
		Source: abySHVLim[3]

## EPIC Subcommutated HK

## Bytes 4,5

Byte #	Bit #	Comments
4 04h	7	MSB STICS commanded HV Limit #5 (equatorial stop MCP)
	6	
	5	
	4	
	3	
	2	
	1	
	0	LSB
		Source: abySHVLim[4]
5 05h	7	MSB STICS commanded HV Limit #6 (south stop MCP)
	6	
	5	
	4	
	3	
	2	
	1	
	0	LSB
		Source: abySHVLim[5]

## EPIC Subcommutated HK

## Bytes 6,7

Byte #	Bit #	Comments
6 06h	7	MSB STICS commanded HV Limit #7 (time of flight PS)
	6	
	5	
	4	
	3	
	2	
	1	
	0	LSB
		Source: abySHVLim[6]
7 07h	7	MSB STICS commanded HV target level #1 (north start MCP)
	6	
	5	
	4	
	3	
	2	
	1	
	0	LSB
		Source: abySHVDestLev[0]

## EPIC Subcommutated HK

## Bytes 8,9

Byte #	Bit #	Comments
8 08h	7	MSB STICS commanded HV target level #2 (equatorial start MCP)
	6	
	5	
	4	
	3	
	2	
	1	
	0	LSB
		Source: abySHVDestLev[1]
9 09h	7	MSB STICS commanded HV target level #3 (south start MCP)
	6	
	5	
	4	
	3	
	2	
	1	
	0	LSB
		Source: abySHVDestLev[2]

0Ah,0Bh

EPIC Subcommutated HK

Bytes 10,11

Byte #	Bit #	Comments
10 0Ah	7	MSB STICS commanded HV target level #4 (north stop MCP)
	6	
	5	
	4	
	3	
	2	
	1	
	0	LSB
		Source: abySHVDestLev[3]
11 0Bh	7	MSB STICS commanded HV target level #5 (equatorial stop MCP)
	6	
	5	
	4	
	3	
	2	
	1	
	0	LSB
		Source: abySHVDestLev[4]

0C,0D

EPIC Subcommutated HK

Bytes 12,13

Byte #	Bit #	Comments
12 0Ch	7	MSB STICS commanded HV target level #6 (north stop MCP)
	6	
	5	
	4	
	3	
	2	
	1	
	0	LSB
		Source: abySHVDestLev[5]
13 0Dh	7	MSB STICS commanded HV target level #7 (time of flight PS)
	6	
	5	
	4	
	3	
	2	
	1	
	0	LSB
		Source: abySHVDestLev[6]



0E,0F

EPIC Subcommutated HK

Bytes 14,15

Byte #	Bit #	Comments
14 0Eh	7	STICS positive DPPS target status Source: awSenCurCmd[S DPPS EN] bit 0
	6	STICS HVPS7 (time of flight PS) target status Source: awSenCurCmd[S MINI HVPS] bit 6
	5	STICS HVPS6 (south stop MCP) target status Source: awSenCurCmd[S MINI HVPS] bit 5
	4	STICS HVPS5 (equatorial stop MCP) target status Source: awSenCurCmd[S MINI HVPS] bit 4
	3	STICS HVPS4 (north stop MCP) target status Source: awSenCurCmd[S MINI HVPS] bit 3
	2	STICS HVPS3 (south start MCP) target status Source: awSenCurCmd[S MINI HVPS] bit 2
	1	STICS HVPS2 (equatorial start MCP) target status Source: awSenCurCmd[S MINI HVPS] bit 1
	0	STICS HVPS1 (north start MCP) target status Source: awSenCurCmd[S MINI HVPS] bit 0
15 0Fh	7	MSB STICS selected range for BR2
	6	LSB Source: awSCRPriorTab[2] bit 0,1
	5	MSB STICS selected range for BR1
	4	LSB Source: awSCRPriorTab[1] bit 0,1
	3	MSB STICS selected range for BR0
	2	LSB Source: awSCRPriorTab[0] bit 0,1
	1	
	0	STICS negative DPPS target status Source: awSenCurCmd[S MINI HVPS] bit 1

10h,11h

EPIC Subcommutated HK

Bytes 16,17

Byte #	Bit #	Comments
16 10h	7	STICS LVPS over-current flag Source: adwSTICSAnsw[2] bit 15
	6	STICS AE I/F echo 0 : disabled (error) check status 1 : enabled
	5	STICS Test Logic Enable Source: adwSTICSAnsw[2] bit 13
	4	STICS South SSD Preamp Power Source: adwSTICSAnsw[2] bit 12
	3	STICS Equatorial SSD Preamp Power Source: adwSTICSAnsw[2] bit 11
	2	STICS North SSD Preamp Power Source: adwSTICSAnsw[2] bit 10
	1	?
	0	
17 11h	7	MSB STICS commanded valid event mode
	6	
	5	LSB Source: bySValEvent bit 0..2
	4	STICS South time disable ("1" = disable) Source: adwSTICSAnsw[3] bit 12
	3	STICS Equatorial Stop time disable ("1" = disable) Source: adwSTICSAnsw[3] bit 11
	2	STICS Equatorial Start B disable ("1" = disable) Source: adwSTICSAnsw[3] bit 10
	1	STICS Equatorial Start A disable ("1" = disable) Source: adwSTICSAnsw[3] bit 9
0	STICS North time disable ("1" = disable) Source: adwSTICSAnsw[3] bit 8	

EPIC Subcommutated HK		12h,13h Bytes 18,19	
Byte #	Bit #	Comments	
18 12h	7		
	6		
	5	STICS time calibrate enable Source: adwSTICSAnsw[4] bit 13	
	4	STICS slow rate enable Source: adwSTICSAnsw[4] bit 12	
	3	STICS multiple stop enable Source: adwSTICSAnsw[4] bit 11	
	2	STICS multiple start enable Source: adwSTICSAnsw[4] bit 10	
	1		
	0	STICS detector main bias power enable Source: adwSTICSAnsw[4] bit 8	
19 13h	7		
	6	STICS Group 2	Compression codes used for rate groups.  "0" = code A      "1" = code C
	5	STICS Group 1	
	4	STICS south bias disable Source: adwSTICSANSW[5] bit 12	
	3	STICS equatorial bias disable Source: adwSTICSAnsw[5] bit 11	
	2	STICS north bias disable Source: adwSTICSAnsw[5] bit 10	
	1	MSB STICS # of activated stepping sequence	
	0	LSB Source: byStepSeq, bit 0,1	

14h,15h  
Bytes 20,21

## EPIC Subcommutated HK

Byte #	Bit #	Comments
20 14h	7	
	6	
	5	
	4	
	3	
	2	
	1	
	0	STICS aperture status Source: adwSTICSAnsw[6] bit 8
21 15h	7	MSB STICS HVPS1 voltage monitor (north start MCP)
	6	
	5	
	4	
	3	
	2	
	1	
	0	LSB Source: adwSTICS[Answ[7]

16h,17h  
Bytes 22,23

## EPIC Subcommutated HK

Byte #	Bit #	Comments
22 16h	7	MSB STICS HVPS2 voltage monitor (equ. start MCP)
	6	
	5	
	4	
	3	
	2	
	1	
	0	LSB
		Source: adwSTICSAnsw[8]
23 17h	7	MSB STICS HVPS3 voltage monitor (south start MCP)
	6	
	5	
	4	
	3	
	2	
	1	
	0	LSB
		Source: adwSTICSAnsw[9]

18h,19h

EPIC Subcommutated HK

Bytes 24,25

Byte #	Bit #	Comments
24 18h	7	MSB STICS HVPS4 voltage monitor (north stop MCP)
	6	
	5	
	4	
	3	
	2	
	1	
	0	LSB
		Source: adwSTICSAnsw[10]
25 19h	7	MSB STICS HVPS5 voltage monitor (equatorial stop MCP)
	6	
	5	
	4	
	3	
	2	
	1	
	0	LSB
		Source: adwSTICSAnsw[11]

1Ah,1Bh  
Bytes 26,27

EPIC Subcommutated HK

Byte #	Bit #	Comments
26 1Ah	7	MSB STICS HVPS6 voltage monitor (south stop MCP)
	6	
	5	
	4	
	3	
	2	
	1	
	0	LSB
		Source: adwSTICSAnsw[12]
27 1Bh	7	MSB STICS HVPS7 voltage monitor (time-of-flight PS)
	6	
	5	
	4	
	3	
	2	
	1	
	0	LSB
		Source: adwSTICSAnsw[13]





1Eh,1Fh

EPIC Subcommutated HK

Bytes 30,31

Byte #	Bit #	Comments
30 1Eh	7	MSB STICS DPPS Current
	6	
	5	
	4	
	3	
	2	
	1	
	0	LSB
		Source: adwSTICSAnsw[19]
31 1Fh	7	MSB STICS Analog Electronics Thermistor
	6	
	5	
	4	
	3	
	2	
	1	
	0	LSB
		Source: adwSTICSAnsw[23]

20h,21h

EPIC Subcommutated HK

Bytes 32,33

Byte #	Bit #	Comments
32 20h	7	MSB STICS Sensor Thermistor #2 (unused)
	6	
	5	
	4	
	3	
	2	
	1	
	0	LSB
		Source: adwSTICSAnsw[24]
33 21h	7	MSB STICS Sensor Thermistor #3 (Backpanel)
	6	
	5	
	4	
	3	
	2	
	1	
	0	LSB
		Source: adwSTICSAnsw[25]

22h,23h

EPIC Subcommutated HK

Bytes 34,35

Byte #	Bit #	Comments
34 22h	7	MSB STICS Sensor Thermistor #4 (Detector)
	6	
	5	
	4	
	3	
	2	
	1	
	0	LSB
		Source: adwSTICSAnsw[26]
35 23h	7	MSB STICS LVPS +6 Voltage
	6	
	5	
	4	
	3	
	2	
	1	
	0	LSB
		Source: adwSTICSAnsw[31]

24h,25h

EPIC Subcommutated HK

Bytes 36,37

Byte #	Bit #	Comments
36 24h	7	MSB STICS -6 Voltage
	6	
	5	
	4	
	3	
	2	
	1	
	0	LSB
		Source: adwSTICSAnsw[32]
37 25h	7	MSB STICS +5.2 Voltage
	6	
	5	
	4	
	3	
	2	
	1	
	0	LSB
		Source: adwSTICSAnsw[33]

28h,29h

EPIC Subcommutated HK

Bytes 40,41

Byte #	Bit #	Comments
28 40h	7	MSB STICS LVPS -5.2 Voltage
	6	
	5	
	4	
	3	
	2	
	1	
	0	LSB
Source: adwSTICSAnsw[34]		
39 27h	7	MSB STICS LVPS +12 Voltage
	6	
	5	
	4	
	3	
	2	
	1	
	0	LSB
Source: adwSTICSAnsw[35]		

28h,29h

EPIC Subcommutated HK

Bytes 40,41

Byte #	Bit #	Comments
40 28h	7	MSB STICS LVPS SSD Bias Voltage (unused)
	6	
	5	
	4	
	3	
	2	
	1	
	0	LSB
		Source: adwSTICSAnsw[36]
41 29h	7	MSB STICS LVPS Input Current
	6	
	5	
	4	
	3	
	2	
	1	
	0	LSB
		Source: adwSTICSAnsw[37]

2Ah,2Bh

EPIC Subcommutated HK

Bytes 42,43

Byte #	Bit #	Comments
42 2Ah	7	MSB STICS LVPS -12 Voltage
	6	
	5	
	4	
	3	
	2	
	1	
	0	LSB
		Source: adwSTICSAnsw[38]
43 2Bh	7	MSB
	6	
	5	
	4	
	3	
	2	
	1	
	0	LSB
		Source : bySTICSLatchUp

2Ch,2Dh

EPIC Subcommutated HK

Bytes 44,45

Byte #	Bit #	Comments
44 2Ch	7	MSB bit 5 STICS north energy threshold
	6	
	5	
	4	
	3	
	2	LSB bit 0 Source : awSenCurCmd[S N DET THS]
45 2Dh	1	MSB bit 5 STICS equ. energy threshold
	0	
	7	LSB bit 0 Source: awSenCurCmd[S E DET THS]
	6	
	5	
	4	
3	3	MSB bit 5 STICS south energy threshold
	2	
	1	
	0	



2Eh,2Fh  
Bytes 46,47

## EPIC Subcommutated HK

Byte #	Bit #	Comments	
46 2Eh	7		
	6	LSB bit 0 Source : awSenCurCmd[S E DET THS]	
	5	MSB STICS commanded time time of flight calibration level	
	4		
	3		
	2	LSB Source: bySTOFCalLev bit 0...3	
	1		
	0		
	47 2Fh	7	MSB STICS commanded energy calibration level
		6	
		5	
4			
3			
2			
1			
0	LSB Source: awSenCurCmd[S IFC E REF]		

30h,31h

EPIC Subcommutated HK

Bytes 48,49

Byte #	Bit #	Comments
48 30h	7	
	6	
	5	
	4	
	3	MSB STICS + DPPS level bit 11..0 The spin is determined by the science record counter modulo 32.
	2	
	1	
	0	
49 31h	7	
	6	
	5	
	4	
	3	
	2	
	1	
	0	LSB

Source: awPosDPPSLev[dwSRNo&1Fh]

32h,33h

EPIC Subcommutated HK

Bytes 50,51

Byte #	Bit #	Comments
50 32h	7	
	6	
	5	
	4	
	3	MSB STICS - DPPS level bit 11..0
	2	
	1	
	0	
51 33h	7	
	6	
	5	
	4	
	3	
	2	
	1	
	0	LSB

Source: awNegDPPSLev[wSRNo&1Fh]

34h,35h

EPIC Subcommutated HK

Bytes 52,53

Byte #	Bit #	Comments
52 34h	7	MSB STICS +DPPS discharge count
	6	
	5	
	4	
	3	
	2	
	1	
	0	LSB
Source : byPosBreakDown		
53 35h	7	MSB STICS -DPPS discharge count
	6	
	5	
	4	
	3	
	2	
	1	
	0	LSB
Source : byNegBreakDown		

36h,37h

EPIC Subcommutated HK

Bytes 54,55

Byte #	Bit #	Comments
54 36h	7	MSB bit 15 Copy of H/W register MREG2
	6	
	5	
	4	
	3	
	2	
	1	
	0	
55 37h	7	
	6	
	5	
	4	
	3	
	2	
	1	
	0	LSB bit 0

38h,39h

EPIC Subcommutated HK

Bytes 56,57

Byte #	Bit #	Comments
56 38h	7	MSB bit 15 Copy of H/W register C_COM
	6	
	5	
	4	
	3	
	2	
	1	
	0	
57 39h	7	
	6	
	5	
	4	
	3	
	2	
	1	
	0	LSB bit 0

3Ah,3Bh  
Bytes 58,59

EPIC Subcommutated HK

Byte #	Bit #	Comments
58 3Ah	7	
	6	
	5	
	4	
	3	
	2	
	1	
	0	
59 3Bh	7	
	6	
	5	
	4	
	3	
	2	
	1	
	0	

3Ch,3Dh  
Bytes 60,61

EPIC Subcommutated HK

Byte #	Bit #	Comments
60 3Ch	7	
	6	
	5	
	4	
	3	
	2	
	1	
	0	
61 3Dh	7	
	6	
	5	
	4	
	3	
	2	
	1	
	0	



3Eh,3Fh  
Bytes 62,63

EPIC Subcommutated HK

Byte #	Bit #	Comments
62 3Eh	7	
	6	
	5	
	4	
	3	
	2	
	1	
	0	
63 3Fh	7	
	6	
	5	
	4	
	3	
	2	
	1	
	0	

40h,41h

EPIC Subcommutated HK

Bytes 64, 65

Byte #	Bit #	Comments
64 40h	7	MSB ICS commanded HV Limit #1 (north stop MCP)
	6	
	5	
	4	
	3	
	2	
	1	
	0	LSB
		Source: abyIHVLim[0]
65 41h	7	MSB ICS commanded HV Limit #2 (north start MCP)
	6	
	5	
	4	
	3	
	2	
	1	
	0	LSB
		Source: abyIHVLim[1]

42h,43h

EPIC Subcommutated HK

Bytes 66, 67

Byte #	Bit #	Comments
66 42h	7	MSB ICS commanded HV Limit #3 (south stop MCP)
	6	
	5	
	4	
	3	
	2	
	1	
	0	LSB
		Source: abyIHVLim[2]
67 43h	7	MSB ICS commanded HV Limit #4 (south start MCP)
	6	
	5	
	4	
	3	
	2	
	1	
	0	LSB
		Source: abyIHVLim[3]

44h,45h

EPIC Subcommutated HK

Bytes 68, 69

Byte #	Bit #	Comments
68 44h	7	MSB ICS commanded HV Limit #5 (time of flight PS)
	6	
	5	
	4	
	3	
	2	
	1	
	0	LSB
		Source: abyIHVLim[4]
69 45h	7	MSB ICS commanded HV target level #1 (north stop MCP)
	6	
	5	
	4	
	3	
	2	
	1	
	0	LSB
		Source: abyIHVDestLev[0]

46h,47h

EPIC Subcommutated HK

Bytes 70, 71

Byte #	Bit #	Comments
70 46h	7	MSB ICS commanded HV target level #2 (north start MCP)
	6	
	5	
	4	
	3	
	2	
	1	
	0	LSB
		Source: abyIHVDestLev[1]
71 47h	7	MSB ICS commanded HV target level #3 (south stop MCP)
	6	
	5	
	4	
	3	
	2	
	1	
	0	LSB
		Source: abyIHVDestLev[2]

48h,49h

EPIC Subcommutated HK

Bytes 72, 73

Byte #	Bit #	Comments
72 48h	7	MSB ICS commanded HV target level #4 (south start MCP)
	6	
	5	
	4	
	3	
	2	
	1	
	0	LSB
		Source: abyIHVDestLev[3]
73 49h	7	MSB ICS commanded HV target level #5 (time-of-flight PS)
	6	
	5	
	4	
	3	
	2	
	1	
	0	LSB
		Source: abyIHVDestLev[4]

4Ah,4Bh

EPIC Subcommutated HK

Bytes 74, 75

Byte #	Bit #	Comments
74 4Ah	7	MSB ICS Energy Calibration Level
	6	
	5	
	4	
	3	
	2	
	1	
	0	LSB Source: byIECalLev
75 4Bh	7	ICS I/F error check 0 : disabled mode 1 : enabled
	6	
	5	
	4	ICS calibration 0 : disabled read out mode 1 : enabled
	3	MSB ICS frozen mass PHA range
	2	LSB Source: byFixMassSpin
	1	MSB ICS frozen energy PHA range
	0	LSB Source: byFixEnergySpin

4Ch,4Dh

EPIC Subcommutated HK

Bytes 76, 77

Byte #	Bit #	Comments
76 4Ch	7	ICS LVPS over current ("1" if over current) Source: adwICS1Answ[2] bit 15
	6	ICS energy calibrate power enable Source: adwICSAnsw[2] bit 14
	5	ICS test logic enable Source: adwICSAnsw[2] bit 13
	4	ICS south SSD preamp power enable Source: adwICSAnsw[2] bit 12
	3	ICS electron detector preamp power enable Source adwICSAnsw[2] bit 11
	2	ICS north SSD preamp power enable Source: adwICSAnsw[2] bit 10
	1	ICS mass PHA range freeze enable Source: inverted byMassRotate, bit 1
	0	ICS energy PHA range freeze enable Source: inverted byEnergyRotate, bit 0
77 4Dh	7	MSB ICS commanded valid event mode
	6	
	5	LSB Source: byIValEvent
	4	ICS south stop disable Source: adwICSAnsw[3] bit 12
	3	
	2	ICS south start disable Source: adwICSAnsw[3] bit 10
	1	ICS north start disable Source: adwICSAnsw[3] bit 9
	0	ICS north stop disable Source: adwICSAnsw[3] bit 8



4Eh,4Fh  
Bytes 78, 79

## EPIC Subcommutated HK

Byte #	Bit #	Comments
78 4Eh	7	ICS PHA FIFO mode Source : byICHSPHAMode
	6	ICS position sensor (power) enable Source: adwICSAnsw[4] bit 14
	5	ICS time calibration power enable Source: adwICSAnsw[4] bit 13
	4	ICS slow rate analysis enable Source: adwICSAnsw[4] bit 12
	3	ICS multiple stop enable Source adwICSAnsw[4] bit 11
	2	ICS multiple start enable Source: adwICSAnsw[4] bit 10
	1	ICS detector bias high enable Source: adwICSAnsw[4] bit 9
	0	ICS automatic aperture control enable
79 4Fh	7	ICS Sector summation enable format scheme F Source: bySecSumF bit 7
	6	ICS head summation enable format scheme F Source: byHeadSumF bit 6
	5	ICS sector summation enable format scheme D Source: bySecSum D bit 5
	4	ICS head summation enable format scheme D Source: byHeadSumD bit 4
	3	ICS sector summation enable format scheme C Source: bySecSumC bit 3
	2	ICS head summation enable format scheme C Source: byHeadSumC bit 2
	1 0	

50h,51h

EPIC Subcommutated HK

Bytes 80, 81

Byte #	Bit #	Comments
80 50h	7	ICS south Motor Power Source: adwICSAnsw[6] bit 15
	6	2 ICS south position sensor status index bit
	5	1 11 closed/calibrate 01 open 10 foil
	4	0 00 10% + foil Source: adwICSAnsw[6] bit 4..6
	3	ICS north motor power Source: adwICSAnsw[6] bit 3
	2	2 ICS north position sensor status index bit
	1	1 11 closed/calibrate 01 open 10 foil
	0	0 00 10% + foil Source: adwICSAnsw[6] bit 0..2
81 51h	7	MSB ICS HVPS1 voltage monitor (north stop MCP)
	6	
	5	
	4	
	3	
	2	
	1	
	0	LSB Source: adwICSAnsw[7]

52h,53h

EPIC Subcommutated HK

Bytes 82, 83

Byte #	Bit #	Comments
82 52h	7	MSB ICS HVPS2 voltage monitor (north start MCP)
	6	
	5	
	4	
	3	
	2	
	1	
	0	LSB
Source: adwICSAnsw[8]		
83 53h	7	MSB ICS HVPS3 voltage monitor (south stop MCP)
	6	
	5	
	4	
	3	
	2	
	1	
	0	LSB
Source: adwICSAnsw[9]		

54h,55h

EPIC Subcommutated HK

Bytes 84, 85

Byte #	Bit #	Comments
84 54h	7	MSB ICS HVPS4 voltage monitor (south start MCP)
	6	
	5	
	4	
	3	
	2	
	1	
	0	LSB
		Source: adwICSAnsw[10]
85 55h	7	MSB ICS HVPS5 voltage monitor (time of flight PS)
	6	
	5	
	4	
	3	
	2	
	1	
	0	LSB
		Source: adwICSAnsw[11]

56h,57h

EPIC Subcommutated HK

Bytes 86, 87

Byte #	Bit #	Comments
86 56h	7	MSB ICS MCPPS & TOFPS Input Current
	6	
	5	
	4	
	3	
	2	
	1	
	0	LSB Source: adwICSAnsw[14]
87 57h	7	MSB ICS commanded time of flight calibration level
	6	
	5	
	4	LSB Source: byITOFCalLev bit 0..3
	3	MSB ICS GROUND
	2	
	1	
	0	LSB Source: adwICSAnsw[17] bit 0..3

58h,59h

EPIC Subcommutated HK

Bytes 88, 89

Byte #	Bit #	Comments
88 58h	7	MSB ICS motor current
	6	
	5	
	4	
	3	
	2	
	1	
	0	LSB
		Source: adwICSAnsw[19]
89 59h	7	MSB ICS Analog Electronics Thermistor #1
	6	
	5	
	4	
	3	
	2	
	1	
	0	LSB
		Source: adwICSAnsw[23]

5Ah,5Bh

EPIC Subcommutated HK

Bytes 90, 91

Byte #	Bit #	Comments
90 5Ah	7	MSB ICS sensor thermistor #2 (Backpanel)
	6	
	5	
	4	
	3	
	2	
	1	
	0	LSB
Source: adwICSAnsw[24]		
91 5Bh	7	MSB ICS sensor thermistor #3 (South Head)
	6	
	5	
	4	
	3	
	2	
	1	
	0	LSB
Source: adwICSAnsw[25]		

5Ch,5Dh

EPIC Subcommutated HK

Bytes 92, 93

Byte #	Bit #	Comments
92 5Ch	7	MSB ICS sensor thermistor #4
	6	
	5	
	4	
	3	
	2	
	1	
	0	LSB
Source: adwICSAnsw[26]		
93 5Dh	7	MSB ICS LVPS +6 Voltage
	6	
	5	
	4	
	3	
	2	
	1	
	0	LSB
Source: adwICSAnsw[31]		



5Eh,5Fh

EPIC Subcommutated HK

Bytes 94, 95

Byte #	Bit #	Comments
94 5Eh	7	MSB ICS LVPS -6V Voltage
	6	
	5	
	4	
	3	
	2	
	1	
	0	LSB
		Source: adwICSAnsw[32]
95 5Fh	7	MSB ICS LVPS +5.2 Voltage
	6	
	5	
	4	
	3	
	2	
	1	
	0	LSB
		Source: adwICSAnsw[33]

60h,61h

EPIC Subcommutated HK

Bytes 96, 97

Byte #	Bit #	Comments
96 60h	7	MSB ICS -5.2 Voltage
	6	
	5	
	4	
	3	
	2	
	1	
	0	LSB
		Source: adwICSAnsw[34]
97 61h	7	MSB ICS +12 Voltage
	6	
	5	
	4	
	3	
	2	
	1	
	0	LSB
		Source: adwICSAnsw[35]

62h,63h

EPIC Subcommutated HK

Bytes 98, 99

Byte #	Bit #	Comments
98 62h	7	MSB ICS LVPS SSD Bias Voltage
	6	
	5	
	4	
	3	
	2	
	1	
	0	LSB
Source: adwICSAnsw[36]		
99 63h	7	MSB ICS LVPS Input Current
	6	
	5	
	4	
	3	
	2	
	1	
	0	LSB
Source: adwICSAnsw[37]		

64h,65h

EPIC Subcommutated HK

Bytes 100,101

Byte #	Bit #	Comments
100 64h	7	MSB ICS -12 Voltage
	6	
	5	
	4	
	3	
	2	
	1	
	0	LSB
		Source: adwICSAnsw[38]
101 65h	7	MSB bit 5 ICS north energy threshold
	6	
	5	
	4	
	3	
	2	LSB bit 0
		Source: awSenCurCmd[I N DT THS]
	1	MSB bit 5 ICS electr. det. #1 energy threshold
	0	

66h,67h

EPIC Subcommutated HK

Bytes 102,103

Byte #	Bit #	Comments
102 66h	7	
	6	
	5	
	4	LSB  Source: awSenCurCmd[I E1 DT THS]
	3	MSB bit 5 ICS sourth energy threshold
103 67h	2	
	1	
	0	
	7	
	6	LSB  Source: awSenCurCmd[I S DET THS]
	5	MSB bit 5 ICS electr. det. #2 energy threshold
	4	
	3	
2		
1		
0	LSB  Source: awSenCurCmd[I E2 DT THS]	

68h,69h

EPIC Subcommutated HK

Bytes 104,105

Byte #	Bit #	Comments	
104 68h	7	ICS Group 2	Compression codes used for rate groups.  "0" = code A      "1" = code C
	6	ICS Group 1	
	5	ICS HVPS5 (time of flight) target status Source: byIHVPSStat bit 4	
	4	ICS HVPS4 (south start) target status Source: byIHVPSStat bit 3	
	3	ICS HVPS3 (south stop) target status Source: byIHVPSStat bit 2	
	2	ICS HVPS2 (north start) target status Source: byIHVPSStat bit 1	
	1	ICS HVPS1 (north stop) target status Source: byIHVPSStat bit 0	
	0	ICS reduced motor movement enable	
105 69h	7		
	6		
	5		
	4		
	3		
	2		
	1		
	0		

6Ah,6Bh

EPIC Subcommutated HK

Bytes 106,107

Byte #	Bit #	Comments
106 6Ah	7	MSB
	6	
	5	
	4	
	3	
	2	
	1	
	0	LSB
Source : byICSLatchUp		
107 6Bh	7	MSB awSCBCornerTab[(SRNO & 1F) *10 + 0]
	6	
	5	
	4	
	3	
	2	
	1	
	0	LSB

6Ch,6Dh

EPIC Subcommutated HK

Bytes 108,109

Byte #	Bit #	Comments
108 6Ch	7	MSB awSCBCornerTab[(SRNO & 1F)*10 + 1]
	6	
	5	
	4	
	3	
	2	
	1	
	0	LSB
109 6Dh	7	MSB awSCBCornerTab[(SRNO & 1F) *10 + 2]
	6	
	5	
	4	
	3	
	2	
	1	
	0	LSB



6Eh,6Fh

EPIC Subcommutated HK

Bytes 110,111

Byte #	Bit #	Comments
110 6Eh	7	MSB awSCBCornerTab[(SRNO & 1F) *10 + 3]
	6	
	5	
	4	
	3	
	2	
	1	
	0	LSB
111 6Fh	7	MSB awSCBCornerTab[(SRNO & 1F) *10 + 4]
	6	
	5	
	4	
	3	
	2	
	1	
	0	LSB

70h,71h

EPIC Subcommutated HK

Bytes 112,113

Byte #	Bit #	Comments
112 70h	7	MSB awSCBCornerTab[(SRNO & 1F) *10 + 5]
	6	
	5	
	4	
	3	
	2	
	1	
	0	LSB
113 71h	7	MSB awSCBCornerTab[(SRNO & 1F) *10 + 6]
	6	
	5	
	4	
	3	
	2	
	1	
	0	LSB

72h,73h

EPIC Subcommutated HK

Bytes 114,115

Byte #	Bit #	Comments
114 72h	7	MSB awSCBCornerTab[(SRNO & 1F) *10 + 7]
	6	
	5	
	4	
	3	
	2	
	1	
	0	LSB
115 73h	7	MSB awSCBCornerTab[(SRNO & 1F) *10 + 8]
	6	
	5	
	4	
	3	
	2	
	1	
	0	LSB

74h,75h

EPIC Subcommutated HK

Bytes 116,117

Byte #	Bit #	Comments
116 74h	7	MSB awSCBCornerTab[(SRNO & 1F) *10 + 9]
	6	
	5	
	4	
	3	
	2	
	1	
	0	LSB
117 75h	7	MSB awSRCCornerTab[(SRNO & F) * 5 + 0]
	6	
	5	
	4	
	3	
	2	
	1	
	0	LSB

76h,77h

EPIC Subcommutated HK

Bytes 118,119

Byte #	Bit #	Comments
118 76h	7	MSB awSRCCornerTab[ (SRNO & F) * 5 + 1]
	6	
	5	
	4	
	3	
	2	
	1	
	0	LSB
119 77h	7	MSB awSRCCornerTab[ (SRNO & F) * 5 + 2]
	6	
	5	
	4	
	3	
	2	
	1	
	0	LSB

78h,79h

EPIC Subcommutated HK

Bytes 120,121

Byte #	Bit #	Comments
120 78h	7	MSB awSRCCornerTab[ (SRNO & F) * 5 + 3]
	6	
	5	
	4	
	3	
	2	
	1	
	0	LSB
121 79h	7	MSB awSRCCornerTab[ (SRNO & F) * 5 + 4]
	6	
	5	
	4	
	3	
	2	
	1	
	0	LSB

7Ah,7Bh

Bytes 122,123

EPIC Subcommutated HK

Byte #	Bit #	Comments
122 7Ah	7	MSB DPU count of executed valid commands
	6	
	5	
	4	
	3	
	2	
	1	
	0	LSB
123 7Bh	7	MSB DPU 2nd to the last valid BC command identifier.
	6	
	5	
	4	
	3	
	2	
	1	
	0	LSB

7Ch,7Dh

EPIC Subcommutated HK

Bytes 124,125

Byte #	Bit #	Comments
124 7Ch	7	MSB DPU next to the last valid BC command identifier
	6	
	5	
	4	
	3	
	2	
	1	
	0	LSB
125 7Dh	7	MSB DPU last valid BC command identifier
	6	
	5	
	4	
	3	
	2	
	1	
	0	LSB



7Eh,7Fh

EPIC Subcommutated HK

Bytes 126,127

Byte #	Bit #	Comments
126 7Eh	7	MSB DPU number of invalid commands (invalidation during execution)
	6	
	5	
	4	
	3	
	2	
	1	
	0	LSB
127 7Fh	7	MSB DPU BC command identifier of last invalid command
	6	
	5	
	4	
	3	
	2	
	1	
	0	LSB

80h,81h

EPIC Subcommutated HK

Bytes 128,129

Byte #	Bit #	Comments
128 80h	7	MSB DPU error code for last invalid command
	6	
	5	
	4	
	3	
	2	
	1	
	0	LSB
129 81h	7	Watch dog enable 0 : watch dog disabled 1 : watch dog enabled
	6	MSB Reset Cause 0 : normal DPU on 1 : Latch Up
	5	LSB 2 : UVC 3 : Watchdog
	4	DPU NVRAM content error 0 --> no error 1 --> error
	3	MSB DPU D_PLDBAD address (bit 19..16) (segment address)
	2	
	1	
	0	LSB

82h,83h

EPIC Subcommutated HK

Bytes 130,131

Byte #	Bit #	Comments
130 82h	7	DPU D_PLDEAD address (bit 15..0)
	6	
	5	
	4	
	3	
	2	
	1	
	0	
131 83h	7	
	6	
	5	
	4	
	3	
	2	
	1	
	0	LSB

84h,85h

EPIC Subcommutated HK

Bytes 132,133

Byte #	Bit #	Comments
132 84h	7	
	6	
	5	
	4	
	3	
	2	
	1	
	0	
133 85h	7	
	6	
	5	Snapshot CFG load success 0 : ok, 1 : CRC error
	4	Current CFG load success 0 : ok, 1 : CRC error
	3	Snapshot CFG ICS reconfig 0 : ok, 1 : error
	2	Current CFG ICS reconfig 0 : ok, 1 : error
	1	Snapshot CFG STICS reconfig 0 : ok, 1 : error
0	Current CFG STICS reconfig 0 : ok, 1 : error	

86h,87h

EPIC Subcommutated HK

Bytes 134,135

Byte #	Bit #	Comments
134 86h	7	MSB DPU Reset-Counter
	6	
	5	
	4	
	3	
	2	LSB  Source: byResetCounter
	1	
	0	Test tables                    0 : disabled 1 : loaded status
135 87h	7	Low Level LU-Test status
	6	bit 7..4 :                    (15-value) is the time after which the current strobing will be activated.
	5	
	4	
	3	bit 3 :                        0 : test STICS classification (for this test, the time definition is not used)
	2	bit 2 :                        0 : test ICS classification (for this test, the time definition is not used)
	1	bit 1 :                        0 : test P memory
	0	bit 0 :                        0 : test P circuitry Source : byLUMask

88h,89h

EPIC Subcommutated HK

Bytes 136,137

Byte #	Bit #	Comments
136 88h	7	MSB D_PRGADR program load address (bit 19..4)
	6	
	5	
	4	
	3	
	2	
	1	
	0	
137 89h	7	
	6	
	5	
	4	
	3	
	2	
	1	
	0	LSB

8Ah,8Bh

EPIC Subcommutated HK

Bytes 138,139

Byte #	Bit #	Comments
138 8Ah	7	D_PRGADR program load address (bit 3..0)
	6	
	5	
	4	wAdrOffset Source : wAdrSegment
	3	
	2	Alarm Monitor Status 0 : disabled 1 : enabled
139 8Bh	1	Sector Clock Source 0 : S/C preferred 1 : fixed to internal
	0	Internal Sector Clock 0 : inactive 1 : active
	7	MSB STICS classification memory parity errors
	6	
	5	
	4	
	3	
	2	
	1	
	0	LSB Source : wSParityErrCnt

8Ch,8Dh

EPIC Subcommutated HK

Bytes 140,141

Byte #	Bit #	Comments
140 8Ch	7	MSB ICS classification memory parity error
	6	
	5	
	4	
	3	
	2	
	1	
	0	LSB
		Source : wIParityErrCnt
141 8Dh	7	MSB STICS irreparable classification memory parity errors
	6	
	5	
	4	
	3	
	2	
	1	
	0	LSB
		Source : wSFatalParErrCnt



8Eh,8Fh

EPIC Subcommutated HK

Bytes 142,143

Byte #	Bit #	Comments
142 8Eh	7	MSB ICS irreparable classification memory parity errors
	6	
	5	
	4	
	3	
	2	
	1	
	0	LSB  Source : wIFatalParErrCnt
143 8Fh	7	Enable Alarm channel 0 status 0 : off \ > for enable and alarm
	6	Alarm STICS analog electronics thermistor 1 : on /
	5	Enable Alarm channel 1 status 0 : off \ > for enable and alarm
	4	Alarm STICS thermistor 2 1 : on /
	3	Enable Alarm channel 2 status 0 : off \ > for enable and alarm
	2	Alarm STICS thermistor 3 1 : on /
	1	Enable Alarm channel 3 status 0 : off \ > for enable and alarm
	0	Alarm STICS thermistor 4 1 : on /

90h,91h

EPIC Subcommutated HK

Bytes 144,145

Byte #	Bit #	Comments
144 90h	7	Enable Alarm channel 4 status 0 : off \
	6	> for enable and alarm 1 : on / Alarm ICS analog electronics thermistor
	5	Enable Alarm channel 5 status 0 : off \
	4	> for enable and alarm 1 : on / Alarm ICS thermistor 2
	3	Enable Alarm channel 6 status 0 : off \
	2	> for enable and alarm 1 : on / Alarm ICS thermistor 3
	1	Enable Alarm channel 7 status 0 : off \
	0	> for enable and alarm 1 : on / Alarm ICS thermistor 4
145 91h	7	Enable Alarm channel 8 status 0 : off \
	6	> for enable and alarm 1 : on / Alarm STICS +6 Voltage
	5	Enable Alarm channel 9 status 0 : off \
	4	> for enable and alarm 1 : on / Alarm STICS north start MCP voltage
	3	Enable Alarm channel 10 status 0 : off \
	2	> for enable and alarm 1 : on / Alarm STICS north stop MCP voltage
	1	Enable Alarm channel 11 status 0 : off \
	0	> for enable and alarm 1 : on / Alarm STICS equatorial start MCP voltage

92h,93h

EPIC Subcommutated HK

Bytes 146,147

Byte #	Bit #	Comments
146 92h	7	Enable Alarm channel 12 status 0 : off \
	6	> for enable and alarm 1 : on / Alarm STICS equatorial stop MCP voltage
	5	Enable Alarm channel 13 status 0 : off \
	4	> for enable and alarm 1 : on / Alarm STICS south start MCP voltage
	3	Enable Alarm channel 14 status 0 : off \
	2	> for enable and alarm 1 : on / Alarm STICS south stop MCP voltage
	1	Enable Alarm channel 15 status 0 : off \
	0	> for enable and alarm 1 : on / Alarm STICS TOF PS voltage
147 93h	7	Enable Alarm channel 16 status 0 : off \
	6	> for enable and alarm 1 : on / Alarm ICS +6V current
	5	Enable Alarm channel 17 status 0 : off \
	4	> for enable and alarm 1 : on / Alarm ICS north stop MCP voltage
	3	Enable Alarm channel 18 status 0 : off \
	2	> for enable and alarm 1 : on / Alarm ICS north start MCP voltage
	1	Enable Alarm channel 19 status 0 : off \
	0	> for enable and alarm 1 : on / Alarm ICS south stop MCP voltage

94h,95h

EPIC Subcommutated HK

Bytes 148,149

Byte #	Bit #	Comments
148 94h	7	Enable Alarm channel 20 status 0 : off \
	6	> for enable and alarm 1 : on / Alarm ICS south start MCP voltage
	5	Enable Alarm channel 21 status 0 : off \
	4	> for enable and alarm 1 : on / Alarm ICS TOF PS voltage
	3	Enable Alarm channel 22 status 0 : off \
	2	> for enable and alarm 1 : on / Alarm STICS LVPS current
	1	Enable Alarm channel 23 status 0 : off \
	0	> for enable and alarm 1 : on / Alarm STICS MCPPS current
149 95h	7	Enable Alarm channel 24 status 0 : off \
	6	> for enable and alarm 1 : on / Alarm STICS DPPS current
	5	Enable Alarm channel 25 status 0 : off \
	4	> for enable and alarm 1 : on / Alarm ICS LVPS current
	3	Enable Alarm channel 26 status 0 : off \
	2	> for enable and alarm 1 : on / Alarm ICS MCPPS current
	1	Enable Alarm channel 27 status 0 : off \
	0	> for enable and alarm 1 : on / Alarm ICS motor current

96h,97h

EPIC Subcommutated HK

Bytes 150,151

Byte #	Bit #	Comments
150 96h	7	Enable Alarm channel 28 status 0 : off \ > for enable and alarm
	6	
	5	Enable Alarm channel 29 status 0 : off \ > for enable and alarm
	4	
	3	Enable Alarm channel 30 status 0 : off \ > for enable and alarm
	2	
	1	Enable Alarm channel 31 status 0 : off \ > for enable and alarm
	0	
151 97h	7	MSB Sun Sector
	6	
	5	
	4	
	3	MSB Parameter Index (bit 11..8)
	2	
	1	
	0	

98h,99h

EPIC Subcommutated HK

Bytes 152,153

Byte #	Bit #	Comments
152 98h	7	Parameter Index (bit 7..0)
	6	
	5	
	4	
	3	
	2	
	1	
	0	LSB
153 99h	7	MSB Parameter Byte 0
	6	
	5	
	4	
	3	
	2	
	1	
	0	LSB

9Ah,9Bh

EPIC Subcommutated HK

Bytes 154,155

Byte #	Bit #	Comments
154 9Ah	7	MSB    Parameter Byte 1
	6	
	5	
	4	
	3	
	2	
	1	
	0	LSB
155 9Bh	7	MSB    Parameter Byte 2
	6	
	5	
	4	
	3	
	2	
	1	
	0	LSB

9Ch,9Dh

EPIC Subcommutated HK

Bytes 156,157

Byte #	Bit #	Comments
156 9Ch	7	MSB    Parameter Byte 3
	6	
	5	
	4	
	3	
	2	
	1	
	0	LSB
157 9Dh	7	MSB    Parameter Byte 4
	6	
	5	
	4	
	3	
	2	
	1	
	0	LSB



9Eh,9Fh

EPIC Subcommutated HK

Bytes 158,159

Byte #	Bit #	Comments
158 9Eh	7	MSB    Parameter Byte 5
	6	
	5	
	4	
	3	
	2	
	1	
	0	LSB
159 9Fh	7	MSB    Parameter Byte 6
	6	
	5	
	4	
	3	
	2	
	1	
	0	LSB

A0h,A1h

EPIC Subcommutated HK

Bytes 160,161

Byte #	Bit #	Comments
160 A0h	7	MSB    Parameter Byte 7
	6	
	5	
	4	
	3	
	2	
	1	
	0	
161 A1h	7	MSB    Parameter Byte 8
	6	
	5	
	4	
	3	
	2	
	1	
	0	LSB

A2h,A3h

EPIC Subcommutated HK

Bytes 162,163

Byte #	Bit #	Comments
162 A2h	7	MSB    Parameter Byte 9
	6	
	5	
	4	
	3	
	2	
	1	
	0	LSB
163 A3h	7	MSB    Parameter Byte 10
	6	
	5	
	4	
	3	
	2	
	1	
	0	LSB

A4h,A5h

EPIC Subcommutated HK

Bytes 164,165

Byte #	Bit #	Comments
164 A4h	7	MSB    Parameter Byte 11
	6	
	5	
	4	
	3	
	2	
	1	
	0	LSB
165 A5h	7	MSB    Parameter Byte 12
	6	
	5	
	4	
	3	
	2	
	1	
	0	LSB

A6h,A7h

EPIC Subcommutated HK

Bytes 166,167

Byte #	Bit #	Comments
166 A6h	7	MSB    Parameter Byte 13
	6	
	5	
	4	
	3	
	2	
	1	
	0	LSB
167 A7h	7	MSB    Parameter Byte 14
	6	
	5	
	4	
	3	
	2	
	1	
	0	LSB

A8h,A9h

EPIC Subcommutated HK

Bytes 168,169

Byte #	Bit #	Comments
168 A8h	7	MSB    Parameter Byte 15
	6	
	5	
	4	
	3	
	2	
	1	
	0	LSB
169 A9h	7	MSB    Parameter Byte 15
	6	
	5	
	4	
	3	
	2	
	1	
	0	LSB

AAh,ABh

EPIC Subcommutated HK

Bytes 170,171

Byte #	Bit #	Comments
170 AAh	7	Science Record Counter (bit 23..16)
	6	
	5	
	4	
	3	
	2	
	1	
	0	
171 ABh	7	Science Record Counter (bit 15..8)
	6	
	5	
	4	
	3	
	2	
	1	
	0	

ACh,ADh  
Bytes 172,173

Byte #	Bit #	Comments
172 ACh	7	Science Record Counter (bit 7..0)
	6	
	5	
	4	
	3	
	2	
	1	
	0	LSB
173 ADh	7	MSB Subsector Offset for Sunpulse
	6	
	5	
	4	
	3	
	2	
	1	
	0	LSB



AEh,AFh

EPIC Subcommutated HK

Bytes 174,175

Byte #	Bit #	Comments
174 AEh	7	MSB D_SENCMD Answer (bit 31..24)
	6	
	5	
	4	
	3	
	2	
	1	
	0	
175 AFh	7	D_SENCMD Answer (bit 23..16)
	6	
	5	
	4	
	3	
	2	
	1	
	0	

EPIC Subcommutated HK		B0h,B1h Bytes 176,177
Byte #	Bit #	Comments
176 B0h	7	D_SENCOMD Answer (bit 15..8)
	6	
	5	
	4	
	3	
	2	
	1	
	0	
177 B1h	7	D_SENCOMD Answer (bit 7..0)
	6	
	5	
	4	
	3	
	2	
	1	
	0	LSB

B2h,B3h

EPIC Subcommutated HK

Bytes 178,179

Byte #	Bit #	Comments
178 B2h	7	MSB STICS classification control memory double errors
	6	
	5	
	4	
	3	
	2	
	1	
	0	LSB
179 B3h	7	MSB ICS classification control memory double errors
	6	
	5	
	4	
	3	
	2	
	1	
	0	LSB

B4h,B5h  
Bytes 180,181

## EPIC Subcommutated HK

Byte #	Bit #	Comments
180 B4h	7	MSB P-RAM single errors, compressed with scheme 'A'
	6	
	5	
	4	
	3	
	2	
	1	
	0	LSB
181 B5h	7	MSB P-ROM single errors, compressed with scheme 'A'
	6	
	5	
	4	
	3	
	2	
	1	
	0	LSB

EPIC Subcommutated HK		B6h,B7h Bytes 182,183
Byte #	Bit #	Comments
182 B6h	7	MSB bit 15 Number of automatic reconfigurations remaining
	6	
	5	
	4	
	3	
	2	
	1	
	0	
183 B7h	7	
	6	
	5	
	4	
	3	
	2	
	1	
	0	LSB (bit 0)

EPIC Subcommutated HK		B8h,B9h Bytes 184,185
Byte #	Bit #	Comments
184 B8h	7	MSB Alarm channel[(SRNO & 7)*4 +0] lower limit
	6	
	5	
	4	
	3	
	2	
	1	
	0	LSB
185 B9h	7	MSB Alarm channel[(SRNO & 7)*4 +0] upper limit
	6	
	5	
	4	
	3	
	2	
	1	
	0	LSB

BAh,BBh

EPIC Subcommutated HK

Bytes 186,187

Byte #	Bit #	Comments
186 BAh	7	MSB Alarm channel[(SRNO & 7)*4 +1] lower limit
	6	
	5	
	4	
	3	
	2	
	1	
	0	LSB
187 BBh	7	MSB Alarm channel[(SRNO & 7)*4 +1] upper limit
	6	
	5	
	4	
	3	
	2	
	1	
	0	LSB

BCh,BDh

EPIC Subcommutated HK

Bytes 188,189

Byte #	Bit #	Comments
188 BCh	7	MSB Alarm channel[(SRNO & 7)*4 +2] lower limit
	6	
	5	
	4	
	3	
	2	
	1	
	0	LSB
189 BDh	7	MSB Alarm channel[(SRNO & 7)*4 +2] upper limit
	6	
	5	
	4	
	3	
	2	
	1	
	0	LSB



BEh,BFh

EPIC Subcommutated HK

Bytes 190,191

Byte #	Bit #	Comments
190 BEh	7	MSB Alarm channel[(SRNO & 7)*4 +3] lower limit
	6	
	5	
	4	
	3	
	2	
	1	
	0	LSB
191 BFh	7	MSB Alarm channel[(SRNO & 7)*4 +3] upper limit
	6	
	5	
	4	
	3	
	2	
	1	
	0	LSB

## 5. DPU TIMING

This chapter provides some information about the DPU internal timing. Especially it provides useful information about dead times of the measurement periods which have to be taken into account if the actual event rates are to be calculated.

The timing information provided here was taken from traces with the HP processor emulation system on which the S/W was developed. The used S/W was the version of the 13th, March 1991. This differs from the version of the 14th, March in that program patch jumps were not yet implemented.

### 5.1 Sectorization timing

The following table provides basic information about the timing which depends on the S/C spin clock.

<u>EPIC unit</u>	<u>Spacecraft unit</u>	<u>Nominal time</u>
1 Science Record	16 S/C spins	96 sec
1 Spin	1 S/C spin	3 sec
1 Sector	1/16 S/C spin	187.5 ms

Table 35 : EPIC timing compared to S/C timing

A sector can roughly be subdivided into a time of measurement and a time of data readout where the measurement is disabled. The data readout is executed by the sector interrupt routine. This interrupt routine also handles the synchronization of measurement modes (e.g. ICS head summation) to science records. It therefore has more work to do as after 'normal' sectors if it reaches a spin boundary and even more if it reaches a science record boundary. The following table describes the timing for these cases.

Telemetry mode	STICS		ICS	
	Sector 0	sector 1 - 15	Sector 0	sector 1 - 15
Dual sensor	130.0 ± 0.2 mSec	18.2 ± 0.2 mSec	34.6 ± 0.2 mSec	18.2 ± 0.2 mSec
STICS only	130.0 ± 0.2 mSec	18.1 ± 0.2 mSec		
ICS only			34.6 ± 0.2 mSec	18.1 ± 0.2 mSec

Table 36 : Sector dead times

- x. ms start of sector interrupt routine
- x. ms disable STICS PHA & event classification hardware
- x. ms disable ICS PHA & event classification hardware
- x. ms increment sector counter
- x. ms end of sector interrupt routine

- x. ms enable STICS PHA & event classification hardware
- x. ms enable ICS PHA & event classification hardware
- x. ms start of next sector interrupt routine

- x. ms start of sector interrupt routine
- x. ms disable STICS PHA & event classification hardware
- x. ms disable ICS PHA & event classification hardware
- x. ms start to transmit DPPS step command
- x. ms increment sector counter
- x. ms increment spin counter

One S/C spin is subdivided into 16 sectors.

## 6. DPU special function registers

This chapter describes special DPU I/O ports which are no 8086 system standard. The following table gives a brief overview of all system I/O ports.

Address	Port Name	Access	Description
0000h,0002h	PIC	R/W	Base address of interrupt controller 82C59.
4000h,4001h, ...,400Fh	DMA	R/W	82C37 DMA controller
1000h,1002h, ...,1006h	TIM	R/W	82C54 16 bit timer
1E00h	SEGREG	WR	DMA page register
1600H	COA	WR	command interrupt acknowledge
1C00H	SIA	WR	sector interrupt acknowledge
3800h	FBAA	WR	telemetry A frame begin interrupt acknowledge
3A00h	VOA	WR	under voltage control interrupt acknowledge
3C00	FBAB	WR	telemetry B frame begin interrupt acknowledge
3000h	MREG1	RD	S/C signals, RAM single error counter
3200h	MREG2	RD	power status
		WR	reset RAM single error counters
3000h	SCICMD	WR	S/C interface control
3400h	COMREG	RD	S/C command interface
3600h	SUNREG	WR	Subsector offset of sunpulse
D000h	PREG1	WR	power switch register
2800H	WATCHDOG	WR	watchdog reset register
6000h	ICS_COM	WR	ICS command register
	ICS_DATA_L	RD	ICS command answer low word
6002h	ICS_RESET	WR	ICS command I/F reset
	ICS_DATA_H	RD	ICS command answer high word
6004h	ICS_STATUS	RD	ICS command I/F status
6800h	STICS_COM	WR	STICS command register
	STICS_DATA_L	RD	STICS command answer low word
6802h	STICS_RESET	WR	STICS command I/F reset
	STICS_DATA_H	RD	STICS command answer high word
6804h	STICS_STATUS	RD	STICS command I/F status
1200h	C_COM	R/W	classification control register
1280h	C_STAT	RD	classification status register
	S_CL_PAR	WR	reset STICS parity error
12C0h	S_CL_DEF	WR	reset STICS double error
12D0h	S_CL_INIT	WR	reset STICS classification (event generation)

1400h	S_PE_TOF	RD	STICS PHA event, TOF word
	S_PS_0	WR	STICS prior switches 0 - 15
1480h	S_PE_E	RD	STICS PHA event, energy word
	S_PS_1	WR	STICS prior switches 16 - 31
12A0h	I_CL_PAR	WR	reset ICS parity error
12E0h	I_CL_DEF	WR	reset TICS double error
12F0h	I_CL_INIT	WR	reset ICS classification (event generation)
1500h	I_PE_TOF	RD	ICS PHA event, TOF word
	I_PS_0	WR	ICS prior switches 0 - 15
1580h	I_PE_E	RD	ICS PHA event, energy word
	I_PS_1	WR	ICS prior switches 16 - 31
1800h	S_CL_PE	WR	clear STICS PHA interrupt
1A00h	I_CL_PE	WR	clear ICS PHA interrupt

Table 37 : DPU I/O ports

### 6.1 LU-Test Register (LUTEST)

Address : 0F000H

Access : 8 Bit, W/O

Purpose : To activate the low level Latch Up current sensors

Layout :

7	6	5	4	3	2	1	0
TIME				SP	IP	UP	UP

UPC                     $\mu$ P - Test, active "0"

UPM                     $\mu$ P - Memory Test, active "0"

IPM                    ICS Memory Test, active "0"

SPM                    STICS Memory Test, active "0"

TIME                    Test time (= TIME \* 2  $\mu$ s)

A low level latch up test is performed after a write operation to this register. However, if the 4 least significant bits were all set to 1, no latchup test is performed.

## 6.2 DPU Command Register (COMREG)

Address : 3400H  
 Access : 16 Bit, R/O  
 Purpose : supplies S/C commands to the DPU

Layout :

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
x	x	x	x	ER	DC	BC	EC	COMMAND						LSB	

COMMAND            command byte from S/C  
 ECS                Status of Error Checker  
                     0 : Error Checker is enabled  
                     1 : Error Checker is disabled  
 BC                 “1” if the received command was a BC  
 DC                 “1” if the received command was a DC  
 ERR                “0” if an command transmission error occurred, i.e. the command was not  
                     transmitted with 8 bits but with less or more

## 6.3 Message Register 1 (MREG1)

Address : 3000H  
 Access : 16 Bit, R/O  
 Purpose : Reports the telemetry status

Layout :

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ROM single				RAM single				TB	TA	SU	FT	FB	FW	FB	FW

ROM single error    Number of single errors in ROM  
 RAM single error    Number of single errors in RAM  
 FWA                 F0W0 - Pulse of telemetry A, active high  
 FBA                 Frame Begin Pulse of telemetry A, active high. This signal also causes a  
                     frame begin interrupt to the processor.  
 FWB                 F0W0 - Pulse of telemetry B, active high  
 FBB                 Frame Begin Pulse of telemetry B, active high. This signal also causes a  
                     frame begin interrupt to the processor.  
 FTC                 “Format C” signal for telemetry A, active high  
 SUN                 Sun Pulse Signal, active high. If this bit is set, the sun pulse occurred during  
                     the last sector. (The sunpulse is latched with every sector interrupt signal).  
 TAS                 Telemetry A status, “1” means telemetry A is enabled.  
 TBS                 Telemetry B status, “1” means telemetry B is enabled.

### 6.3 SCI-Control Register (SCICMD)

Address : 03000H  
 Access : 8 Bit, W/O  
 Purpose : To control the S/C interface

Layout :

7	6	5	4	3	2	1	0
x	x	x	x	x	TB	TA	EC

ECO enables (“1”) or disables (“0”) the error checker for the DPU command channel

TAO enables (“1”) or disables (“0”) telemetry A

TBO enables (“1”) or disables (“0”) telemetry B

### 6.5 Power Control Register (PREG1)

Address : 0D000H  
 Access : 8 Bit, W/O  
 Purpose : to switch the various software controlled power switches inside the DPU

Layout :

7	6	5	4	3	2	1	0
SWADR			0	x	x	x	SW

SWB Switch Bit, switches the selected power supply on (“1”) or off (“0”)

SWADR Switch Address, selects the power supply to be switched :

- 0 : unused
- 1 : ICS LVPS
- 2 : ICS MCPPS
- 3 : STICS ACTUATOR PS
- 4 : STICS LVPS
- 5 : STICS DPPS
- 6 : STICS MCPPS
- 7 : Instrument PS (main switch for all above)

## 6.6 Message Register 2 (MREG2)

Address : 3200H

Access : 16 bit, R/O

Purpose : mirrors the status of the power switches to the DPU

Layout :

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LU	PR	SW	HW	HV	SA	IL	SL	ED	BH	SH	IH	IM	SM	SD	EI

EIP	Epic Instrument Power
SDP	STICS Deflection Plate Power
SMP	STICS Microchannel Plate Power
IMP	ICS Microchannel Plate Power
IHP	ICS Supplement Heater Power
SHP	STICS Supplement Heater Power
BHP	Bakeout Heater Power
EDP	EPIC DPU Power
SLP	STICS Low Voltage Power
ILP	ICS Low Voltage Power
SAP	STICS Actuator Power
HVE	HV - Enable
	“1” : HV is enabled
	“0” : HV is disabled
HWS	“1” : DC timing circuit is active, hardware controlled relay may be currently switching
	“0” : DC timing circuit is inactive.
SWS	“1” : software timing circuit is active, software controlled relay is currently switching
	“0” : all software controlled relays are inactive
PRS	“0” : PROM1a is selected
	“1” : PROM1b is selected
LUR	0 : Last power on was by command
	1 : Last power on was after a latch up detection

Note : The “Power” - Bits in this register have the following meanings :

“0” : respective power is switched off

“1” : respective power is switched on



## 6.6 Classification Status Register (C\_STAT)

Address : 1280H

Access : 16 Bit, R/O

Purpose : mirrors the status of the classifications units to the DPU

Layout :

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
x	x	x	x	x	x	x	VI	DE	DE	PE	PE	PI	PS	IC	SC

SCR	STICS classification is running
ICR	ICS classification is running
PS	STICS PHA word received
PI	ICS PHA word received
PES	Parity error in STICS table memory
PEI	Parity error in ICS table memory
DES	Double error in STICS control memory
DEI	Double error in ICS control memory
VIP	Under voltage condition

Note : all Bits are active high

## 6.7 Classification Command Register (C\_COM)

Address : 1200H

Access : 16 bit, W/O

Purpose : to control the classification units

Layout :

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PAGE					VI	ED	ED	EP	EP	HC	HC	PE	CE	PE	CE

CES	“0” : Disable STICS classification “1” : Enable STICS classification
PES	“0” : Disable STICS PHA events “1” : Enable STICS PHA events
CEI	“0” : Disable ICS classification “1” : Enable ICS classification
PEI	“0” : Disable ICS PHA events “1” : Enable ICS PHA events
HCS	“0” : Allow STICS classification operation “1” : Halt STICS classification immediately This bit has priority over the CES bit !
HCI	“0” : Allow ICS classification operation “1” : Halt ICS classification immediately This bit has priority over the CEI bit !
EPS	“0” : Disable STICS parity error interrupts “1” : Enable STICS parity errors interrupts
EPI	“0” : Disable ICS parity errors interrupts “1” : Enable ICS parity errors interrupts
EDS	“0” : Disable STICS double errors interrupts “1” : Enable STICS double errors interrupts
EDI	“0” : Disable ICS Double errors interrupts “1” : Enable ICS double errors
VIE	“0” : Disable UVC interrupt “1” : Enable UVC interrupt
PAGE	selects page 0..31 of the classification control memories

**7. STICS Counting Rate Memory channels**

Rate	Channels (Direction 0 - 6)						
	0	1	2	3	4	5	6
HR0	16	272	528	784	1040	1296	1552
HR1	17	273	529	785	1041	1297	1553
HR2	18	274	530	786	1042	1298	1554

Rate	Channels (Direction 0 - 6)						
	0	1	2	3	4	5	6
SMR0	19	275	531	787	1043	1299	1555
SMR1	20	276	532	788	1044	1300	1556
SMR2	21	277	533	789	1045	1301	1557

Rate	Channels (Direction 0 - 6)						
	0	1	2	3	4	5	6
MR0	32	288	544	800	1056	1312	1568
MR1	33	289	545	801	1057	1313	1569
MR2	34	290	546	802	1058	1314	1570
MR3	35	291	547	803	1059	1315	1571
MR4	36	292	548	804	1060	1316	1572
MR5	37	293	549	805	1061	1317	1573
MR6	38	294	550	806	1062	1318	1574
MR7	39	295	551	807	1063	1319	1575
MR8	40	296	552	808	1064	1320	1576
MR9	41	297	553	809	1065	1321	1577
MR10	42	298	554	810	1066	1322	1578
MR11	43	299	555	811	1067	1323	1579
MR12	44	300	556	812	1068	1324	1580
MR13	45	301	557	813	1069	1325	1581
MR14	46	302	558	814	1070	1326	1582
MR15	47	303	559	815	1071	1327	1583
MR16	48	304	560	816	1072	1328	1584
MR17	49	305	561	817	1073	1329	1585
MR18	50	306	562	818	1074	1330	1586
MR19	51	307	563	819	1075	1331	1587
MR20	52	308	564	820	1076	1332	1588
MR21	53q	309	565	821	1077	1333	1589

MR22	54	310	566	822	1078	1334	1590
MR23	55	311	567	823	1079	1335	1591
MR24	56	312	568	824	1080	1336	1592
MR25	57	313	569	825	1081	1337	1593
MR26	58	314	570	826	1082	1338	1594
MR27	59	315	571	827	1083	1339	1595
MR28	60	316	572	828	1084	1340	1596
MR29	61	317	573	829	1085	1341	1597

Rate	Channels (Direction 0 - 6)						
	0	1	2	3	4	5	6
SI_DIAG0	112	368	624	880	1136	1392	1648
SI_DIAG1	113	369	625	881	1137	1393	1649
SI_DIAG3	114	370	626	882	1138	1394	1650
SI_DIAG4	115	371	627	883	1139	1395	1651
SI_DIAG5	116	372	628	884	1140	1396	1652
SI_DIAG6	117	373	629	885	1141	1397	1653
SI_DIAG7	118	374	630	886	1142	1398	1654

Rate	Channels (Direction 0 - 6)						
	0	1	2	3	4	5	6
BR0	0	256	512	768	1024	1280	1536
BR1	1	257	513	769	1025	1281	1537
BR2	2	258	514	770	1026	1282	1538
BR_DIAG	3	259	515	771	1027	1283	1539

## **8. Startup sequence**

After the DPU got a RESET, it does the basic initialization first. The following steps are executed in the given order :

1. Interrupts are disabled.
2. Data segment and stack segment are setup.
3. DPU scratch pad memory (128kB) is initialized to 0.
4. All interrupt sources are reset to inactive state.
5. The 80C86 supporting hardware (82C54, 82C59, 82C37) is initialized.
6. The job manager and his priority levels are initialized.
7. All interrupt service routines and their interrupt vectors are initialized.
8. The classification hardware is initialized and disabled.
9. The configuration variables are set to the default ROM configuration
10. The default sensor command telegrams (HK & Accumulator readout for ICS & STICS, DPPS setting for STICS) are installed.
11. Interrupts are enabled.
12. The telemetry interface is activated.
13. The sector, spin and science record serving jobs are initialized.
14. The classification memory is initialized to default values (“test tables”).
15. The appropriate configuration image is loaded from the battery backup ram.
16. The DPU operational status is set according to the loaded configuration image.
17. The STICS sensor operational status is set according to the loaded configuration image.
18. The ICS sensor operational status is set according to the loaded configuration image.
19. Instrument operation starts

Some of the most important steps are steps 11,12,13 and steps 15-18. After the interrupts are enabled (step 11), the DPU will start to service the sector interrupt. This means that

20. the ICS accumulator readout is started
21. the STICS accumulator readout is started
22. the STICS DPPS voltage step is set once every spin.

After the telemetry interface is enabled (step 12) the DPU starts serving the status channel bytes and sends zeroes on the data channel.

After the default sector, spin and science record jobs are installed (step 13), the DPU

23. starts reading HK from ICS in every sector 1
24. starts reading HK from STICS in every sector 1

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25. starts formatting EDBs (experiment data blocks) and delivers the formatted EDBs to the telemetry interface serving process

In step 15 the appropriate configuration image is loaded from the non volatile (battery backed up) RAM. This stores two configurations : one configuration the DPU was in before the last switch off or RESET occurred (“current configuration”) and one which was saved by command (“snapshot configuration”). The third possible configuration is the one which is stored in ROM (“ROM configuration”) and to which all status variables are already set to when the initialization process reaches step 15.

The configuration is chosen with respect to the reason which caused the RESET :

26. The ROM configuration is chosen if
  - o the CRC of at least one of the configurations stored in the nonvolatile RAM is incorrect.
27. The current configuration is chosen if
  - o the RESET was caused by a previous latch up switch off.
  - o the RESET was caused by a previous UVC switch off
  - o the RESET was caused by a watchdog interrupt
28. The snapshot configuration is chosen if
  - o the RESET was caused by a commanded DPU switch off/on sequence.

The snapshot configuration can also be installed by command while the DPU is running.

### **8.1 Setting the DPU operational state**

The configuration image for the DPU operational state will store the following :

- o classification table parameters for ICS
- o classification table parameters for STICS
- o the current mode of the data formatting process
- o the currently used compression schemes
- o the current PHA mode for ICS
- o the current PHA mode (range definitions) for STICS
- o the current mode of housekeeping formatting (fixed HK index)
- o the latch up sensing operational mode (enabled / disabled)
- o the telemetry activation status
- o the sun sector position and the subsector offset
- o the power status

- o the alarm monitor status
- o the state of the memory fault interrupts (enable/disable)

This will be more detailed in future versions of this manual.

## 8.2 Setting the ICS sensor operational state

The ICS sensor status is commanded in the following order :

1. C00/C07 North, Equatorial and South preamplifier power set simultaneously with the C07/C00 command to the state stored in the configuration image.  
ROM configuration default value : all disabled.
2. C0F/C08 The time preamplifiers #0-#2 are set simultaneously to the state stored in the loaded configuration image.  
ROM configuration default value : all disabled.
3. C12/C10 The time preamplifier #4 is set to the state stored in the loaded configuration image.  
ROM default value : disabled
4. C20 Both motor powers (North / South) are set to OFF state (independent of the configuration image)
5. C2B/C28 The multiple event enable start and stop switches are set simultaneously to the state stored in the loaded configuration image.  
ROM default value : start disabled, stop disabled
6. C33/C30 The test logic and the calibrate energy switches are simultaneously set to the state stored in the configuration image.  
ROM default value : test logic disabled, calibrate energy disabled.
7. C38 The motor phases are both set to 0 (independent of the configuration image),
8. C49/C48 The SSD Bias is set to the state stored in the configuration image.  
ROM default value : SSD Bias Low (C48 cmd).
9. C51/C50 The slow rate mode is set to the state stored in the configuration image.  
ROM default value : slow rate mode disabled.

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| 10. | C59/C58 | The calibrate oscillator is set to the state stored in the configuration image.<br>ROM default value : disabled.  |
| 11. | C68     | The position led power is disabled (independent of the configuration image).  |
| 12. | A87/A80 | The valid event logic is set to the state stored in the configuration image.<br>ROM default value : valid event mode 0.   |
| 13. | A0x     | The time-of-flight calibration level is set to the state stored in the configuration image.<br>ROM default value : 0  |
| 14. | 7xx     | The energy calibration level is set to the state stored in the configuration image.<br>ROM default value : 0  |
| 15. | 83F/800 | The north detector analog threshold is set to the state stored in the configuration image.<br>ROM default value : 0.  |
| 16. | 87F/840 | The electron detector threshold #1 is set to the state stored in the configuration image.<br>ROM default value : 0  |
| 17. | 8BF/880 | The south detector analog threshold is set to the state stored in the configuration image.<br>ROM default value : 0   |
| 18. | 8FF/8C0 | The electron detector threshold #2 is set to the state stored in the configuration image.<br>ROM default value : 0  |
| 19. | B1F/B00 | The MCPPS & TOFPS enables are set one after the other (MCPPS0 - 3, TOFPS) to the values stored in the loaded configuration image. The interval between two switches will be 400 $\mu$ s. If HV is not enabled, the INSTRUMENT POWER is switched off or the MCP power is switched off, the ICS initialization will abort after this step.<br>ROM default value : all PS off  |
| 20. | 4xx/0xx | The MCPPS references (north start, south start, north stop, south stop) and the TOFPS reference are concurrently stepped to the level stored in the configuration image.<br>ROM default value : level 0 for all references<br>Problem : What is the “current level” of the references the DPU should assume after a RESET. Currently we will assume level 0, but this might be dangerous. To be discussed with APL. |



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21. 500/600 Both motor power levels are set to level 0 (independent of the configuration image).

### 8.3 Setting the STICS sensor operational state

The STICS sensor status is commanded in the following order :

1. C00/C07 North, Equatorial and South preamplifier power set simultaneously with the C07/C00 command to the state stored in the configuration image.  
ROM configuration default value : all disabled.
2. C0F/C08 The time preamplifiers #0-#2 are set simultaneously to the state stored in the loaded configuration image.  
ROM configuration default value : all disabled.
3. C13/C10 The time preamplifiers #3-#4 are simultaneously set to the state stored in the loaded configuration image.  
ROM default value : disabled
4. C2B/C28 The multiple event enable start and stop switches are set simultaneously to the state stored in the loaded configuration image.  
ROM default value : start disabled, stop disabled
5. C31/C30 The test logic switch is set to the state stored in the configuration image.  
ROM default value : test logic disabled, calibrate energy disabled.
6. C3F/C38 The detector bias power disables (north, equatorial, south) are simultaneously set to the state stored in the loaded configuration image.  
ROM default value : detector bias power disabled.
7. C41/C40 The SSD Bias switch is set to the state stored in the loaded configuration image.  
ROM default value : off
8. C49/C48 The SSD Bias is set to the state stored in the configuration image.  
ROM default value : SSD Bias Low (C48 cmd).
9. C51/C50 The slow rate mode is set to the state stored in the configuration image.  
ROM default value : slow rate mode disabled.

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|-----|---------|--|
| 10. | C59/C58 | The calibrate oscillator is set to the state stored in the configuration image.<br>ROM default value : disabled.   |
| 11. | A87/A80 | The valid event logic is set to the state stored in the configuration image.<br>ROM default value : valid event mode 0.  |
| 12. | A0x     | The time-of-flight calibration level is set to the state stored in the configuration image.<br>ROM default value : 0   |
| 13. | 7xx     | The energy calibration level is set to the state stored in the configuration image.<br>ROM default value : 0   |
| 14. | 83F/800 | The north detector analog threshold is set to the state stored in the configuration image.<br>ROM default value : 0.   |
| 15. | 87F/840 | The equatorial detector threshold is set to the state stored in the configuration image.<br>ROM default value : 0  |
| 16. | 8BF/880 | The south detector analog threshold is set to the state stored in the configuration image.<br>ROM default value : 0  |
| 17. | B7F/B00 | The Mini HVPS enables are set one after the other to the states stored in the loaded configuration image. The interval between two switches will be 400 $\mu$ s. If HV is not enabled, the INSTRUMENT POWER is switched off or the STICS MCP power is switched off, the STICS initialization will abort after this step.<br>ROM default value : all PS off |
| 18. | B83/B80 | The DPPS enables are set one after the other to the states stored in the loaded configuration image. The interval between two switches will be 400 $\mu$ s. If HV is not enabled, the INSTRUMENT POWER is switched off or the STICS DPPS power is switched off, the STICS initialization will abort after this step.<br>ROM default value : all PS off     |
| 19. | 7xx/0xx | The MCPPS references (north start, equ. start, south start, north stop, equ. stop, south stop) and the TOFPS reference are concurrently stepped to the level stored in the configuration image.<br>ROM default value : level 0 for all references  |

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Problem : What is the “current level” of the references the DPU should assume after a RESET. Currently we will assume level 0, but this might be dangerous. To be discussed with UMD.

## **9. Change for Sensor Commanding**

The process structure for sensor commanding changes with the 6.11.90. Up to that time, command emitting procedures were not allowed to send commands any time (e.g. motor control) and procedures which emitted synchronized commands were not able to check whether their commands really had been transmitted.

This is changed with the new scheme which will be described now.

### **9.1 Command classes**

Commands to switch the sensor operational mode are initiated during DPU initialization and from within DPU command procedures. The success of every such single command should be checked by the emitting processes. These commands are often synchronized with the measurement and have to be sent out during a measurement deadtime. Therefore they have to be collected in a buffer until the next deadtime is reached. Then they should be sent out as fast as possible, i.e. with a high priority (foreground commands).

Some other commands are also “single commands” and don’t have to be synchronized with the measurement. They are executed with relatively low priority (background commands).

Another class of commands are those which, on a procedure’s demand, should be sent out as soon as possible (real-time commands). The best example for this are the motor control commands, where it is important to keep the motor phases lengths as equal as possible. This kind of commands should have the highest priority.

The majority of commands to be sent out to the sensors are housekeeping and accumulator readout commands. There is no need to control the success of every single command but only the success of groups of commands (command telegrams), e.g. the sectored accumulator read out commands. It is sufficient to know about the success of the whole telegram. Since it is important to the measurement at what time these telegrams were transmitted to the sensor, command telegrams should have a priority between the real-time commands and the synchronized single commands.

### **9.2 Command transmission module**

The command transmission module will consist of procedures to send out command telegrams and single commands and to check the successful transmission. These procedures are :

fSendTelegram	a procedure which accepts a command telegram as parameter and puts the telegram into a queue of telegrams. This function returns a telegram ID which can be used to request the transmission status of that telegram.
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fTelegramStatus	a procedure which reports the transmission status of a given telegram. The telegram ID is passed as a parameter to fTelegramStatus
fSendCommand	a procedure which accepts a single command as parameter and puts the command into a queue of commands. This functions returns a command ID which can be used to test the transmission status of the command.
fCommandStatus	a procedure which reports the transmission status of a command. The command ID is passed as a parameter. This procedure also returns the command answer if the command was successful.
fSendCommandAndWait	this function simply calls fSendCommand and fCommandStatus. If the command can't be transmitted successfully (time-out) fSendCommandAndWait reports an error.

The requirements for the EPIC DPU software are defined in the “ENERGETIC PARTICLES AND ION COMPOSITION EXPERIMENT (EPIC) SOFTWARE REQUIREMENTS and DATA DEFINITION DOCUMENT”. The following is based on the preliminary revision of this manual, parts are already adopted to Revision A.

## **10. Real time aspects**

One of the main aspects to take care about in the DPU software is real-time. The two main time bases are the telemetry interface and the S/C spin clock. Both are synchronous repetitively (the spin may vary +/- 5%) but asynchronous to each other.

On the other hand, there are several fully asynchronous events (sorted by frequency) :

- PHA Event
- Incoming DPU commands
- H/W - Errors (Latch Up, SEU)
- Emergency Switch Off (UVC)

Since it is not possible to predict all possible combinations of synchronous and asynchronous events, the DPU software will watch itself if it carries out all necessary tasks in time. These checks will be done on spin-related boundaries (sectors, spins and science records). The test phase of the DPU software will end, if under no test conditions real-time violations can be detected.

Discussions brought up a priority scheme of tasks to be executed. The following list describes the priority of the different tasks in the system software. Priority 0 is the highest, priority 15 the lowest priority. Every priority level is able to interrupt an other level if a task of the assigned priority has to be carried out. For the non-hardware controlled levels, this is organized by a central module, called “job manager”. It receives information about the ongoing events (command reception, new sector, new spin,

new science record) and activates the different levels. From the status of the job manager it may be decided whether DPU keeps “real time” or not.

Because commands may cause actions of long duration, they may be divided into a “pre-execution phase” where parameters are interpreted and calculations are done and an “execution phase” where the result of the forgoing phase becomes valid. An example for this is the calculation of the STICS S-Table for every voltage step. The table calculation is done during the spin and the table is copied into the classification memory at the start of the next sector 0.

#### Priority H/W-Int Task

0	NMI	Watchdog-Function. This task may be deactivated by hardware Execution time : < 200 $\mu$ s
1	INT0	UVC / Classification Error Interrupt. Depending on the type of interrupt occurred, the UVC event or a classification error interrupt is served Execution time : < 200 ms for UVC, < 100 $\mu$ s for error servicing, the error will be serviced by the background program. The classification which caused the error will be deactivated during repair and will be reactivated with the first science record start after repair.
2	INT1	Timer 0. This Timer is responsible to generate the sector dead time and, in emergency situations, the artificial sector interrupt. Execution time : < 150 $\mu$ s
3	INT2	Frame Begin Interrupt. Depending on the current frame number and on which telemetry has to be served, this procedure prepares the DMA to send out the next data bytes. This procedure increments the HK subcom index and frees an EDB buffer, if it has been fully transmitted. Additionally, in every 4th interrupt of telemetry A, the low level LU detection for the $\mu$ P RAM/ROM and for the $\mu$ P circuitries will be done. Execution time : < 300 $\mu$ s for status channel servicing, < 500 $\mu$ s for science channel servicing.
4	INT3	Command Interrupt. This procedure fetches the DPU command bytes from telemetry, validates and interprets them. The command and command parameter bytes are filled into command buffers depending on the execution/preparation priority of the received command.

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- Execution time : < 300  $\mu$ s
- 5 INT4 Timer 1. This Timer is responsible to generate the 400  $\mu$ s time out for sensor servicing. It is only active while any sensor is being serviced.  
Execution time : < 200  $\mu$ s
- 6 INT5 Sector Interrupt. This procedure handles the central “science timing”. It generates sectors, spins, measurement spins and science records. In addition it performs sun pulse synchronization. During the sector interrupt routine everything is done which is needed to end the last sector and to prepare the measurement for the following sector. Equivalences exist for measurement spins and science records. After the counting memory has been read out, the low level LU detection for the classification memory will be executed. This will be done during sensor servicing and will therefor not lengthen the sector dead time.  
Execution time : < 94 ms for sector 0, < 20 ms for all other sectors.
- 7 INT6 PHA Interrupt. This interrupt procedure handles the PHA events of sensors and places the unformatted PHA data into a sector- and range- oriented buffer.  
Execution time : < 200  $\mu$ s
- 8 INT7 Timer 2. This timer is used for varying tasks, e.g. the time-outs for relay switching etc.  
Execution time : < 150  $\mu$ s
- 9 - Execution of commands which are to be carried out immediately.  
Execution time : < 1ms
- 10 - Sector Tasks. In this level, all tasks which are to be executed (repetitively or not) on a sector boundary. However, these are tasks which are carried out during measuring. All other sector oriented tasks are done during the sector interrupt (see level 6). The currently known tasks are :  
- accumulation of sectored science rates and engineering rates.  
- sensor HK readout  
Execution time : any, have to be ready until next sector boundary, DPU self controlled
- 11 - Spin Tasks. Same as for Sector Tasks, but for spins. The currently known tasks are :  
- accumulation of unsectored science rates and engineering rates.  
- precalculation of the S-Table for the next STICS voltage step

- 
- EDB - formatting  
Execution time : any, have to be ready until next spin boundary, DPU self controlled
  - 12 - Science Record Tasks. Same as for sector tasks, but for science records. The currently known tasks are :
    - HK Buffer switching  
Execution time : any, have to be ready until next science record boundary, DPU self controlled
  - 13 - Preexecution of commands with a small amount of parameters and with a low preexecution time. Execution will be in level 9, 10 or 11.  
Execution time : < 100 ms
  - 14 - Preexecution of commands with a large amount of parameters and with a long preexecution time. Execution will be in level 9,10 or 11.  
Execution time : any
  - 15 - Background program. It is responsible for carrying out the tasks with very low priority. The currently known are :
    - memory scrubbing
    - handling of double memory error in classification control unit
    - handling of parity error in classification.
 Execution time : any

The measurement cycles are based on the S/C spin timing. All DPU tasks are organized in respect to that timing while the instruments are active. If any condition occurs which will lead to an unsynchronized status, measurement spins will be dropped.

Level 6 (sector interrupt) is the point, where it is decided whether to measure in the next spin or to drop a spin. This depends on the central "Instrument Ready" condition, which is composed of several flags. If one of them is set when the next sector 0 comes up, the next spin will be dropped. The currently known flags are :

- Re-found sun at wrong position : After the sun pulse was lost, we re-found it in a wrong sector. The next spin will be in "SUN SEARCH" mode.
- Motor has to be moved : During the next spin, one of the ICS motors has to be moved. The next spin will be in "INSTRUMENT IDLE" mode

- Telemetry is not ready : The telemetry is not in data mode or the S/C's spin rate is too high. The next spin will be in "INSTRUMENT IDLE" mode.
- Classification Tables have to be / are being recalculated and/or to be repaired : Due to double error and/or parity error in the classification memory, the next spin (or the next few spins) have to be dropped. They will be in "INSTRUMENT IDLE" mode.
- Both instruments are or are to be switched off : If both instruments are switched off, the next spins will be in "INSTRUMENT IDLE" mode until one of the instruments is reactivated.
- DPU has to be switched off : This is a synchronized DPU switch-off procedure. After re-powering, the first spin will be in "SEARCH SUN" mode. "INSTRUMENT IDLE" mode will follow, until the instrument is fully initialized. Then the spin mode switches to "INSTRUMENT ACTIVE"

These conditions may be flagged from any module, independent of its execution priority.

## **11. Memory assignment**

Science data buffering has the most impact on the needed size of data buffers. These sizes may be calculated from the defined readout schemes. To keep the sector dead time small, all counting memory channels are first copied as raw data to a sector buffer, from which they then are processed further. For simplicity, all uncompressed rates are stored in double words, each occupying 4 bytes.

### **11.1 STICS rates data buffers**

For STICS, 36 science rates are defined. Most of these (30 MR) are read out on a spin by spin basis, others are read out with equatorial and polar direction information (HR, SMR, BR). Because the latter ones vary on command (which is not yet defined (?)), all 36 rates will be read out redundantly when the spin boundary is reached.

This scheme leads to the following memory consumption:

Rate	No. of Rates	Polar Dir.	Equ. Dir.	Sector Buffer	Accumul Buffer
HR	3	6	16	72	768 x 2
SMR	3	3	8	36	288 x 2
MR	36	1	1	144	144 x 2
BR	3	3	8	36	288 x 2
ER	21	-	1	84	84 x 2
Total memory needed (Bytes)	372	3144			

Table 38 : STICS buffer assignment in NORMAL MODE



Remark : 1. "x 2" is needed for applying exchange buffer techniques.

153. The two channels multiplexed on HR1 are read out every sector, but will need only one accumulation buffer

Rate	No. of Rates	Polar Dir.	Equ. Dir.	Sector Buffer	Accumul Buffer
HR	5	6	16	120	1920 x 2
MR	36	1	1	144	144 x 2
BR	3	3	8	36	288 x 2
ER	21	-	1	84	84 x 2
Total memory needed (Bytes)	300	4704			

Table 39 : STICS buffer assignment in STICS SINGLE SENSOR MODE

### 11.2 ICS rates data buffers

The ICS readout scheme is not as simple as the STICS ones is and is divided into several different readout schemes which need different buffers sizes. Since it is not possible to buffer all data of one science record, EDB data for ICS will be divided into three areas :

- o area 1, which data was collected over 2 spins
- o area 2, which data was collected over 16 spins
- o area 4, which data was collected over 32 spins

Readout Scheme	No. of Rates	Sectors Summed	Spins Summed	Head Summed	# of Aquis.	Sector Buffer	Accu. Buffer
A	2	1	1	2	2	16	256x2
B	1	2	1	2	2	8	64x2
B	1	2	1	-	2	4	64x2
C	8	1(2,1)	2(1,1)	1(1,2)	1(2,2)	64	1024x2
D	40	1(2,1,2)	16(8,8,4)	1(1,2,2)	1(2,2,4)	320	5120x2
D	4	1(2)	16(8)	-	1(2)	16	256x2
E	25	1(2,1,2)	32(16,16,8)	1(1,2,2)	1(2,2,4)	200	3200x2
E	1	1(2)	32(16)	-	1(2)	4	64x2
Total memory (Bytes)	632	20096					

Table 40 : ICS buffer assignment in NORMAL MODE

Readout Scheme	No. of Rates	Sectors Summed	Spins Summed	Head Summed	# of Aquis.	Sector Buffer	Accu. Buffer
A							
B							
B							
C							
D							
D							
E							
E							
Total memory (Bytes)	<1024	<32768					

Table 41 : ICS buffer assignment in ICS SINGLE SENSOR MODE (TBD)

### 11.3 STICS PHA acquisition

Referring to “STICS PHA Service” prepared by IDA / 26.3.90, STICS needs the following amount of Memory for PHA servicing :

$$4096 \text{ byte} + 64 \text{ byte} = 4160 \text{ Byte}$$

### 11.4 ICS PHA acquisition

Referring to “ICS PHA Service” prepared by IDA / 26.3.90, ICS needs the following amount of Memory for PHA servicing :

$$4096 \text{ byte} + 256 \text{ byte} = 4352 \text{ Byte}$$

## 11.5 DPU Buffers

Some buffers are needed for DPU internal organization. These are :

Purpose	Bytes needed
Interrupt vectors	1024
Processor Stack	< 2048
Variables	< 8192
Command parameter buffer	1024
Job manager lists	1400
EDB Buffers	$960 \times 4 = 3840$
Classification scratch tables	TBD TUB < 32768
Housekeeping buffer telemetry A	$256 \times 2 = 512$
Housekeeping buffer telemetry B	$64 \times 2 = 128$
Sensor command tables	$2 \times 128 \times 3 = 768$
Sensor command answers (HK)	$2 \times 64 \times 2 = 256$
Sensor command answers (ER)	$2 \times 32 \times 4 = 256$
Total DPU (Byte)	< 52216

Table 42 : DPU RAM buffer

## 11.6 Total memory consumption

STICS rates	5004
ICS rates	< 33792
STICS PHA	4160
ICS PHA	4352
DPU	< 52216
Total (Byte)	< 99524

Table 43 : Total memory consumption in EPIC DPU

Since 128 kByte (131072 Byte) are available in the EPIC DPU, we have a minimum of  $131072 - 99524 = 31548$  Byte spare memory.

### 11.7 Permanent Powered RAM

Item	Variable	Values	Default
HVPS upper limit	abyStHVLim[7]	0 <= x <= 255	0
HVPS voltage set	abyStHVSet[7]	0 <= x <= 255	0
Energy threshold	abyStEThr[3]	0 <= x <= 63	8
Valid Event Logging	byStValEvLog	0 <= x <= 7	1
E-Calibration Level	byStECalLvl	0 <= x <= 255	TBD UMD
TOF Clbr. Level	byStTOFCalLvl	0 <= x <= 15	TBD UMD
Features	wStFeatFlags	Flag Register	0
Dig. control	wStPwrCtrl	Flag Register	0
HV pwr cntrl	wStHVPwrCtrl	Flag Register	0
PHA range assignm.	TBD		
Priority definition	TBD		
DPPS commandable seq.	abyDPPSSeq[32]	0 <= x <= 31	0
DPPS seq. select	byDPPSSeqSel	0 <= x <= 3	0

Table 44 : STICS related contents of the non-volatile RAM

Item	Variable	Values	Default
HVPS upper limit	abyIHVLim[5]	0 <= x <= 255	0
HVPS voltage set	abyIHVSet[5]	0 <= x <= 255	0
Energy threshold	abyIEThr[4]	0 <= x <= 63	5
Valid Event Logging	byIValEvLog	0 <= x <= 7	7
E-Calibration Level	byIECalLvl	0 <= x <= 255	TBD APL
TOF Clbr. Level	byITOFCalLvl	10 <= x <= 14	TBD APL
Dig. Control	wIFeatFlags	Flag Register	0
Power cntrl	wIPwrCtrl	Flag Register	0
HV pwr cntrl	wStHVPwrCtrl	Flag Register	0
PHA priority freeze	bIPHAPriorFreeze	On/Off Flag	0
PHA control	wIPHAControl	Flag Register	s.b.

Table 45 : ICS related contents of the non-volatile RAM

Item	Variable	Values	Default
Dig. Control	wDFeat		
Power Control	wDPwrCtrl		
Code connection jumps			

Table 46 : DPU related contents of the non-volatile RAM

## **12. Housekeeping**

The status channels for Telemetry A and Telemetry B transmit 3 byte status which are repeated every 32 S/C frame and which represent the power switching status of the DPU and of the analog electronics of both sensors. Another byte contains a subcom index and two bytes contain science-record-subcommutated data, each byte represents one subcom channel. During one science record, 192 bytes may be transmitted through each subcom channel on telemetry A and 48 channels can be transmitted through each subcom channel on telemetry B. The first channel (BYTE 4) is a copy of the HK data contained in the EDBs. The other channel is not implemented yet. During normal operation, the HK status data contained in the EDBs and the status data transmitted over the first subcom channel in the status bytes, are synchronous. This may change, if the S/C spin is not exactly 20 rpm.

**13. ICS Rate Address Generation Definition**

<u>Prc</u>	<u>Nam</u>	<u>#r</u>	<u>#h</u>	<u>#sec</u>	<u>#spins</u>	<u>#b</u>	<u>addressing</u>																		
0	A	2	1	16	2	2	r rate	<table border="1"> <tr> <td>sp1</td> <td>sp0</td> <td>sc3</td> <td>sc2</td> <td>sc1</td> <td>sc0</td> <td>b1</td> <td>b0</td> </tr> <tr> <td>buf</td> <td>spi</td> <td colspan="4">sec</td> <td colspan="2">accu</td> </tr> </table>	sp1	sp0	sc3	sc2	sc1	sc0	b1	b0	buf	spi	sec				accu		
sp1	sp0	sc3	sc2	sc1	sc0	b1	b0																		
buf	spi	sec				accu																			
1	B	1	1	8	2	2	r rate	<table border="1"> <tr> <td>sp1</td> <td>sp0</td> <td>sc3</td> <td>sc2</td> <td>sc1</td> <td>b1</td> <td>b0</td> <td></td> </tr> <tr> <td>buf</td> <td>spi</td> <td colspan="4">sec</td> <td colspan="2">accu</td> </tr> </table>	sp1	sp0	sc3	sc2	sc1	b1	b0		buf	spi	sec				accu		
sp1	sp0	sc3	sc2	sc1	b1	b0																			
buf	spi	sec				accu																			
2	C1	14	2	16	1	2	r rate	<table border="1"> <tr> <td>sp1</td> <td>h0</td> <td>sc3</td> <td>sc2</td> <td>sc1</td> <td>sc0</td> <td>b1</td> <td>b0</td> </tr> <tr> <td>buf</td> <td>hd</td> <td colspan="4">sec</td> <td colspan="2">accu</td> </tr> </table>	sp1	h0	sc3	sc2	sc1	sc0	b1	b0	buf	hd	sec				accu		
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buf	hd	sec				accu																			
3	C2	14	2	8	2	2	r rate	<table border="1"> <tr> <td>sp1</td> <td>sp0</td> <td>h0</td> <td>sc3</td> <td>sc2</td> <td>sc1</td> <td>b1</td> <td>b0</td> </tr> <tr> <td>buf</td> <td>spi</td> <td>hd</td> <td colspan="4">sec</td> <td colspan="2">accu</td> </tr> </table>	sp1	sp0	h0	sc3	sc2	sc1	b1	b0	buf	spi	hd	sec				accu	
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buf	spi	hd	sec				accu																		
4	C3	14	1	16	2	2	r rate	<table border="1"> <tr> <td>sp1</td> <td>sp0</td> <td>sc3</td> <td>sc2</td> <td>sc1</td> <td>sc0</td> <td>b1</td> <td>b0</td> </tr> <tr> <td>buf</td> <td>spi</td> <td colspan="4">sec</td> <td colspan="2">accu</td> </tr> </table>	sp1	sp0	sc3	sc2	sc1	sc0	b1	b0	buf	spi	sec				accu		
sp1	sp0	sc3	sc2	sc1	sc0	b1	b0																		
buf	spi	sec				accu																			
5	D1	80	2	16	1	2	r rate	<table border="1"> <tr> <td>sp4</td> <td>h0</td> <td>sc3</td> <td>sc2</td> <td>sc1</td> <td>sc0</td> <td>b1</td> <td>b0</td> </tr> <tr> <td>buf</td> <td>hd</td> <td colspan="4">sec</td> <td colspan="2">accu</td> </tr> </table>	sp4	h0	sc3	sc2	sc1	sc0	b1	b0	buf	hd	sec				accu		
sp4	h0	sc3	sc2	sc1	sc0	b1	b0																		
buf	hd	sec				accu																			
6	D2	80	2	8	2	2	r rate	<table border="1"> <tr> <td>sp4</td> <td>sp3</td> <td>h0</td> <td>sc3</td> <td>sc2</td> <td>sc1</td> <td>b1</td> <td>b0</td> </tr> <tr> <td>buf</td> <td>spi</td> <td>hd</td> <td colspan="4">sec</td> <td colspan="2">accu</td> </tr> </table>	sp4	sp3	h0	sc3	sc2	sc1	b1	b0	buf	spi	hd	sec				accu	
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buf	spi	hd	sec				accu																		
7	D3	80	1	16	2	2	r rate	<table border="1"> <tr> <td>sp4</td> <td>sp3</td> <td>sc3</td> <td>sc2</td> <td>sc1</td> <td>sc0</td> <td>b1</td> <td>b0</td> </tr> <tr> <td>buf</td> <td>spi</td> <td colspan="4">sec</td> <td colspan="2">accu</td> </tr> </table>	sp4	sp3	sc3	sc2	sc1	sc0	b1	b0	buf	spi	sec				accu		
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8	D4	80	1	8	4	2	r rate	<table border="1"> <tr> <td>sp4</td> <td>sp3</td> <td>sp2</td> <td>sc3</td> <td>sc2</td> <td>sc1</td> <td>b1</td> <td>b0</td> </tr> <tr> <td>buf</td> <td colspan="2">spi</td> <td colspan="4">sec</td> <td colspan="2">accu</td> </tr> </table>	sp4	sp3	sp2	sc3	sc2	sc1	b1	b0	buf	spi		sec				accu	
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buf	spi		sec				accu																		
9	F1	50	2	16	1	2	r rate	<table border="1"> <tr> <td>sp5</td> <td>h0</td> <td>sc3</td> <td>sc2</td> <td>sc1</td> <td>sc0</td> <td>b1</td> <td>b0</td> </tr> <tr> <td>buf</td> <td>hd</td> <td colspan="4">sec</td> <td colspan="2">accu</td> </tr> </table>	sp5	h0	sc3	sc2	sc1	sc0	b1	b0	buf	hd	sec				accu		
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buf	hd	sec				accu																			
10	F2	50	2	8	2	2	r rate	<table border="1"> <tr> <td>sp5</td> <td>sp4</td> <td>h0</td> <td>sc3</td> <td>sc2</td> <td>sc1</td> <td>b1</td> <td>b0</td> </tr> <tr> <td>buf</td> <td>spi</td> <td>hd</td> <td colspan="4">sec</td> <td colspan="2">accu</td> </tr> </table>	sp5	sp4	h0	sc3	sc2	sc1	b1	b0	buf	spi	hd	sec				accu	
sp5	sp4	h0	sc3	sc2	sc1	b1	b0																		
buf	spi	hd	sec				accu																		
11	F3	50	1	16	2	2	r rate	<table border="1"> <tr> <td>sp5</td> <td>sp4</td> <td>sc3</td> <td>sc2</td> <td>sc1</td> <td>sc0</td> <td>b1</td> <td>b0</td> </tr> <tr> <td>buf</td> <td>spi</td> <td colspan="4">sec</td> <td colspan="2">accu</td> </tr> </table>	sp5	sp4	sc3	sc2	sc1	sc0	b1	b0	buf	spi	sec				accu		
sp5	sp4	sc3	sc2	sc1	sc0	b1	b0																		
buf	spi	sec				accu																			
12	F4	50	1	8	4	2	r rate	<table border="1"> <tr> <td>sp5</td> <td>sp4</td> <td>sp3</td> <td>sc3</td> <td>sc2</td> <td>sc1</td> <td>b1</td> <td>b0</td> </tr> <tr> <td>buf</td> <td colspan="2">spi</td> <td colspan="4">sec</td> <td colspan="2">accu</td> </tr> </table>	sp5	sp4	sp3	sc3	sc2	sc1	b1	b0	buf	spi		sec				accu	
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buf	spi		sec				accu																		
13	FA1	12	2	8	1	2	r rate	<table border="1"> <tr> <td>sp5</td> <td>h0</td> <td>sc3</td> <td>sc2</td> <td>sc1</td> <td>b1</td> <td>b0</td> <td></td> </tr> <tr> <td>buf</td> <td>hd</td> <td colspan="4">sec</td> <td colspan="2">accu</td> </tr> </table>	sp5	h0	sc3	sc2	sc1	b1	b0		buf	hd	sec				accu		
sp5	h0	sc3	sc2	sc1	b1	b0																			
buf	hd	sec				accu																			

#### **14. Known Problems**

13.Mar.91            The ICS motor movement will be interrupted during the first sectors of a spin, where the EDB is formatted.

6.June.91            Due to a bug in the job manager, it might happen that if a job deletes itself or other jobs which precede this job in the job table, the job next to the current job is not executed in that cycle where the deletion occurs.  
This can happen for example while stepping a couple of HV in parallel. If one HV reached its maximum and deletes the stepping job, another HV might not be stepped up in that spin.

Since the ROM in segment E0000h was not built into the DPU, the DPU will report up to 5 ROM errors in each spin, since the software accesses this ROM up to 5 times per spin (guess why...)



## 15. Revision notes

- 4.2.91 First document release
- 28.2.91 Command execution synchronization notes added  
 Changed HV PS names for ICS due to miswiring in ICS A/E flight model  
**(I\_HVCMD, I\_HV\_LIM, I\_HV\_LEV)**  
 Two tables updated due to new formatting scheme of ED2 (D instead of DA) and new addressing scheme of FA rates (sum over 4 sectors instead of 2)
- 13.3.91 Commands D\_RANGE, D\_HSKPG, D\_PLDBAD, S\_DF\_SEQ, S\_RANGE, I\_PHACMD marked with warnings since they were replaced by parameter load commands.
- 5.4.91 Some editorial changes.  
 Classification equations for STICS updated.  
 Limits for mass & mass-per-charge classes updated  
 Energy slope default value updated.  
 Energy compression formula updated.  
 Correlation between STICS bins and HR/MR/SMR described.  
 STICS Deflection Voltage stepping sequence 2 updated.  
 Switches in D\_WATCHDOG command corrected.  
 D\_DIGCMD option 42 (load STICS box definition) documented.  
 D\_JOB command code corrected.  
 S\_HVCMD DPPS switches corrected (options 7,8)  
 S\_PWRCMD options 8 and 11 updated (Main bias power is not inverted)  
 Byte numbers for parameter updated.  
 Structure of parameter 30 (STICS box definition) updated.
- 6.6.91 Editorial changes  
 Classification explained in more detail  
 ICS PHA processing documented
- 12 August 93 Focus changed from “DPU User’s Guide” to “EPIC Instrument User’s Manual”.  
 Instrument Description added.  
 All sections updated.  
 Housekeeping and Command indexes added.  
 Editorial changes.  
 Index added.

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