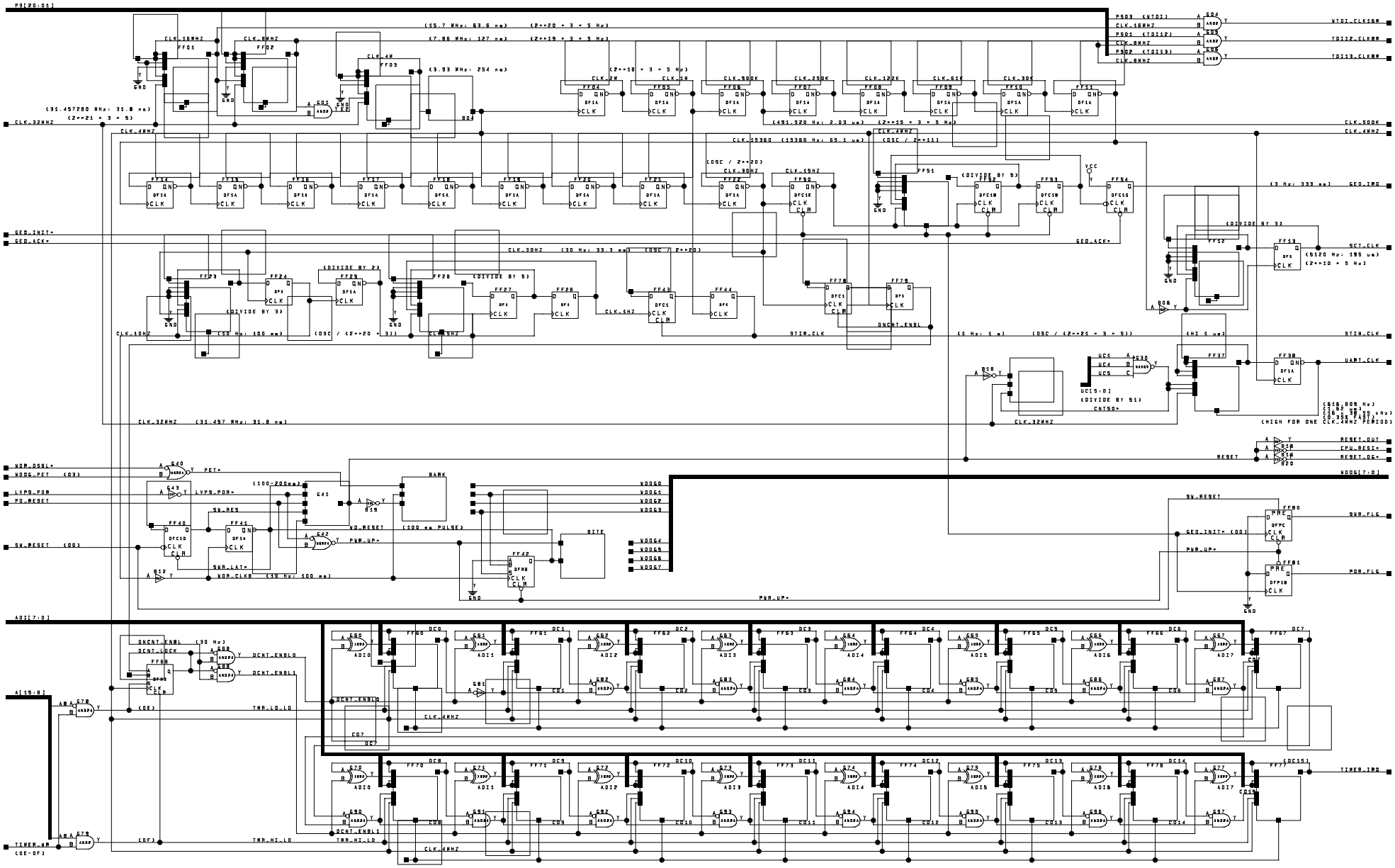
PS[20:04]
CLK_16MHZ
CLK_8MHZ
CLK_4M
CLK_32KHZ
CLK_4MHZ
CLK_500K
CLK_250K
CLK_122K
CLK_61K
CLK_30K
CLK_2M
CLK_1M
CLK_19380
CLK_30HZ
CLK_15HZ
CLK_10HZ
CLK_5HZ
CLK_1HZ
CLK_32MHZ
GEO_INIT*
GEO_ACK*
GEO_IRQ
SCT_CLK
STIM_CLK
UART_CLK
RESET
RESET_OUT
CPU_RESET*
RESET_DG*
VDDS[7:0]
WDR_DSBL*
WDDS_PET
LVPS_POR*
PO_RESET
SW_RESET
PET*
SW_RES
SWR_LAT*
WDR_CLKB
PWR_UP*
BANK
BITE
SWR_FLG
POR_FLG
ADI[7:0]
A[15:8]
DCNT_ENBL
DCNT_LOCK
DCNT_ENBL0
DCNT_ENBL1
TMR_LD_LO
TMR_HI_LD
TIMER_WR
TIMER_IRQ
CPU_CLKD
C.A.Ingraham 1997-04-25
C.A.Ingraham 1998-11-11
C.A.Ingraham
APPROX. SEQ/COMB MODULE COUNT: 75/63
Schematic.
DPUGLU Actel TIMING Block
\IMAGE...\DPUGLU\TIMING
1 of 1
A