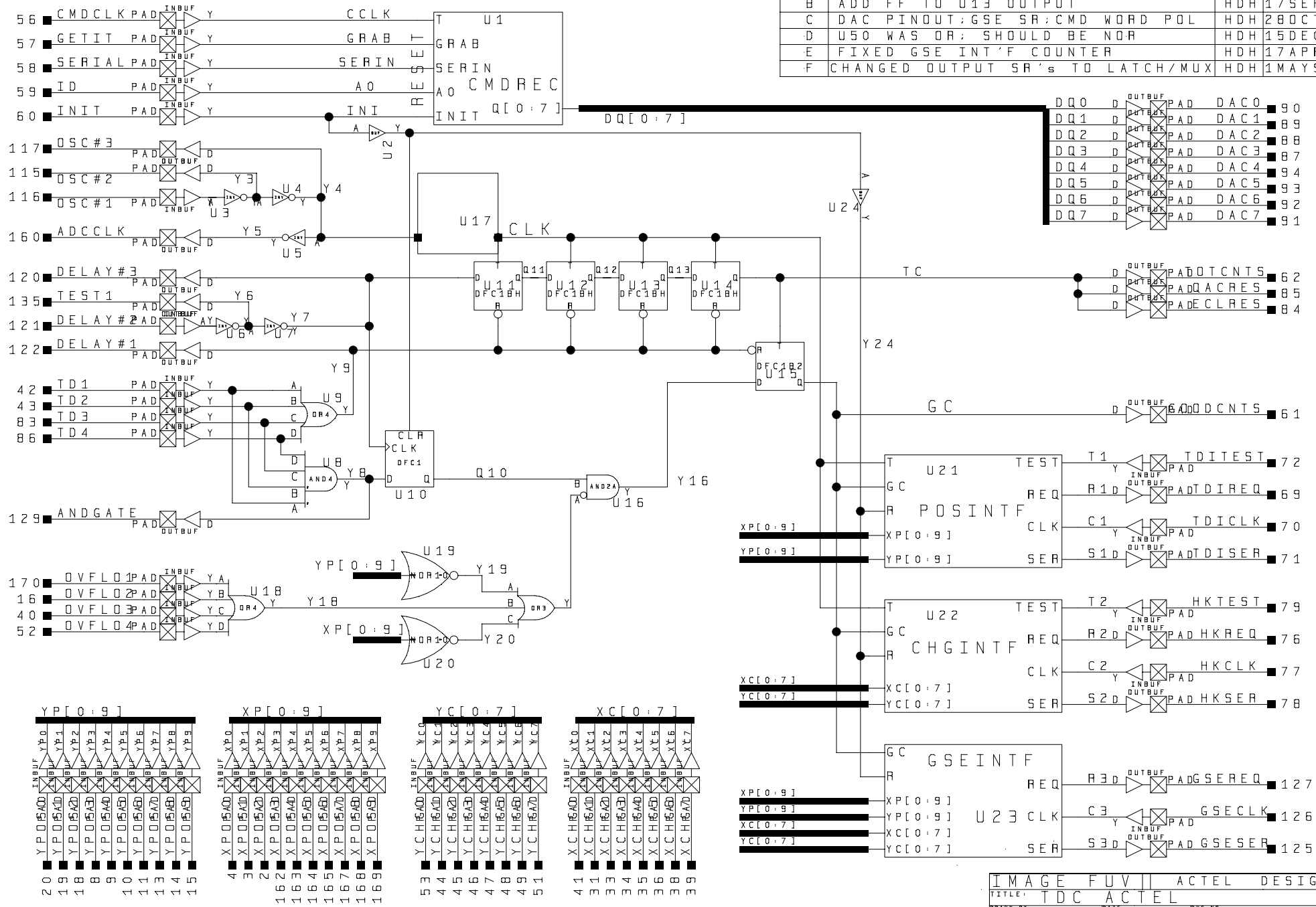


REV	DESCRIPTION	BY	DATE
B	ADD FF TO U13 OUTPUT	HDH	17SEP97
C	DAC PINOUT; GSE SR; CMD WORD POL	HDH	28OCT97
D	U50 WAS OR; SHOULD BE NOR	HDH	15DEC97
E	FIXED GSE INT'F COUNTER	HDH	17APR98
F	CHANGED OUTPUT SR'S TO LATCH/MUX	HDH	1MAY98



DQ	D	OUTBUF	PAD	DAC	Pin
DQ0	D	OUTBUF	PAD	DAC0	90
DQ1	D	OUTBUF	PAD	DAC1	89
DQ2	D	OUTBUF	PAD	DAC2	88
DQ3	D	OUTBUF	PAD	DAC3	87
DQ4	D	OUTBUF	PAD	DAC4	94
DQ5	D	OUTBUF	PAD	DAC5	93
DQ6	D	OUTBUF	PAD	DAC6	92
DQ7	D	OUTBUF	PAD	DAC7	91

D	OUTBUF	PAD	Pin
TC	OUTBUF	PAD	62
QACRES	OUTBUF	PAD	85
QDECLRES	OUTBUF	PAD	84

D	OUTBUF	PAD	Pin
GC	OUTBUF	PAD	61

TEST	Y	INBUF	PAD	Pin
T1	Y	INBUF	PAD	72
R1D	Y	INBUF	PAD	69
C1	Y	INBUF	PAD	70
S1D	Y	INBUF	PAD	71

TEST	Y	INBUF	PAD	Pin
T2	Y	INBUF	PAD	79
R2D	Y	INBUF	PAD	76
C2	Y	INBUF	PAD	77
S2D	Y	INBUF	PAD	78

REQ	OUTBUF	PAD	Pin	
R3D	OUTBUF	PAD	127	
C3	Y	INBUF	PAD	126
S3D	Y	INBUF	PAD	125

YP	YP	XP	XP	YC	YC	XC	XC
YP0	YP0	XP0	XP0	YC0	YC0	XC0	XC0
YP1	YP1	XP1	XP1	YC1	YC1	XC1	XC1
YP2	YP2	XP2	XP2	YC2	YC2	XC2	XC2
YP3	YP3	XP3	XP3	YC3	YC3	XC3	XC3
YP4	YP4	XP4	XP4	YC4	YC4	XC4	XC4
YP5	YP5	XP5	XP5	YC5	YC5	XC5	XC5
YP6	YP6	XP6	XP6	YC6	YC6	XC6	XC6
YP7	YP7	XP7	XP7	YC7	YC7	XC7	XC7
YP8	YP8	XP8	XP8	YC8	YC8	XC8	XC8
YP9	YP9	XP9	XP9	YC9	YC9	XC9	XC9