



PHASE	PHASE	FUNCTION
S0 RD	S2 RD	LOCK BUFFER & READ LOW (Y) BYTE
S1 RD	S3 RD	READ HIGH (X) BYTE, UNLOCK BUFFER, & CLEAN TEST MODE
S0 WR	S2 WR	SET TEST MODE

(CPU/PLU REVISION)
 C02-SAN - A-23
 C. A. Ingraham 1997-05-30
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 Schematic, DPUGLU Act3 SYNC Block
 APPROX. MODULE COUNT: 502/588
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