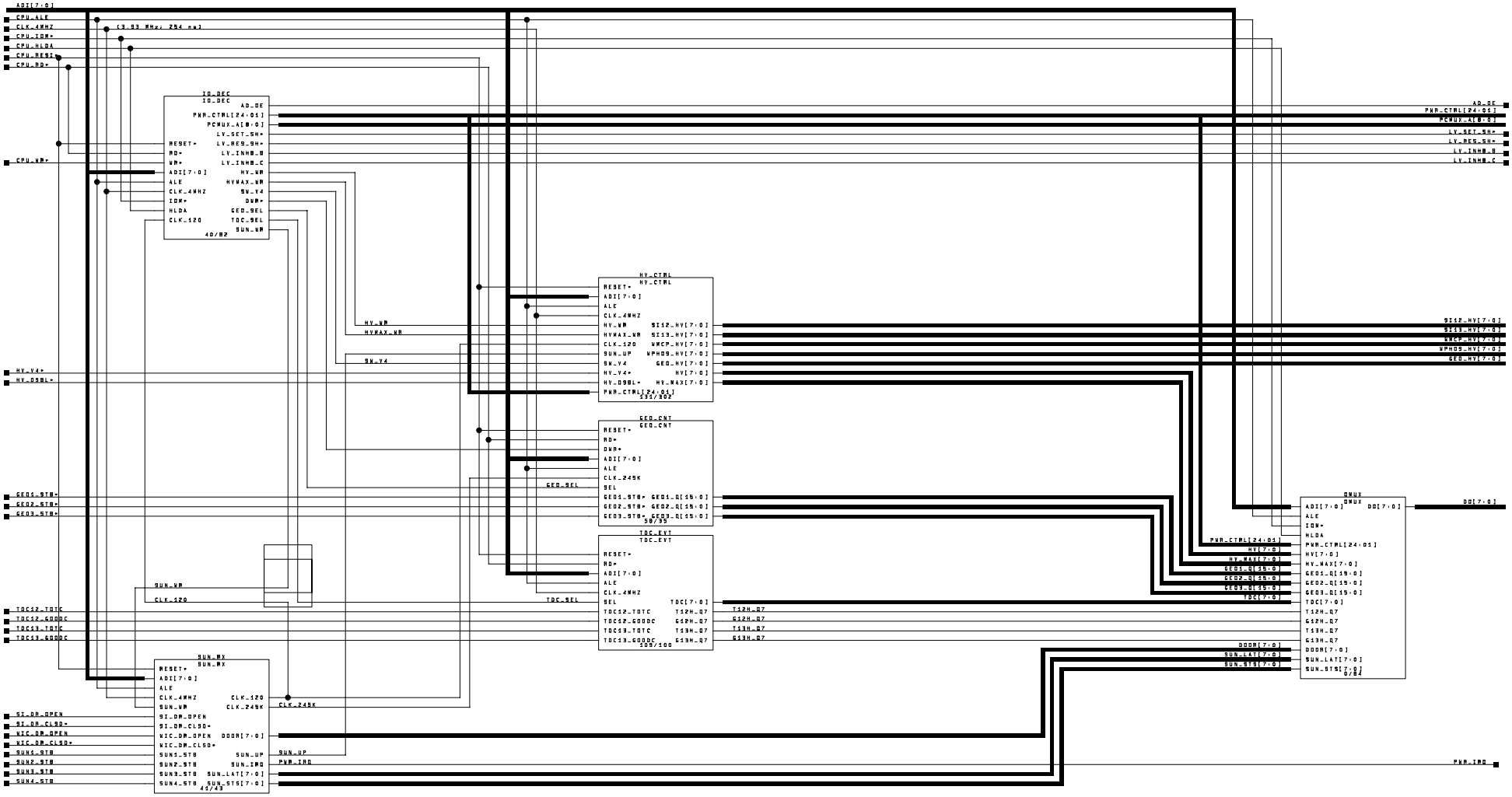
ADI[7:0]
CPU_ALE
CLK_4MHZ
(3.93 MHz; 254 ns)
CPU_IOM*
CPU_HLDA
CPU_RESI
CPU_RD*
CPU_WR*
IO_DEC
IO_DEC
AD_OE
PWR_CTRL[24:01]
PCMUX_A[8:0]
LV_SET_SH*
LV_RES_SH*
LV_INHB_B
LV_INHB_C
HY_WR
HYMAX_WR
SW_V4
DWR*
GEO_SEL
TOC_SEL
SUN_WR
RESET*
RD*
WR*
ALE
CLK_120
HLDA
40/82
HY_CTRL
HY_CTRL
HY_V4*
HY_DSBL*
SI12_HY[7:0]
SI13_HY[7:0]
WMCP_HY[7:0]
WPHOS_HY[7:0]
GEO_HY[7:0]
HY[7:0]
HY_MAX[7:0]
111/302
GEO_CNT
GEO_CNT
GEO1_STB*
GEO2_STB*
GEO3_STB*
GEO1_Q[15:0]
GEO2_Q[15:0]
GEO3_Q[15:0]
CLK_245K
SEL
50/35
TOC_EVT
TOC_EVT
TOC12_TOTC
TOC12_GOOOC
TOC13_TOTC
TOC13_GOOOC
TOC[7:0]
T12H_Q7
G12H_Q7
T13H_Q7
G13H_Q7
109/100
SUN_RX
SUN_RX
SI_DR_OPEN
SI_DR_CLSD*
WIC_DR_OPEN
WIC_DR_CLSD*
SUN1_STB
SUN2_STB
SUN3_STB
SUN4_STB
CLK_245K
DOOR[7:0]
SUN_UP
PWR_IRQ
SUN_LAT[7:0]
SUN_STS[7:0]
45/43
DMUX
DMUX
DD[7:0]
6/84
C.A.Ingraham 1998-01-17
C.A.Ingraham 1999-01-04
C.A.Ingraham
Schematic,
DPUPWR Actel Internal Logic
APPROX. SEQ/COMB MODULE COUNT: 379/642
IMAGE\...\DPUPWR\DPUPWRG
1 of 1
H