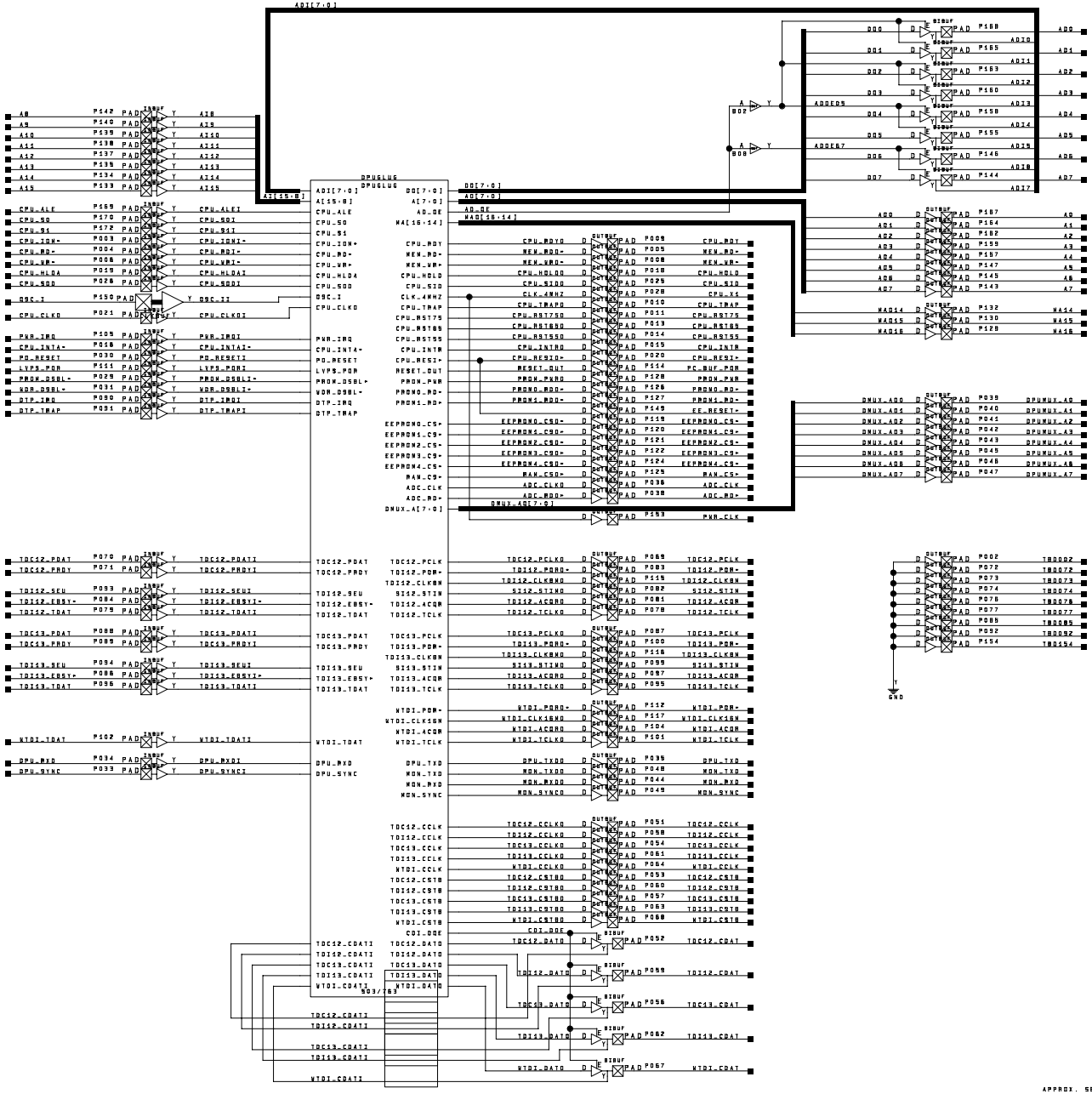

A	1997-10-15	First Release.
B	1997-10-20	Eliminate initial power-up glitch on FDT, FAX Reset FFs in TDM_RX; fix CPU_TDM was CPU_TDM; TDM_TX outputs use O.C.; add PWR_CLK output for DPUPWR; use GDR2 on ~CLK32M.
C	1997-11-20	Add proper control setting to outputs; make stim pulse 1 us wide; add ADC 1/2Hzout sel; fix ADC1 clock; add ADC2 interrupt; add ADC2 Reset; add ADC2 enable; add interrupt mask; Interrupt Requests performed; add IRQ0 to TDM_RX at port D3
D	1998-01-07	Fix UART_CLK rate at 38.4 kb/s (was 55.8 kb/s); add downcount timer; add reset status FFs; remove A[15:14] status bits.
E	1998-01-28	Fix TIMER_WR I/O speeds; fix DCN1_LOCK; fix S1 STIM power-saving; fix BSRF 2.3 errata; fix CDI; add enable power-up; fix CDI readback test; delete SEC_RESET port; fix SEC_CLK from; add SCT Start; add STAC pulse decode; fix SEC INIT timing; revise PRR17 status bits; simplify address latches.
F	1998-02-22	Simplify WR/DWR*; add DPUGLU rev port; major PMA revs; add SC_REV port; fix sum & hash latches; fix CDI state decode.
G	1998-03-09	Upgrade REV ports; fix SCT_LD_ENBL issue; add MUX on WDG_RDO; add TDI reset control; LVPS_POR was active low; delete CLK8 input (pin 184); add TDI32_SEU; TDI13_SEU; finish TDI_MX block; fix PCLK error in PMA; change TX FCOM_Reset to FF; add compatible SEC start errors; add CLK, CAT, CTB, CLK, PCAT, PRST between TDC12 & TDC13; change MUX48 to MUX48U.
H	1998-05-04	Upgrade REV ports; fix SB; fix TDI_RX bit, byte, word, and step timing; add TxREV FF in TDI_RX.
J	1998-06-21	Upgrade REV port to 0A; fix TDI_RX TCLK FF stop input; add TDI readout SR load.
K	1998-06-24	Fix TDI_MX serial clock output.
L	1998-06-25	Upgrade REV port to 0C; fix TDI acquire pulse decode; fix PMA timing logic errors.
M	1998-07-21	Upgrade REV port to 0D; change WIC clk from 32 to 1.8 MHz.
N	1998-08-25	Upgrade REV port to 0E; fix UART TX DVB bit; add separate loopback; simplify TIMING, UART, TDI_RX, REV_DEC, INT_MUX; add TDI readout buffers; revise compression; delete many buffers; simplify extensively.
P	1998-09-16	Upgrade REV port to 10h; fix SMUX-A9 message in REV_DEC; fix 24-28 compr error; at RX41-D0; fix TDI MS site for shift/compr; fix BC-12 decode for shift/compr.
Q	1998-09-24	Upgrade REV port to 11h; fix TDI RX logic.
R	1998-11-11	Upgrade REV port to 12h; add reset to CDI CLK output FF.

C.A.Ingraham 1997-04-18

C.A.Ingraham 1998-11-11

C.A.Ingraham

Schematic,
MEP DPU DPUGLU Actel

APPROX. SEQ+COMB MODULE COUNT: 503+765=1268

\IMAGE\...\DPUGLU\DPUGLU