These notes include requirements and suggestions for the IMAGE FUV MEP DPU printed circuit board layout, Revision A.

GENERAL

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2. Related design documents:
   a. Schematic, Engineering Model, 8097-V4, Rev. B
   b. BOM -- DPU Flight Model, 8098-T1, Rev. A
   c. PCB Outline, 8100-V4, Rev. D
   d. PCB Placement, 8101-V4, Rev. B
   e. PCB Layout Notes, 8099-T1, Rev. A (this document)
3. Board layers. Four layers is the goal, with signal traces on outer layers and power and ground planes on the internal layers as follows:
   Layer 1: Component side; signal traces
   Layer 2: Ground layer: Digital and Analog ground planes
   Layer 3: Power layer; VCC (+5 volt) plane
   Layer 4: Solder side; signal traces
Additional inner signal layers are acceptable.
4. Pin numbers. U101-34 means pin 34 of U101.
5. N.C. pins. Pins marked "N.C." on the schematic are not to be connected to any other signal or net.

ORIENTATION

10. See outline and placement drawings; each is a view of the component side.
   Top: edge near J2, J5, and J3.
   Bottom: edge near Pin 62 end of J18.
   Left: edge near J7 and J18.
   Right: edge near Pin 8 end of J3.
   Component side: shown in outline and placement drawings.

MECHANICAL

20. The board outline is approximately as shown in the outline drawing. See the mechanical outline drawing for details and dimensions of the board corners, mounting holes, and edge cutouts. No components (except the connectors J2, J3, J5, J7, and J18) or outer layer traces are allowed in the keep-out area along the four edges of the board.

21. The eight mounting holes must be as shown. Pads for the mounting holes are allowed in the keep-out area.

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22. Allow a 0.050-inch safety margin between traces and the 0.100-inch wide keep-out area along the edges of the board.

23. Traces on inner layers may pass through the board edge keep-out area but must clear the edges of the board (and the mounting holes and edge cutouts) by at least 0.050 inch.

PLACEMENT

30. See placement suggestion drawing which shows most but not all components.

31. Connectors J2, J3, J5, J7, J18, and J52 must be located exactly as shown in the outline drawing.

32. The placements shown in the placement drawing for other components are suggestions.

33. PROMs. Place PROMs U201 and U202 near the right edge of the board so that a heat sink can be attached from them to the right side of the enclosure. See the placement drawing. Place the PROM power switching transistors (Q201, Q202) close

to the PROM power pins.

34. Place thermistor R212 in the center of the PROM area (U201, U202). Route PROM_TEMP away from digital signals as much as possible.

35. CPU. Place the CPU (U101) close to J18 at the left edge.

Notice that most of the signals from J18 pass straight across to U101.

36. Analog components. Place the analog multiplexers U209-U213 as close to J5 as possible, with the analog "ends" (pins 8 and 9) toward J5. Keep the analog traces between J5 and the

multiplexers as short as possible. Keep the analog traces separate from the digital traces. The placement shown in the drawing is meant to accomplish this.

Place the OP AMP (U305), voltage reference (U214), ADC (U216) and associated discrete components close together and close to

the multiplexers so that the analog signal traces are short and are separated from digital signal traces. This conflicts with the U303-U305 placement requirement below.

Keep each OP AMP's (U303-U305) output traces away from its input traces, and place resistors close to OP AMP input pins.

The following analog signals are particularly critical:
VREF (U214-2 to U216-3)
VIN (U305-7 to U216-18)
All multiplexer analog inputs

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Place RN303-RN307 and U303-U305 between U301 and J3. Keep these traces short and direct. This conflicts with the

U305/U216 placement requirement above. Place U302, Q301, and C302 close to U301.

37. Place U103 and U104 near J2 and J7.

38. Place U409 near the left end of J5.

39. Decoupling capacitors. Place a power supply decoupling capacitor as close as possible to the power pin of each IC. Each of these capacitors is shown on the schematic. For most ICs, the capacitor has the same reference designator number as its IC. For example, C103 is the capacitor for U103.

For ICs with several power pins, place each capacitor close to its power pin as implied by its position on the schematic.

40. Place C267, C268, C269, C270, and C271 as close as possible to the pins to which they connect on U216.

41. Place ferrite beads L401-L405 as close as possible to the pins they connect to on J52.

ROUTING

50. Ground layer. Most of the ground layer is to be digital ground signal GND.

51. Grounds. Two ground signals are present:
    a. Digital ground (GND, represented by the GND symbol)
    b. Analog ground (AGND, represented by the GNDA symbol)

52. Digital ground. This is the ground for all digital logic.

53. Internal analog ground (AGND). The ground layer area under U209-U214 and U216 and associated components is to be a separate plane connected to AGND. It should be separated from the GND area by a gap of about 0.050 inch. Digital signals should not be routed in this area on any layer. (Some exceptions may be necessary.)

54. Fill unused area of the component and solder sides in this analog section with traces connected to analog ground.

55. AGND to GND connection. Connect AGND to GND with a J_NC jumper J201 on the solder side between U216-19 and U216-6. (See J_NC description below.)

56. Power layer. Most of the power layer is to be covered with VCC (+5 volts).

57. Power pins. Five power buses exist: VCC (+5 volts), MUX+V, MUX-V, +12 volts, and -12 volts.

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VCC is the main power for digital ICs, and it is to occupy most of the power layer.

Some digital ICs (U201, U202) have individually switched power as shown on the schematic.

MUX+V and MUX-V supply power to analog ICs U209-U214. Keep these traces away from digital signals.

58. Analog input signals. Several analog signals must pass from J18 (pins 1, 2, 3, 4, and 6) to the analog area (esp. U213). These traces need to be isolated from the adjacent digital signals. Route these analog traces along the left edge on the power layer. Isolate these traces from the VCC area of the power layer with AGND traces on either side of the analog traces.

This area should be filled on the other three layers with a plane connected to AGND. AGND should be separated from the GND area by a gap of about 0.050 inch. Digital signals should not be routed in this area on any layer. (Some exceptions will be necessary.)

59. Analog signals. Do not route an analog signal parallel and adjacent to a digital signal.

60. Critical signals. Traces for these digital signals should

be as short as possible and be routed away from other signals where possible:

a. OSC (U105-8)
b. CPU_X1 (U102-28)
c. TDI12_CLK32M (U102-115)
d. TDI13_CLK32M (U102-116)
e. WTDI_CLK32M (U102-117)

61. Critical signals. The following are very critical analog signals. Traces for these signals must be as short as possible and be routed away from other signals:

a. VIN (U305-7)
b. VREF (214-2)
c. MUX_OUT (U209-8, etc.)

62. Spare gate inputs. Two sections of U401 and two sections of U409 are spare gates whose inputs are grounded through "J_NC" jumpers rather than being connected directly to the ground plane (see J492 at U409-9).

The J_NC jumper is to allow the easy rewiring of a pin which might otherwise be connected to the power or ground layer by its plated-thru hole.

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J_NC is to consist of two holes with pads, much like a two-pin component footprint, except that the holes and pads can be smaller and closer (say, 0.1 inch) together; the pads are to be joined by a short outer-layer trace.

63. Another special jumper, J_1 (e.g. J450 at J52-004), is a similar arrangement for no-connect pins. J_1 is to be one

small hole and pad with a short outer-layer trace to the no-connect component pin.

COMPONENTS

70. Use component footprints supplied by Chris Shculz.

71. Coordinate new component footprints with Chris Shculz.
72. J3 is a 15-pin connector (Positronic SND15F5000G) with pins 9-15 not installed.

73. J7 is a 15-pin connector (Positronic SND15M5000G) with pins 9-15 not installed.

74. J52 is to be installed with the body and female contacts on the solder side and the male contacts on the component side

as shown by the pin numbers on the outline drawing.

MISCELLANEOUS

80. Component side silkscreen shall include reference designators.

81. Add this text in copper on the component side:

IMAGE FUV MEP DPU, ASSY 8103, REV

82. Add this text in copper on the solder side:

IMAGE FUV MEP DPU, FAB 8102, REV A

83. Use a square pad on the outer layers to mark pin 1 on connectors, ICs, and resistor networks; to mark the positive end of polarized capacitors; to mark the cathode end of diodes; and to mark the emitter lead of transistors.

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