SDL/04-040
Revision: B

SOFIE
(Solar Occultation for Ice Experiment)

Electrical and Software
Interface Control Document

SDL PROPRIETARY

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1. INTRODUCTION

1.1 Revision History

REV	CHANGES	DATE
-	Original release.	4/05/2004
A	Fixes and updates.	9/23/2004
B	Fixes and updates (see DN rev B)	9/30/2005

1.2 Scope

This Interface Control Document (ICD) addresses the interfaces between the Electrical, Electronic, and Electro-mechanical (EEE) components within the SOFIE Instrument. It also serves as the ICD between the SOFIE electronic and software development.

1.3 Purpose

This document is an internal SDL proprietary document. This document is to be used by the SDL SOFIE team in the development and testing of the SOFIE system. This document is to be the repository for the interface information that drives the SOFIE electronic and software development effort. This document defines both the electrical hardware and hardware/software interfaces to and within the SOFIE system.

1.4 Document Overview

Two primary types of drawings are used to define the Electrical, Electronic, and Electro-mechanical (EEE) interface within the SOFIE Instrument. These are Functional Partition Diagrams and Physical Interface Diagrams. The Functional Partitions divides the SOFIE Instrument into sub-components and specify the information going between them. The Physical Interface Diagrams define the physical signals, connectors and cables interconnecting the sub-systems.

Section 2. Overview of SOFIE Instrument, presents a brief overview of the SOFIE Instrument and identifies its major components as well as the sub-systems within these components. .

Section 3. SOFIE to Spacecraft Interface Description, describes the interfaces between the SOFIE system and the spacecraft.

Section 4. SOFIE Components and Subcomponents Description, identifies the components of the SOFIE system and the sub-components within these components.

Section 5. SOFIE Optical to Electrical Interface Description, describes the optical to electrical interface between the optical components and the Focal Plane Array Image Sensor.

Section 6. SOFIE Electronics Unit Major Components Description, identifies and describes the major components within the SOFIE Electronics Unit

Section 7. SOFIE Instrument to Electronics Unit Interface Description, identifies interfaces between the SOFIE Instrument and the Electronics Unit and describes the interface signals going between them. The function of the interface signals are described along with the interface timing and special interface requirements.

Section 8. Instrument Unit Internal Interfaces Description, identifies and describes the interfaces within the Instrument Unit. The function of the interface signals are described along with the interface timing and special interface requirements.

Section 9. Electronics Unit Internal Interfaces Description, identifies and describes the interfaces within the Electronics Unit. The function of the interface signals are described along with the interface timing and special interface requirements.

Section 10. FPGA Interface Description, describes between all of the FPGA's in the system. The function of the interface signals are described along with the interface timing and special interface requirements.

Section 11. SOFIE Hardware / Software Interface Description, describes the interface between the hardware components of the SOFIE system and the computing components within the system. Communication protocols are described along with a description of the registers that can be written by the processors. A programmers model of the elements of the Processor system is also described.

Section Error! Reference source not found. **SOFIE Cabling Description,** describes the cables connecting to the SOFIE Instrument as well as the cables going between the Instrument Unit and the Electronics Unit.

Section 12. SOFIE Ground Support Equipment Interface Control, defines the components within the Ground Support Equipment and the interfaces between these components. The Ground Support Equipments interface to SOFIE is the same as the Spacecraft's interface. The Ground Support Equipment also has additional monitoring interfaces to the Spacecraft Communication Bus.

2. OVERVIEW OF SOFIE INSTRUMENT

The SOFIE Instrument is composed of two major components, The SOFIE Instrument Unit and the SOFIE Electronics Unit. Figure 1 shows 3-dimensional views of the SOFIE Instrument and the SOFIE Electronics Unit.

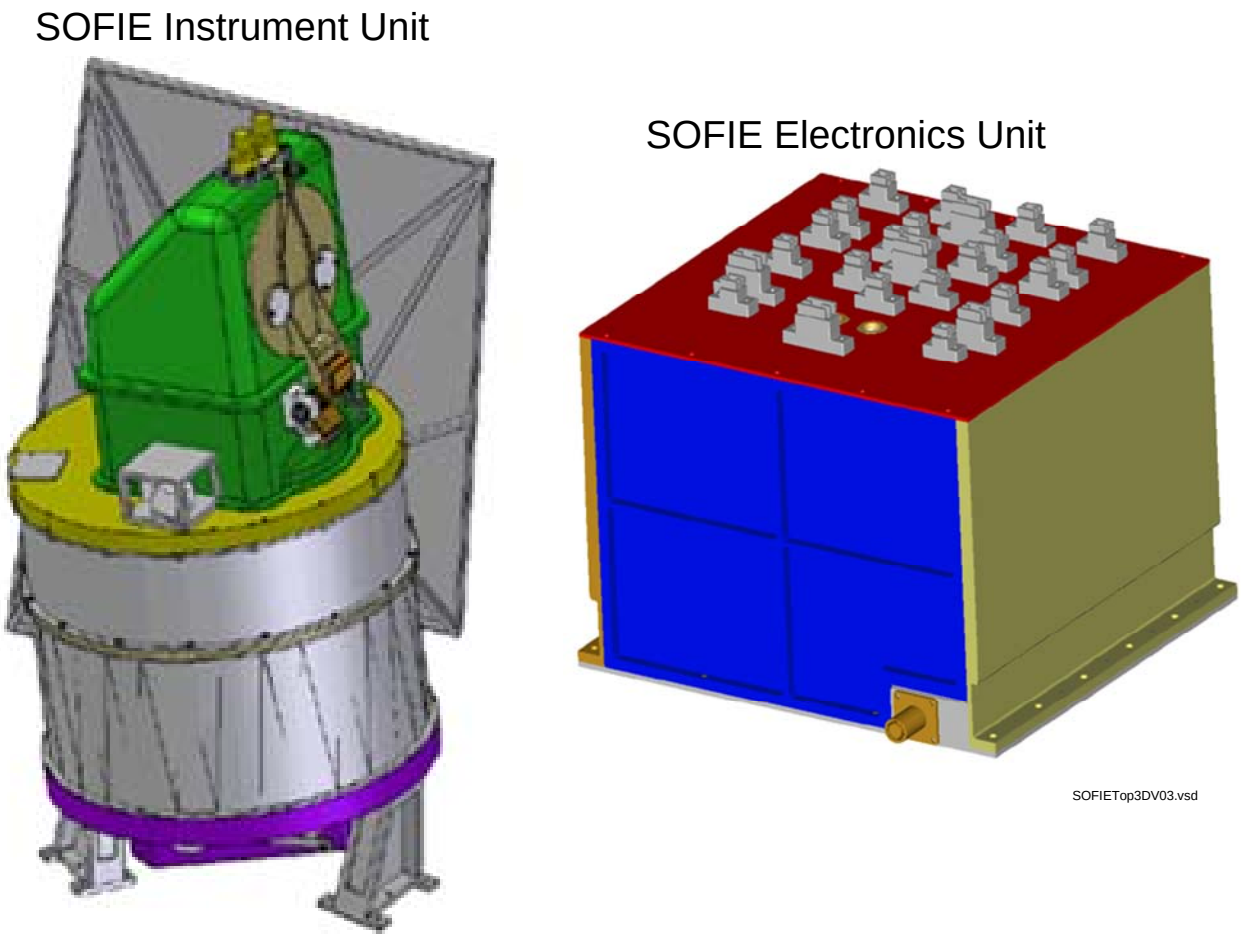


Figure 1 SOFIE Instrument Unit and Electronics Unit

Figure 2 is a top level view of the major components of the SOFIE system and the information flowing between them. The SOFIE Instrument Unit contains the optics, steering mirror, detectors and tracking control functions required to acquire the Sun and make the desired scientific measurements. The SOFIE Electronics Unit contains the electronics for controlling the components in the SOFIE Instrument Unit. It also contains the signal conditioning, data acquisition, and communication components to gather the scientific data and transfer it via the Spacecraft's communication bus.

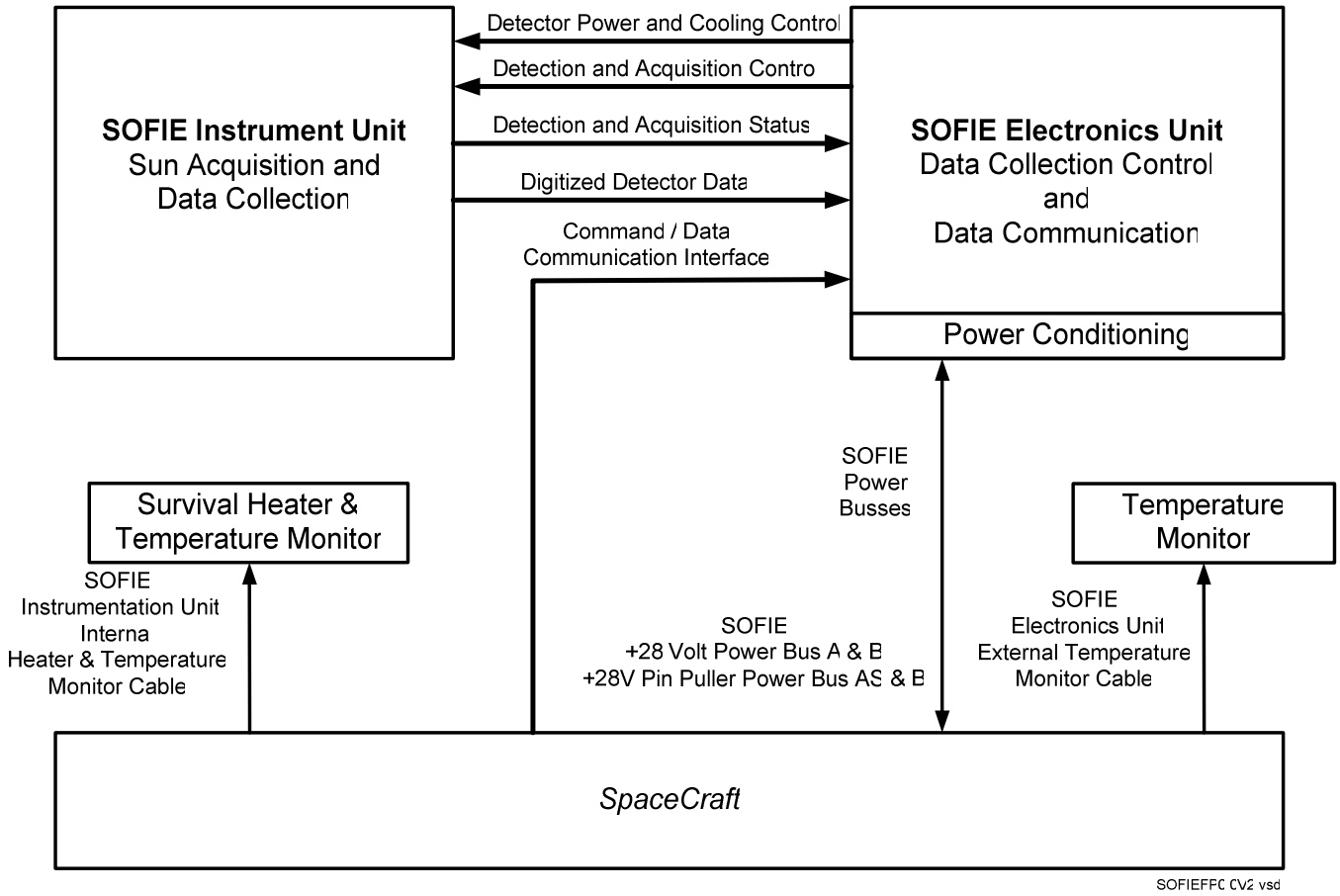


Figure 2 SOFIE System Functional Partition

3. SOFIE SPACECRAFT INTERFACE CONTROL

SOFIE has four interfaces with the Spacecraft:

- Command and Data Communication
- Power Busses
- Electronics Unit Temperature Monitor
- Instrument Unit Survival Heater and Temperature Monitors

The Command and Data Communication interface utilizes a dual redundant 1553 Bus. The Power Busses provide 28 volt DC power to the SOFIE System and 28 volts DC power for the Cover Release Electronics. Each of these busses is a dual redundant bus. The Electronics Unit is monitored by one thermistor and the Instrument Unit is monitored by two. The Instrument Unit is provided with two Survival Heaters.

The electrical interface from SOFIE to the Spacecraft is defined in the AIM Instruments to Spacecraft Bus ICD (AIM-T-0600 Rev. B). An overview of the SOFIE to Spacecraft is shown in Figure 3. Refer to the Spacecraft Interface Control Document for more detailed information on the SOFIE to Spacecraft interfaces.

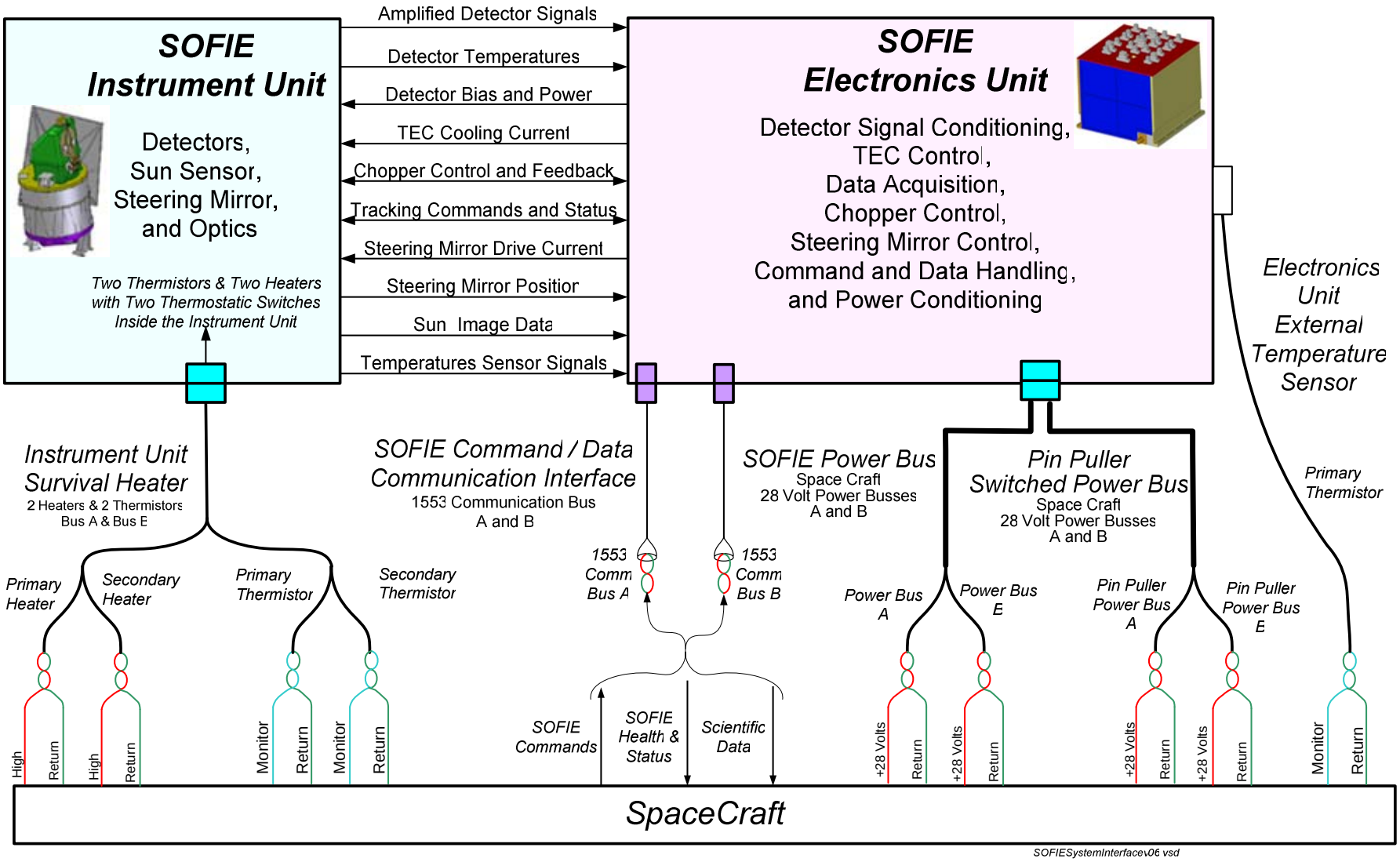


Figure 3 SOFIE Spacecraft Interface

4. SOFIE COMPONENT/SUB-SYSTEM IDENTIFICATION

Figure 4 shows a high level view of the SOFIE System. This section provides a high level description of the components and sub-systems making up the SOFIE system. Figure 5 shows a 3-D model of the SOFIE Instrument Unit identifying its components.

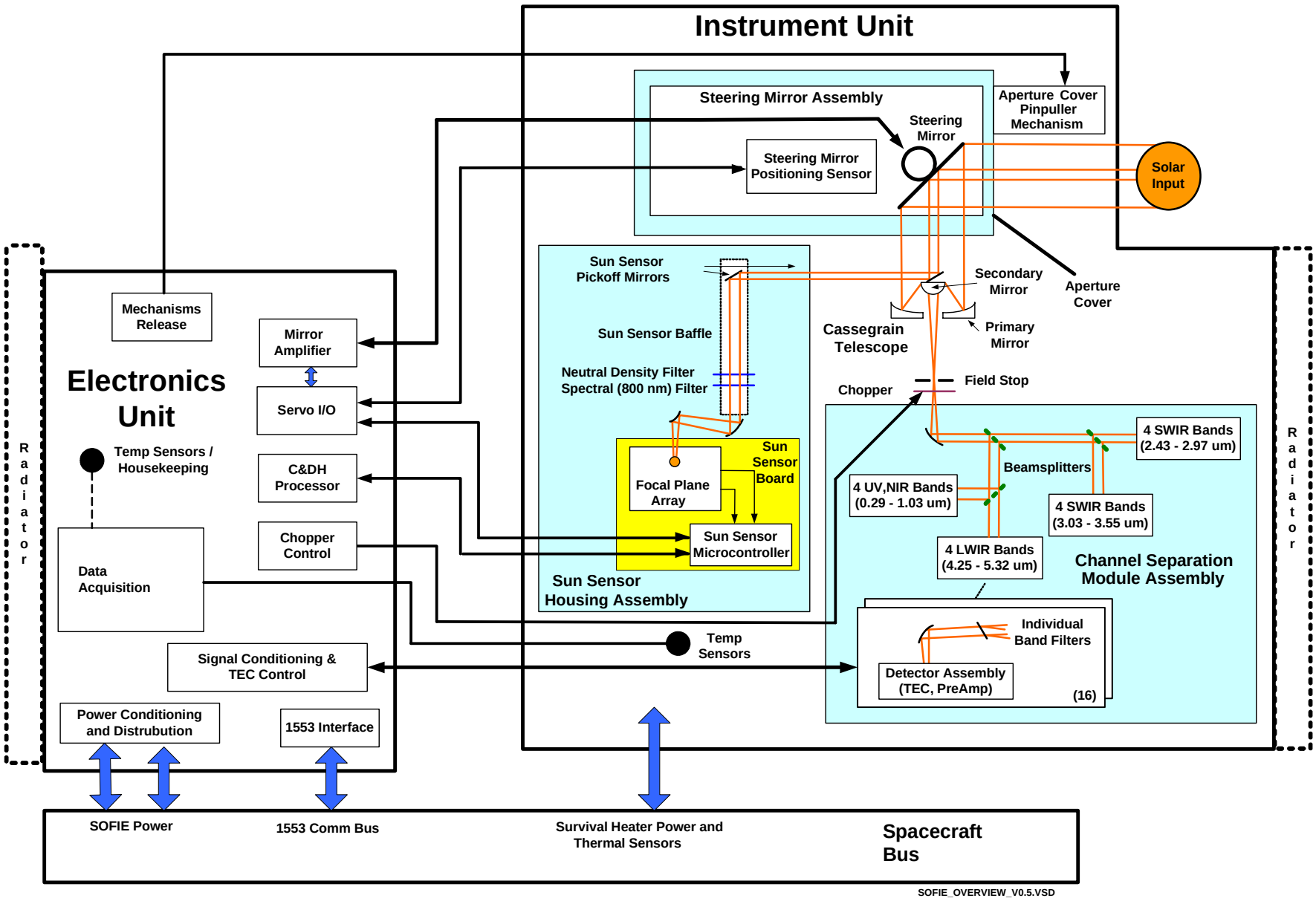

Instrument Unit
Steering Mirror Assembly
Steering Mirror
Steering Mirror Positioning Sensor
Aperture Cover Pinpuller Mechanism
Solar Input
Sun Sensor Pickoff Mirrors
Sun Sensor Baffle
Neutral Density Filter
Spectral (800 nm) Filter
Sun Sensor Board
Focal Plane Array
Sun Sensor Microcontroller
Sun Sensor Housing Assembly
Secondary Mirror
Aperture Cover
Cassegrain Telescope
Primary Mirror
Chopper
Field Stop
4 SWIR Bands (2.43 - 2.97 um)
Beamsplitters
4 UV,NIR Bands (0.29 - 1.03 um)
4 SWIR Bands (3.03 - 3.55 um)
4 LWIR Bands (4.25 - 5.32 um)
Channel Separation Module Assembly
Individual Band Filters
Detector Assembly (TEC, PreAmp)
(16)
Radiator
Mechanisms Release
Electronics Unit
Mirror Amplifier
Servo I/O
C&DH Processor
Chopper Control
Temp Sensors / Housekeeping
Data Acquisition
Signal Conditioning & TEC Control
Power Conditioning and Distrubution
1553 Interface
Temp Sensors
SOFIE Power
1553 Comm Bus
Survival Heater Power and Thermal Sensors
Spacecraft Bus
SOFIE_OVERVIEW_V0.5.VSD

Figure 4 SOFIE Top Level Optical and Electrical Overview

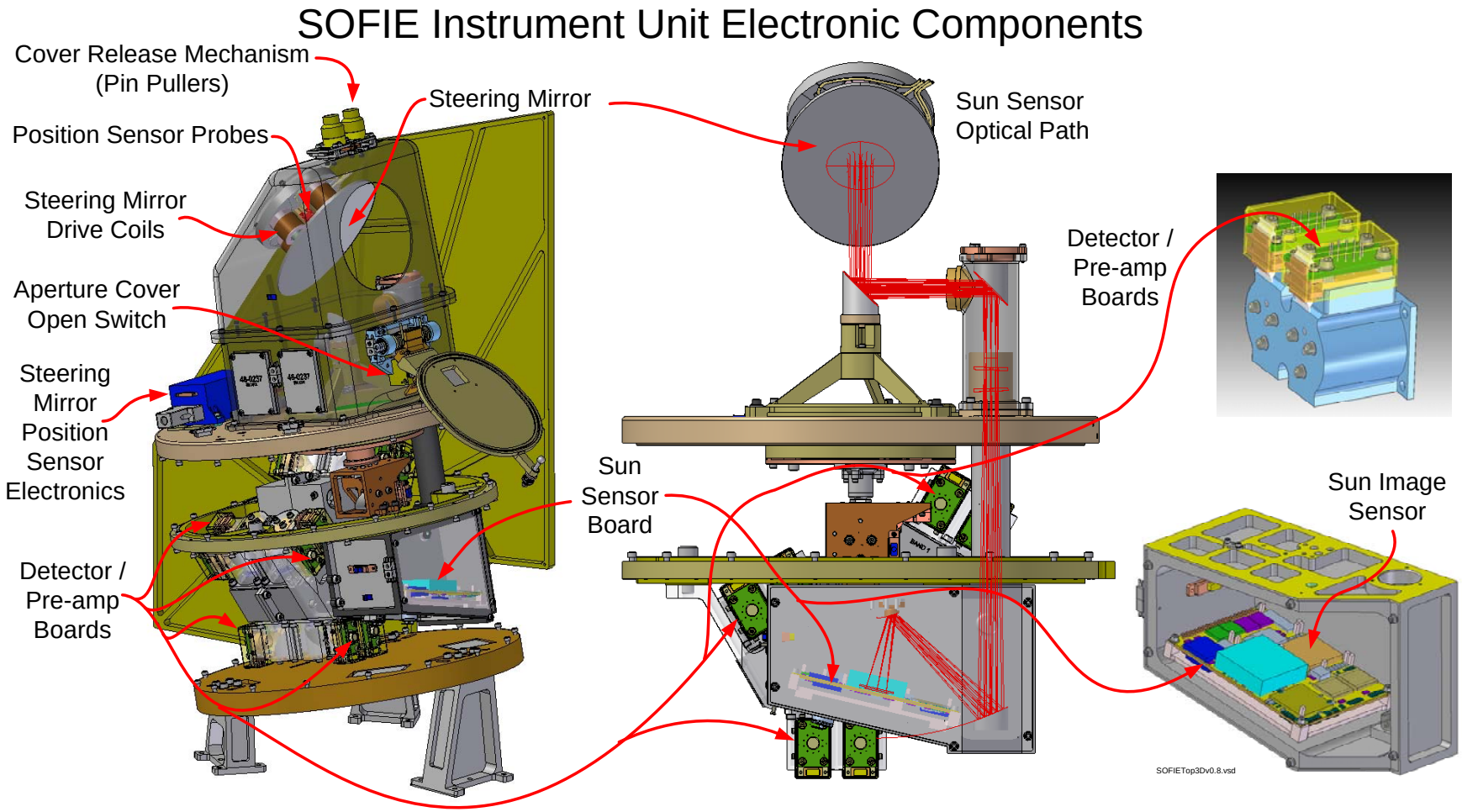


Figure 5 SOFIE Instrument Unit Components

4.1 Instrument Unit Major Components

The SOFIE Instrument Unit contains the following components/sub-systems:

- Steering Mirror Assembly
- Detector/Pre-Amp Board
- Sun Sensor Board
- Instrument Unit Temperature Sensors
- Instrument Unit Aperture Release Mechanism

The Steering Mirror Assembly is being developed by SSG. This assembly is described in SDL/03-413 SOFIE SSG ICD. The Detector/Pre-Amp Board, Sun Sensor Board, and the Instrument Unit Aperture Release Mechanism are described in the following sections. The location of the Instrument Unit Temperature Sensors is given in Appendix B.

4.1.1 Sun Sensor Board

The Printed Circuit Board definition for the Sun Sensor Board is shown in Figure 6.

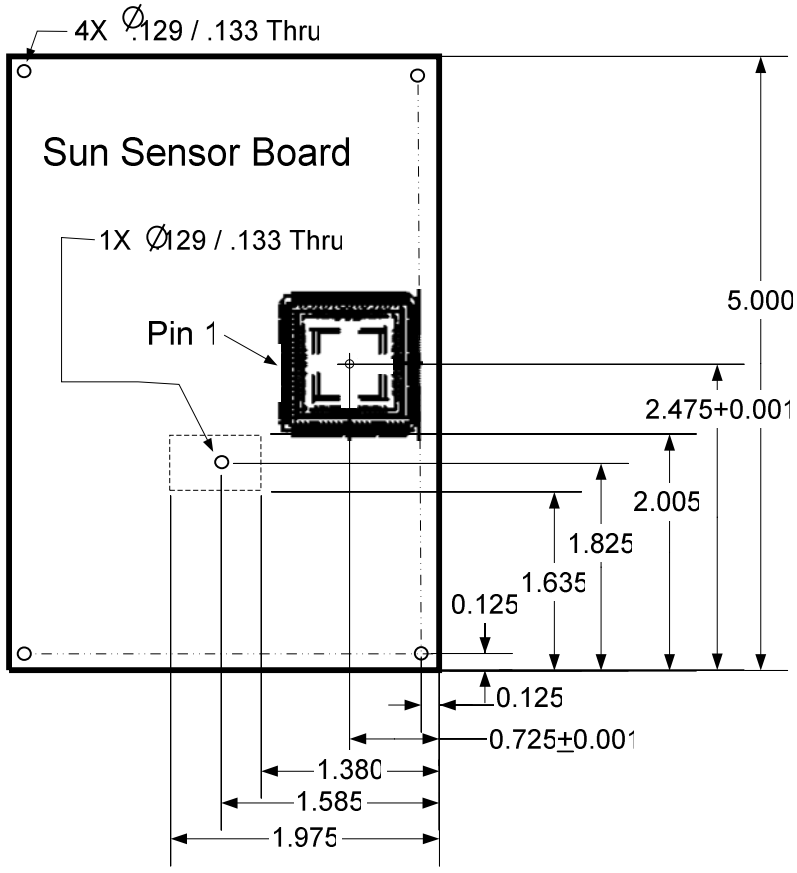


Figure 6 Sun Sensor PCB Definition

4.1.2 Detector/Pre-Amp Board

Figure 7 Depiction of Detector/Pre-amp Component is a depiction of the Detector/Pre-amp Component. The Printed Circuit Board definition for the Detector/Preamp Board is shown in Figure 8 Detector/Pre-amp PCB Definition.

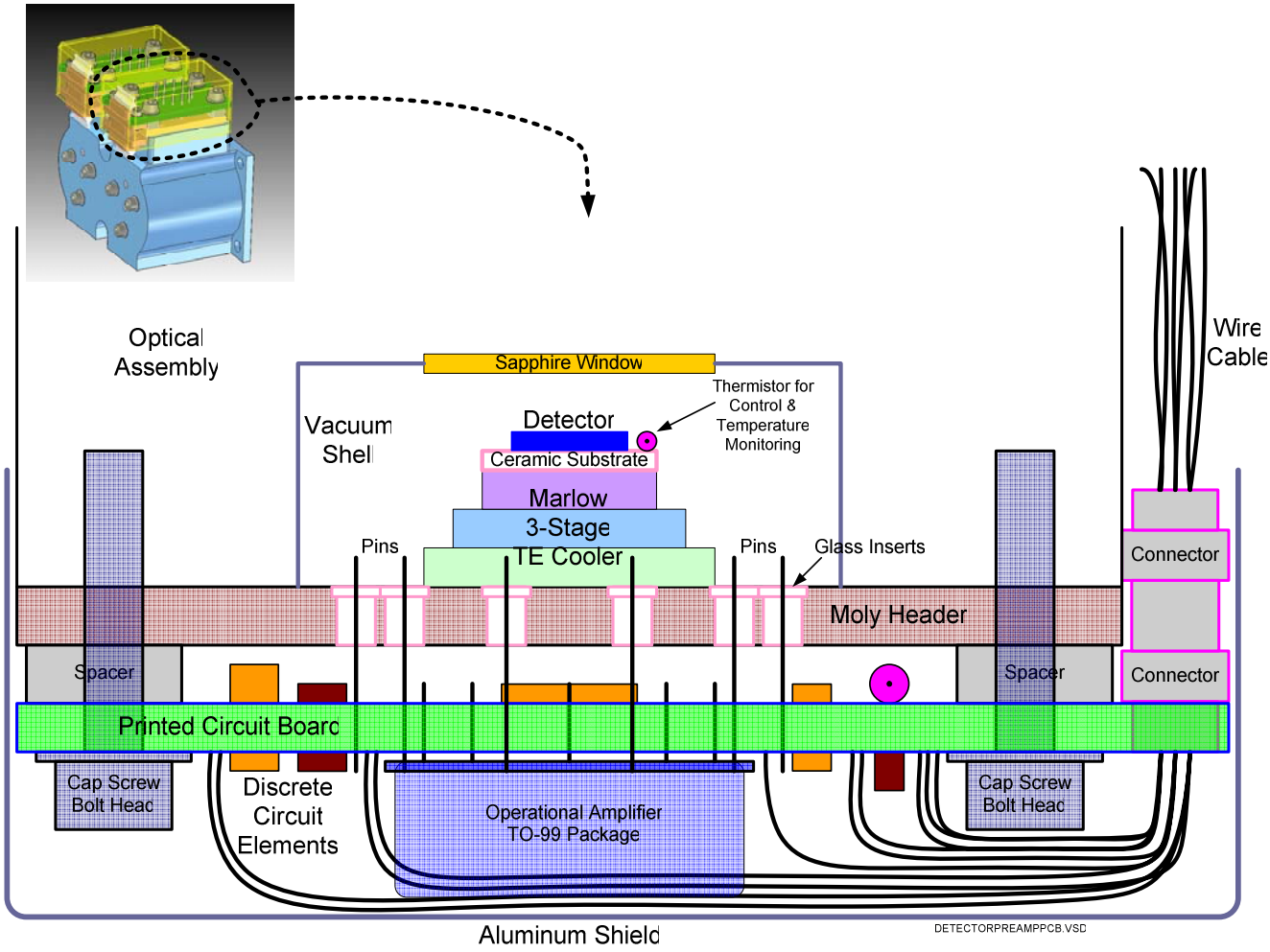


Figure 7 Depiction of Detector/Pre-amp Component

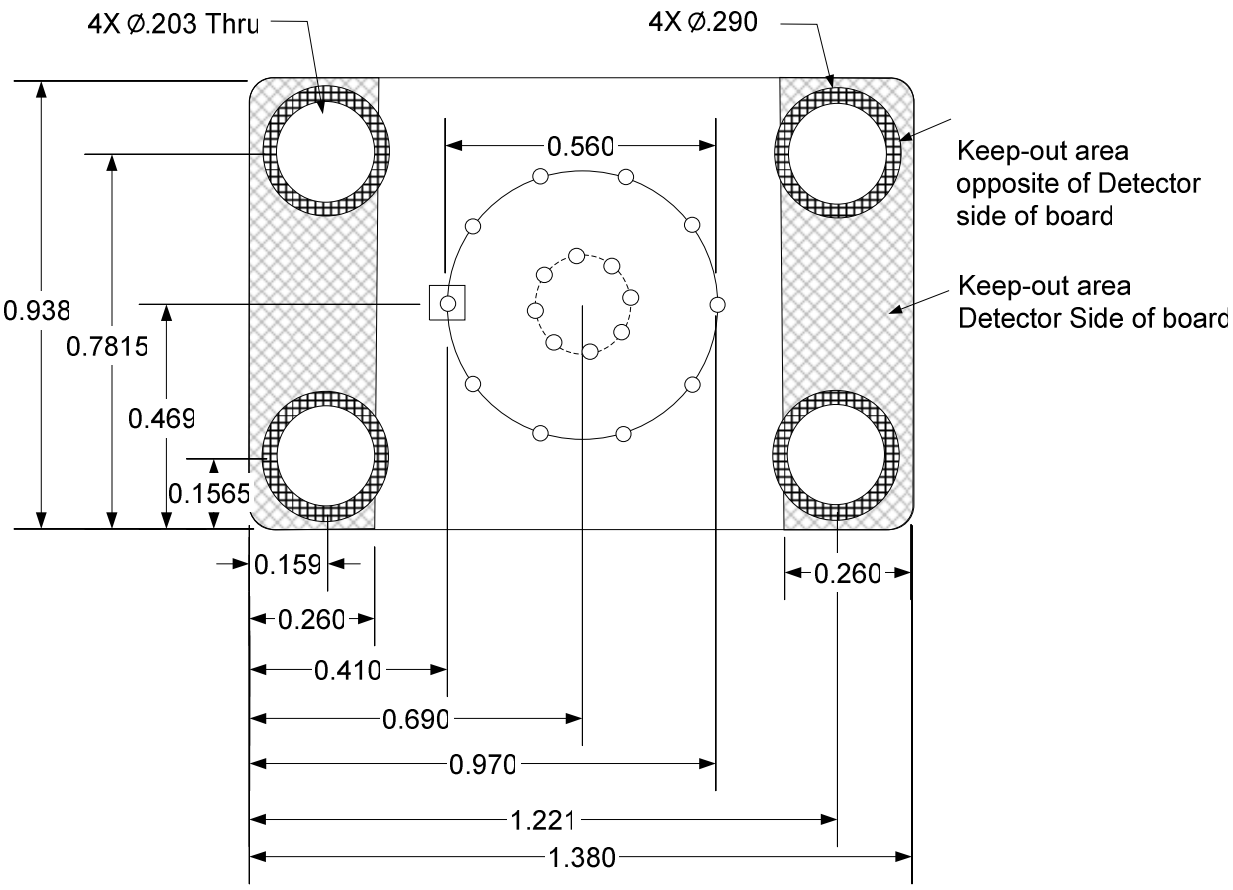


Figure 8 Detector/Pre-amp PCB Definition

5. SUN SENSOR OPTICAL TO ELECTRICAL INTERFACE

A radiation-hardened CMOS image sensor, or focal plane array (FPA), is used to capture the image of the sun. Figure 9 shows the optical to electrical interface on the FPA. The different ray traces show a 1^{o} change in each direction, both azimuth and elevation.

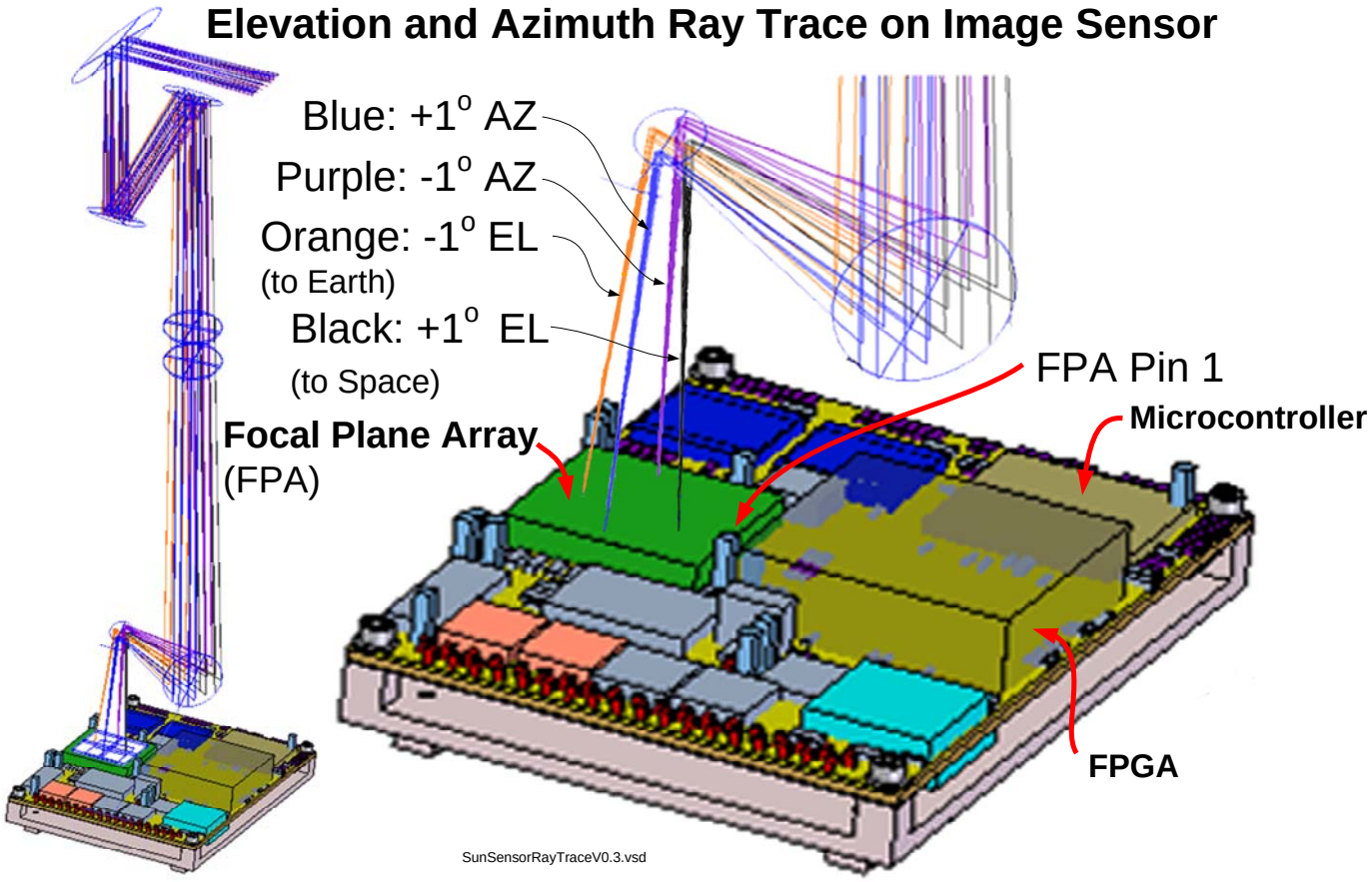


Figure 9 Sun Sensor Optical to Electrical Interface

An expanded view of the Optical to Electrical Interface is shown in Figure 10. This drawing shows the coordinate system for the FPA and the azimuth and elevation directions with respect to the earth. Figure 11 shows the Sun on the FPA with small boxes showing the expected locations that will be read by the software during fine tracking mode.

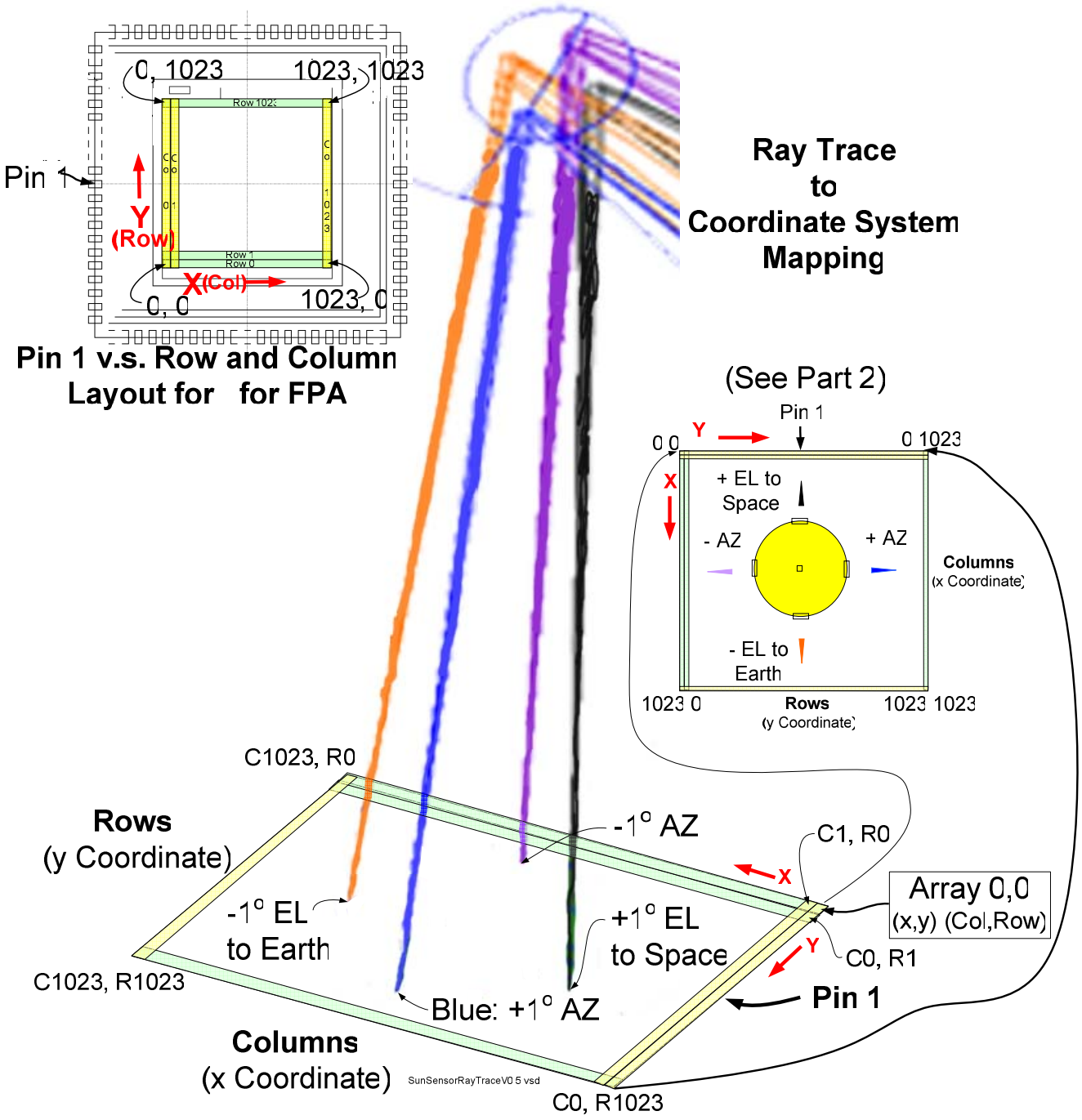


Figure 10 Detailed Optical to Electrical Interface

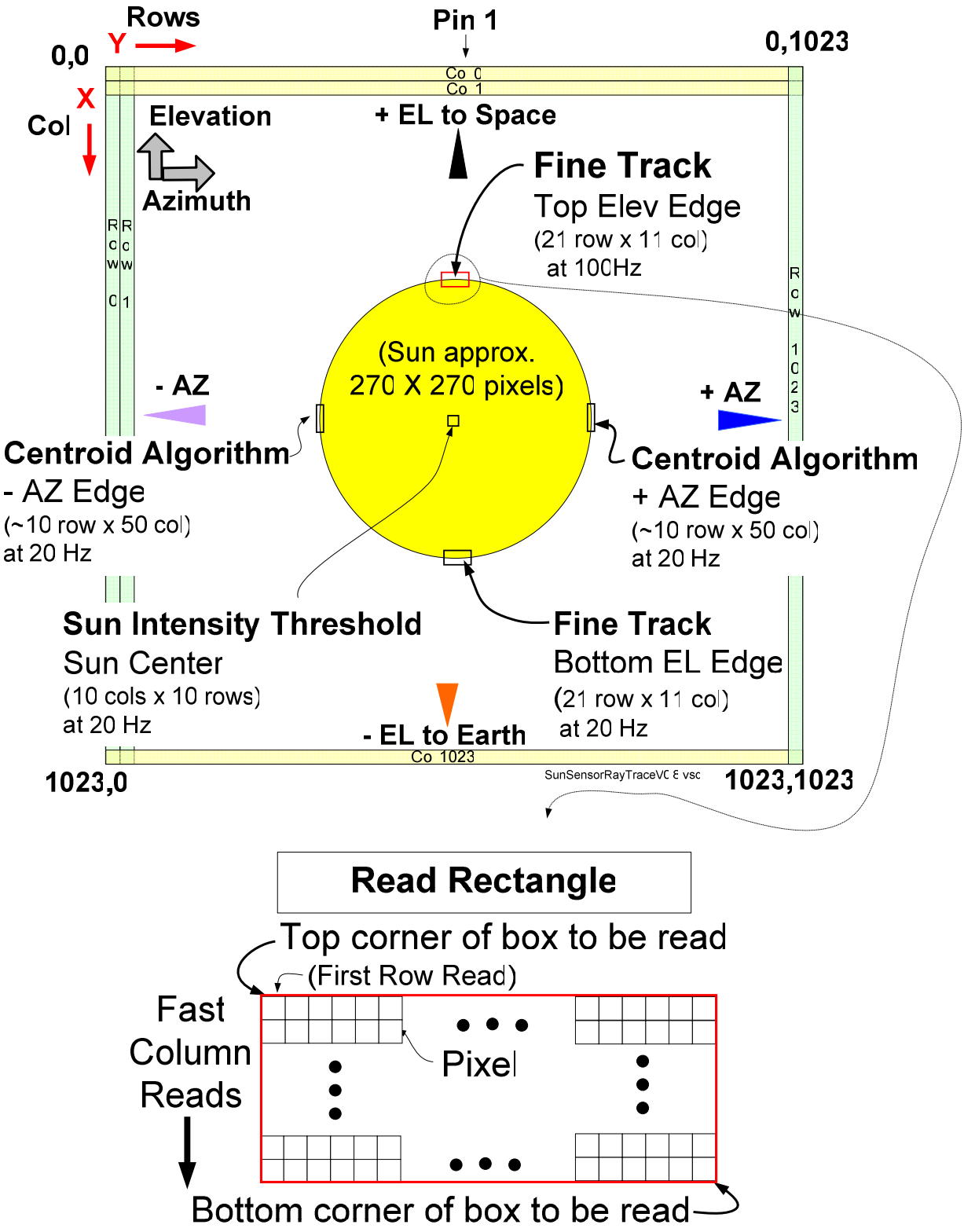


Figure 11 Reading Sun Image on FPA

6. ELECTRONICS UNIT MAJOR COMPONENTS DESCRIPTION

The SOFIE Electronics Unit is composed of the following components/sub-systems:

- Power Conditioning Unit
- Internal Power Cable
- Backplane
- Top Connectors
- Electronic Unit PC Boards:

Figure 12 shows a 3-D model of the SOFIE Electronics Unit identifying its major components. Figure 35 shows 3-D view of the position of each of the PC boards in Electronics Unit.

The components in the Steering Mirror Assembly and the Steering Mirror control boards are addressed in SDL/03-413 SOFIE SSG ICD and are not addressed in this document. The following sections describe the Power Conditioning Unit, the Power Flex Cable, the Electronics Unit Backplane, the individual PC boards within the Electronics Unit, and the Electronics Unit Top Connectors. .

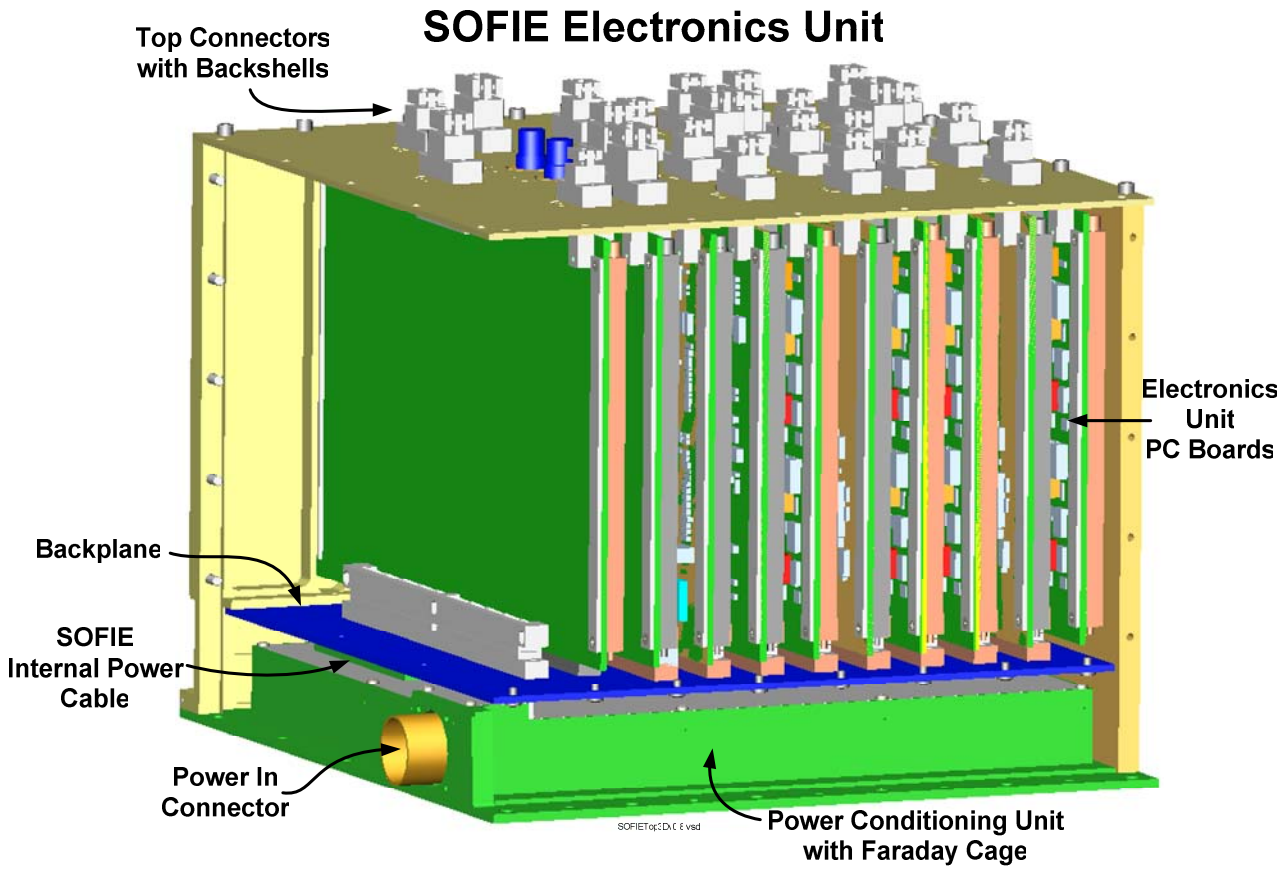


Figure 12 SOFIE Electronic Unit Components

6.1 Power Conditioning Unit Description

6.1.1 SOFIE Power Flow

Figure 13 is a high level diagram of the power flow within the SOFIE system. Figure 14 shows a diagram of the SOFIE Star Grounding System. The Spacecraft 28 volt power is converted by the SOFIE Power Conditioning Unit into the DC voltages required to operate the SOFIE Instrument. The power is fed from the Power Conditioning Unit to the Electronics Unit's Backplane by a flexible power cable. The Backplane distributes the power to the various boards in the system. The Sun Sensor Board receives its power through the cable from the C&DH board to the Sun Sensor Board. The Detector/Pre-Amp Boards receive their power through the cables from the Signal Conditioning Boards in the Electronics Unit. The Steering Mirror Position Sensor receives its power from the Steering Mirror Servo I/O Board in the Electronics Unit.

The power and signal grounds in the Instrument Unit are isolated from the Instrument Unit's chassis ground. The signal grounds for the PC Boards in the Electronics Unit are tied to the chassis ground in the Electronics Unit at a Single Point Ground point where the Flex Power Cable connects to the Electronics Unit's Backplane. The detailed power distribution and grounding for the SOFIE Instrument is shown in Figure 15 and Figure 16.

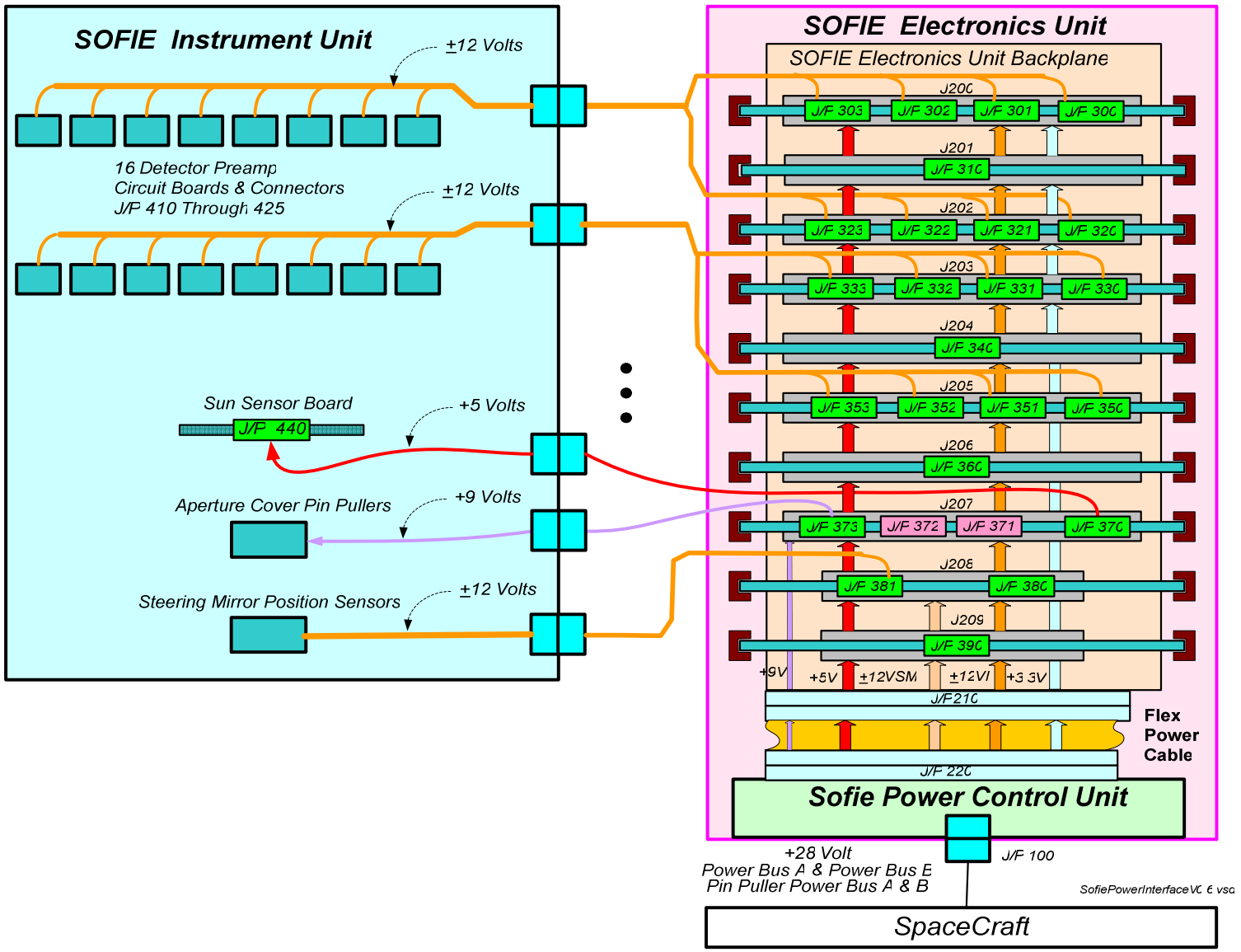


Figure 13 SOFIE Power Flow Overview

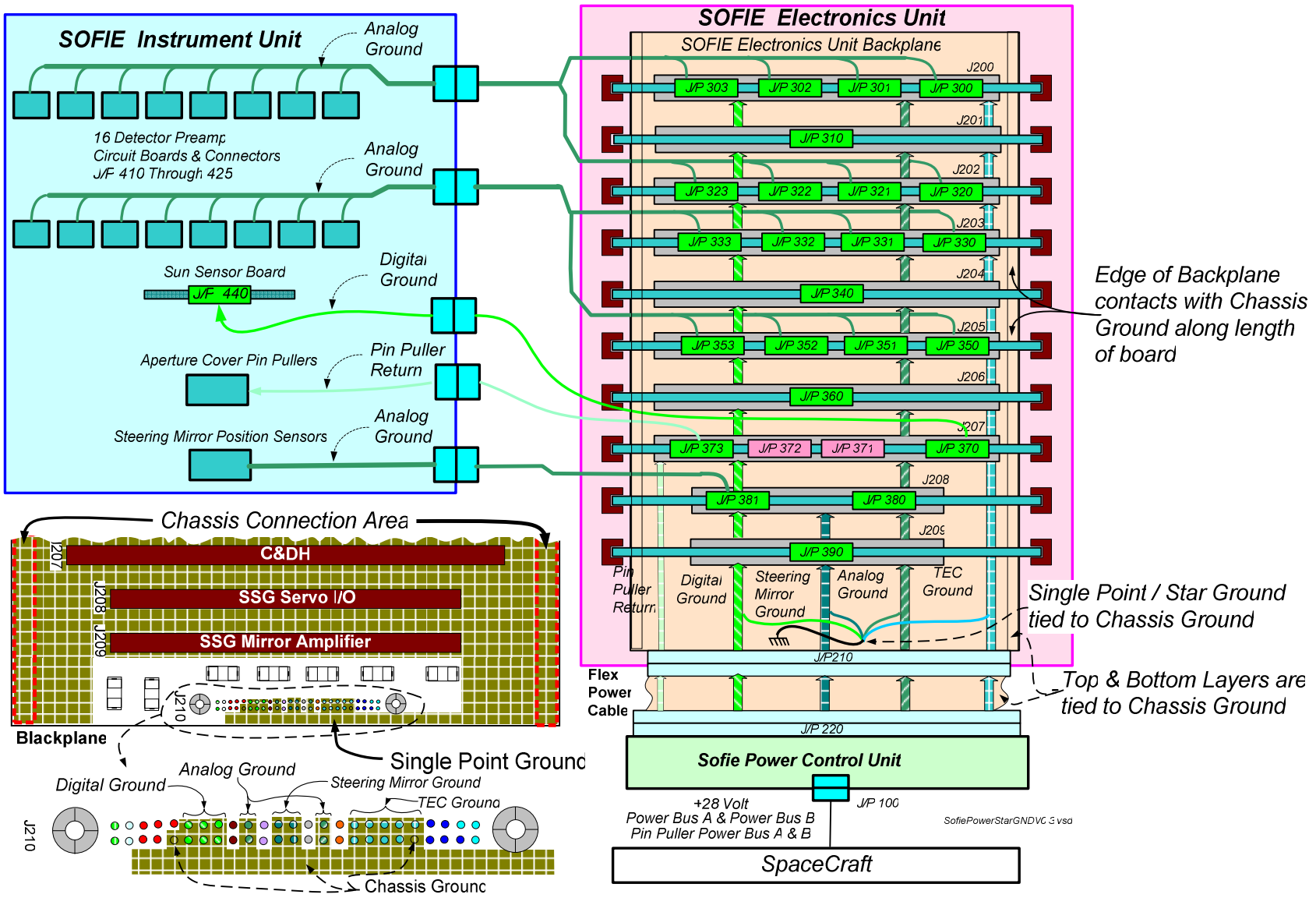


Figure 14 SOFIE Star Grounding Diagram

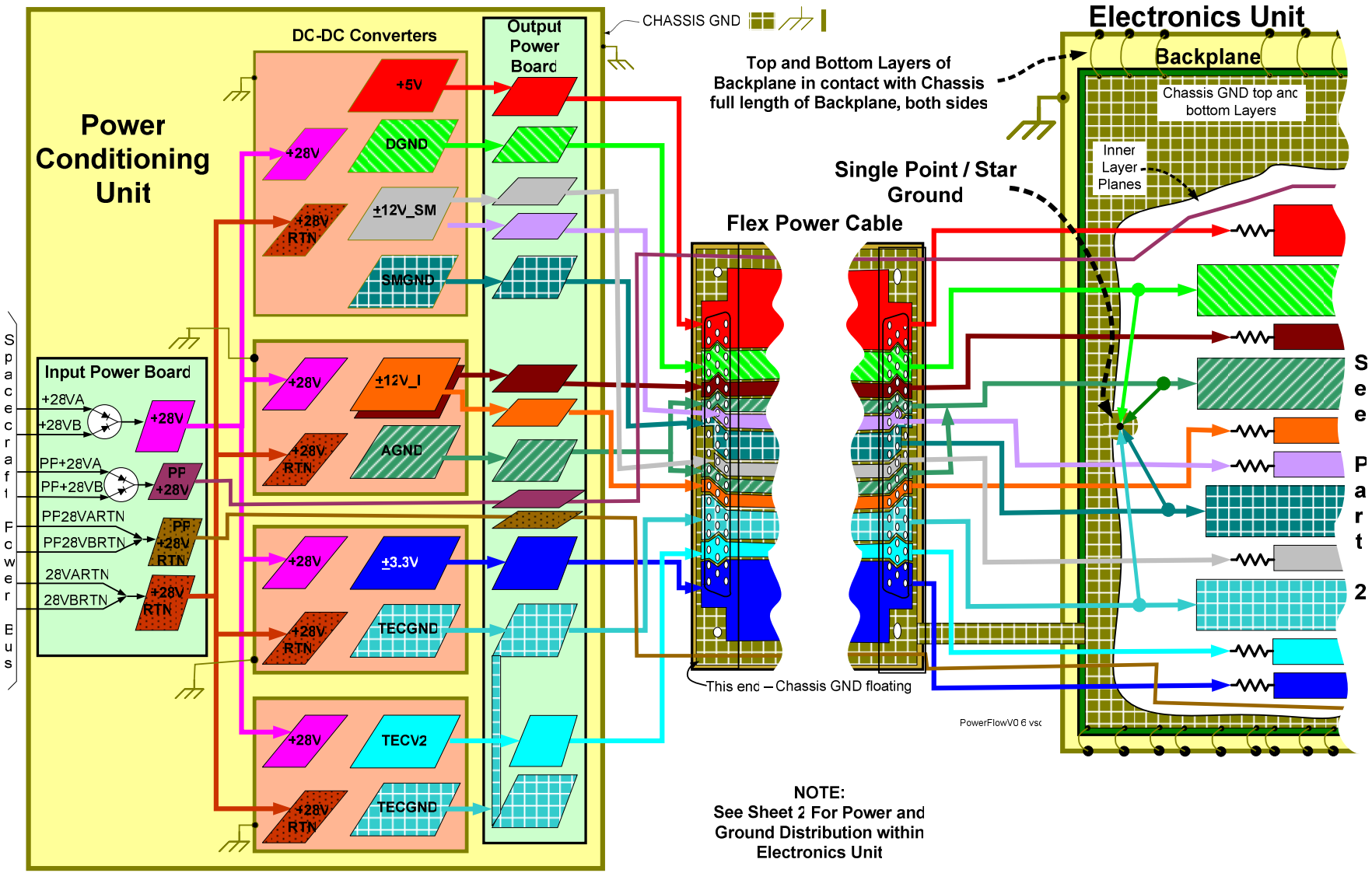


Figure 15 SOFIE Power Distribution and Grounding - part 1

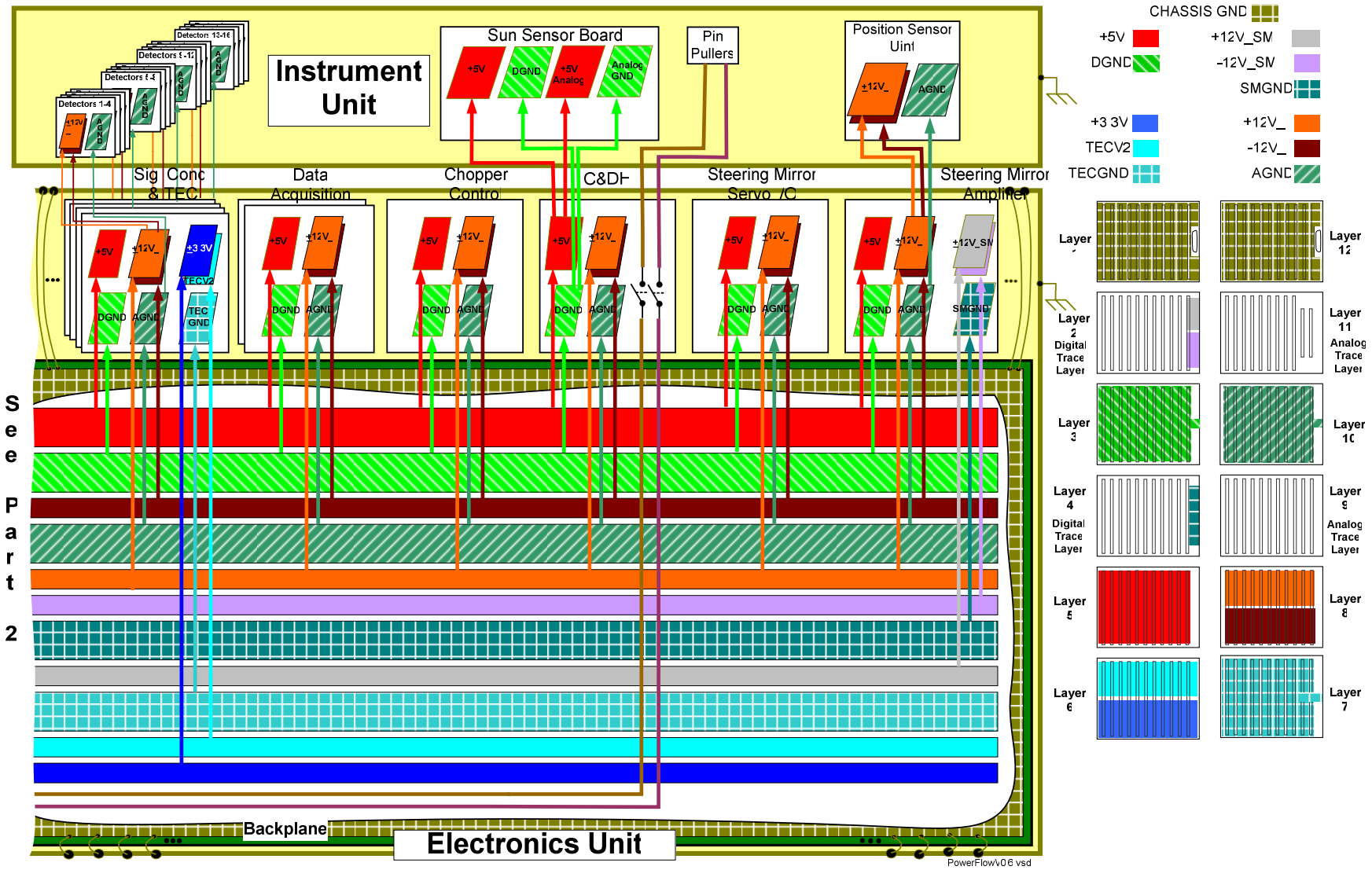
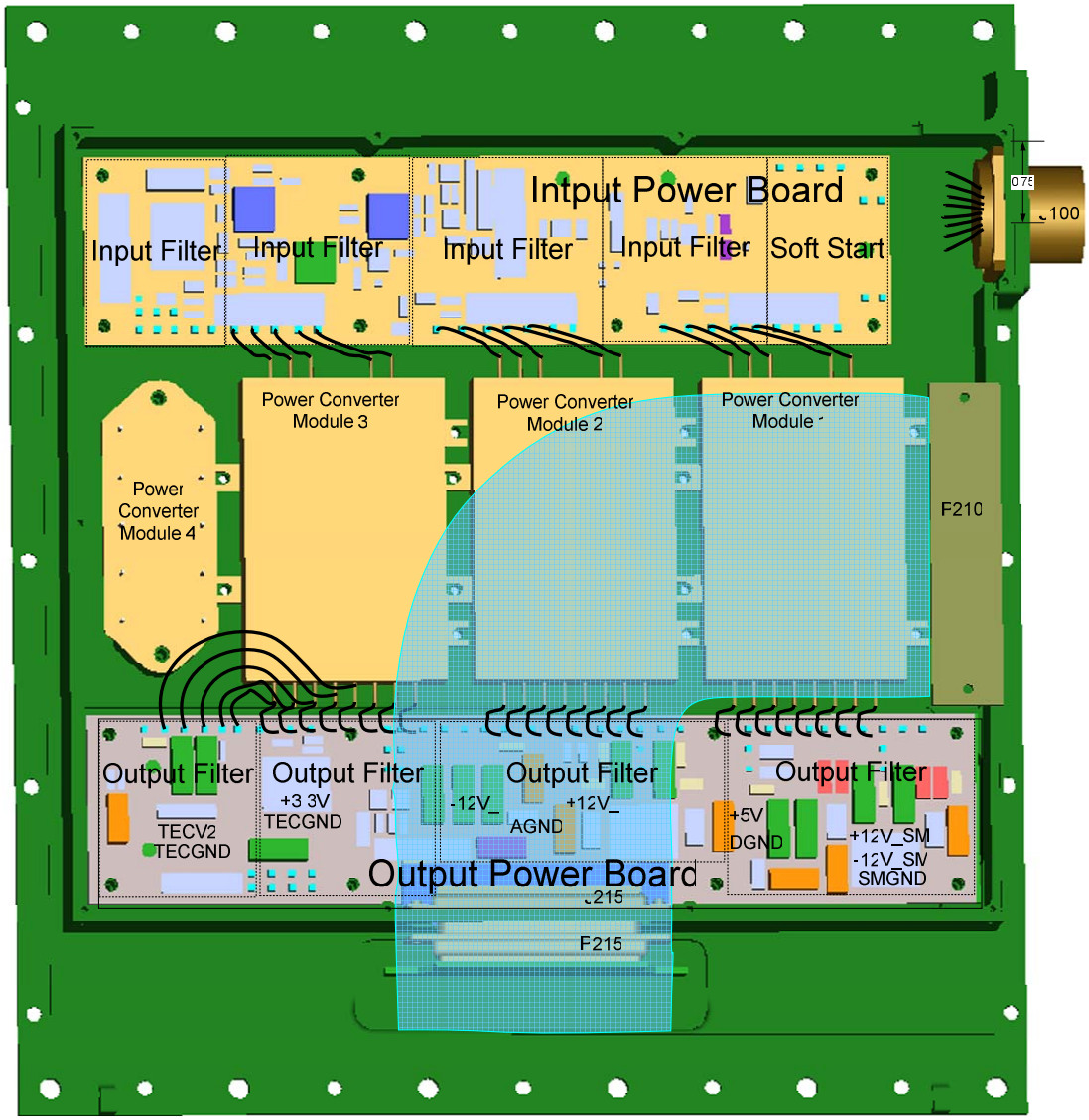


Figure 16 SOFIE Power Distribution and Grounding - part 2

6.1.2 Power Conditioning Unit Description

The approach for the Power Conditioning utilizes off-the-shelf DC/DC modules to convert the 28 volt input power into the voltages needed by SOFIE. Two PCB are used, one for soft start and input filtering and one for output filtering. A 3-D view of the Power Conditional Unit is shown in Figure 17. The power from the Power Conditioning Units is supplied to the backplane through a flexible power cable.



J100 Power In Connector
p/n LJTPQ00RE-13-98F(467)
MS27656E13(467)98F
Keying None

J215 Power Out Connector
p/n SND50F5R70TG
Keying None

F215 Power Cable Connectors - Power Box End
p/n SND50M300E2G
Keying None

F210 Power Cable Connectors - Backplane End
p/n Integrated Pins
Keying None

Power Converter Module 1 Triple Output +5 Volts ±12 Volts 40Watts 20/20 Steering Mirror
p/n International Rectifier M3H28512T

Power Converter Module 2 Dual Ouput ±12 Volts 40 Watts Instrumentation
p/n International Rectifier M3H2812D

Power Converter Module 3 Single Output +3 3 Volts 30 Watts TEC Cooler
p/n International Rectifier M3H2803R3S

Power Converter Module 4 *not used*

Jumpers between the Output Filter for the +3 3 Volt module and the TECV2 Module can be used to jumper the +3 3 volts to the TECV2 outputs if only one TEC voltage is needed

Figure 17 Power Conditioning Unit 3-dimensionsion View

6.1.3 Power Input PC Board Specification

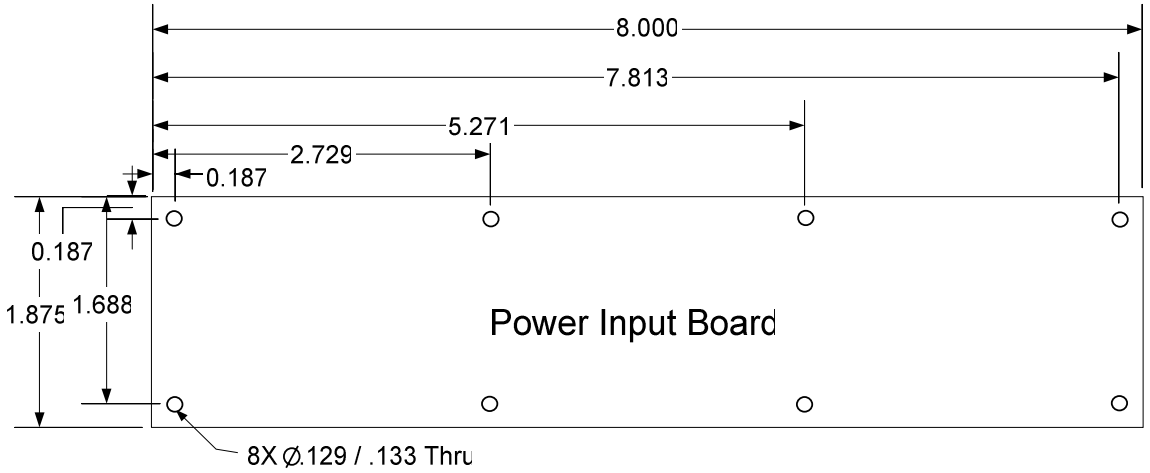


Figure 18 Power Input PCB Specification

6.1.4 Power Output PC Board Specification

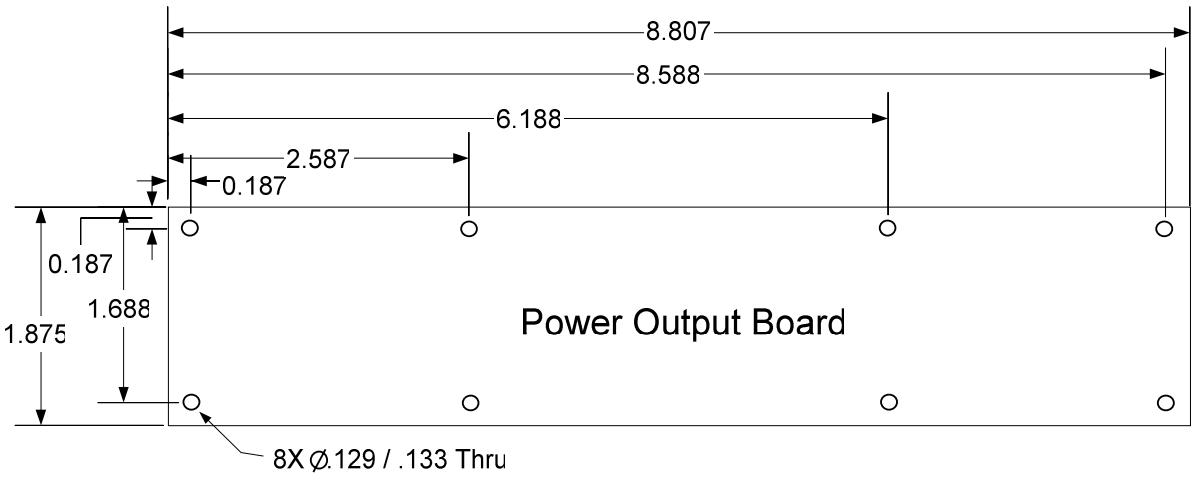


Figure 19 Power Output PCB Specification

6.1.5 Power Flex Cable Specification

The Flexible Power cable is constructed using “Ridged-Flex” fabrication technology which integrates standard ridged PC Boards at the end of the cable with a flexible region in between. The drawings defining the Flex Power Cable are shown in Figure 20 through Figure 25.

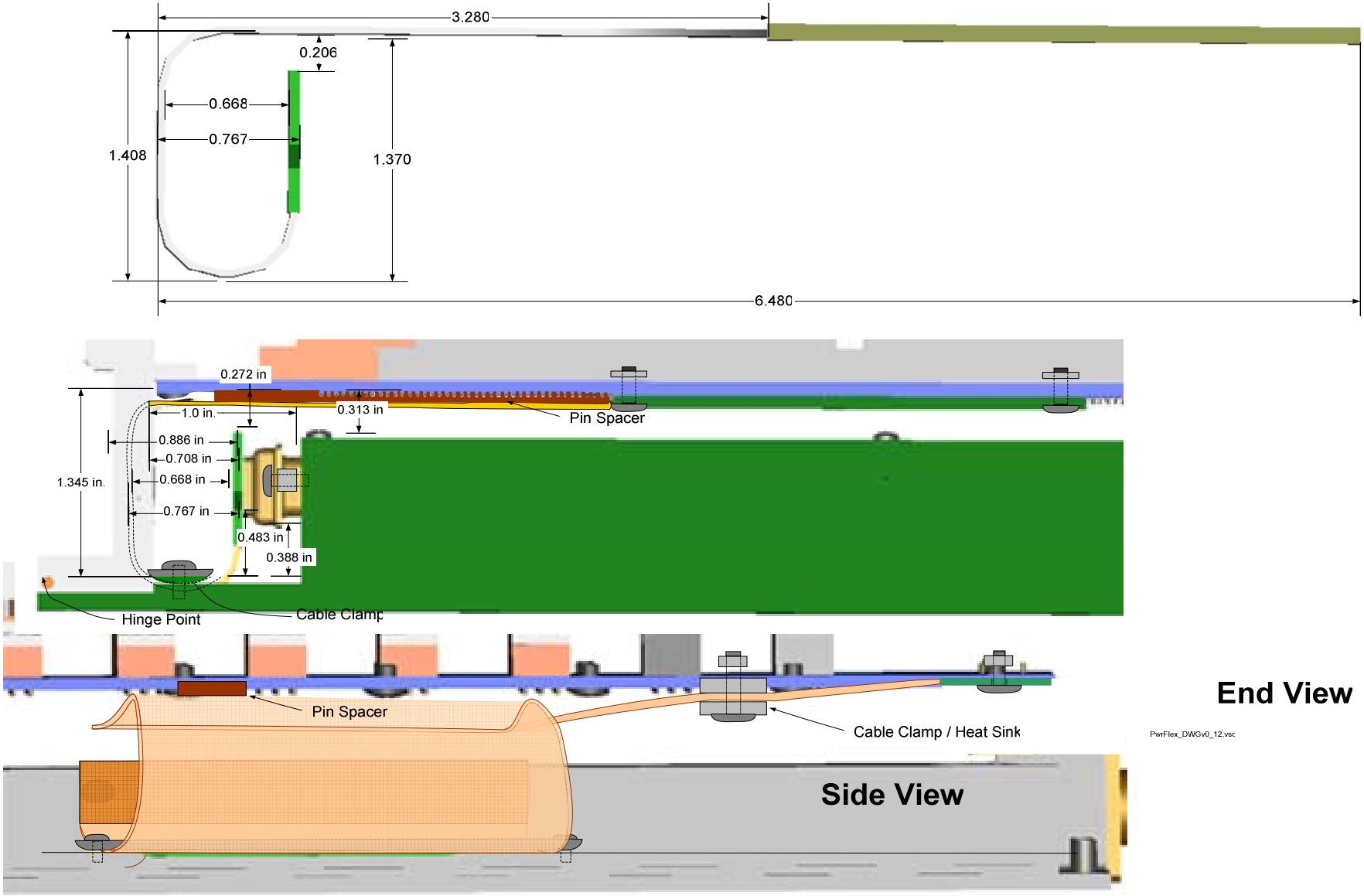


Figure 20 Power Flex Cable Specification - Part 1

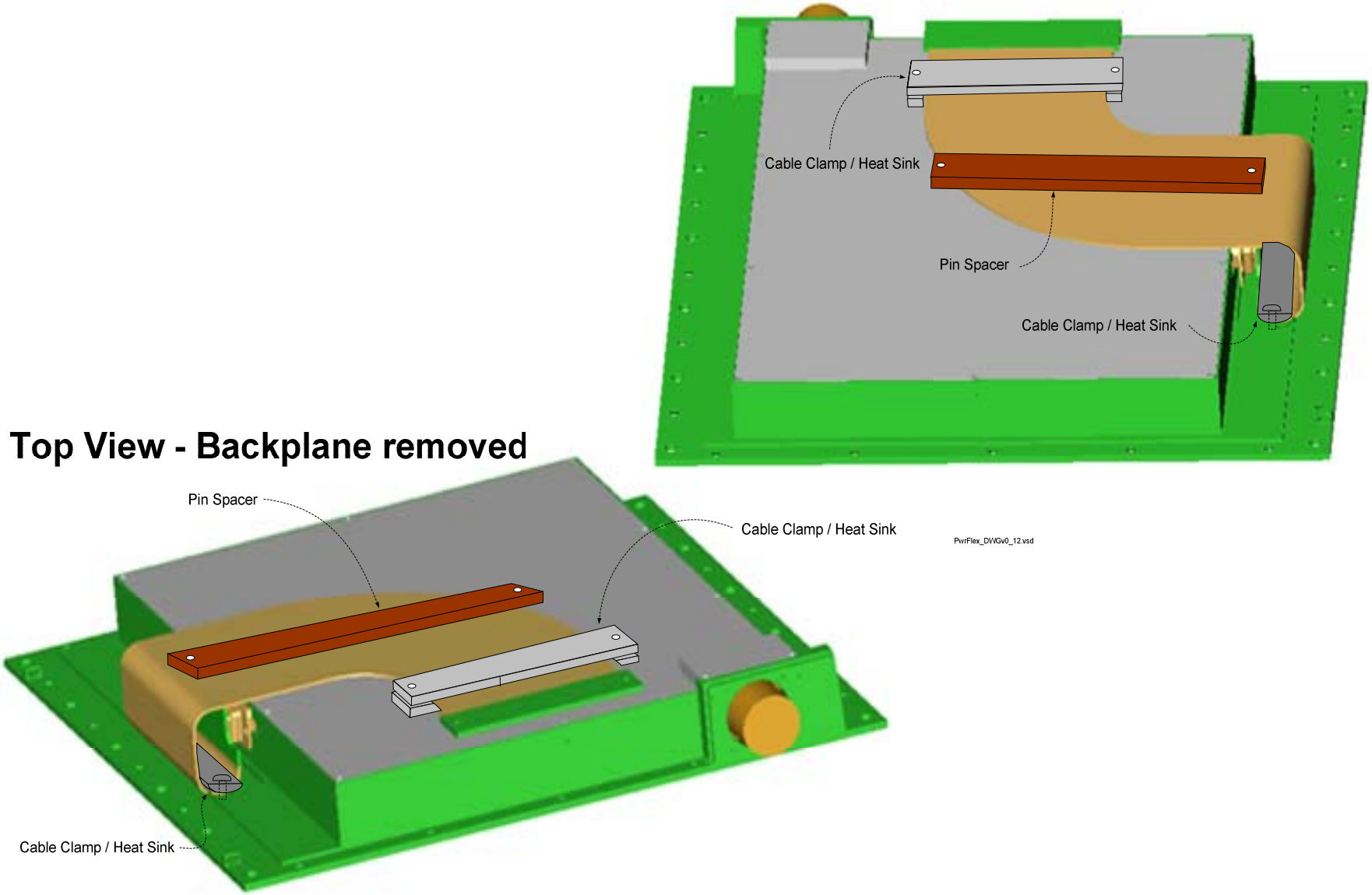


Figure 21 Power Flex Cable Specification - Part 2

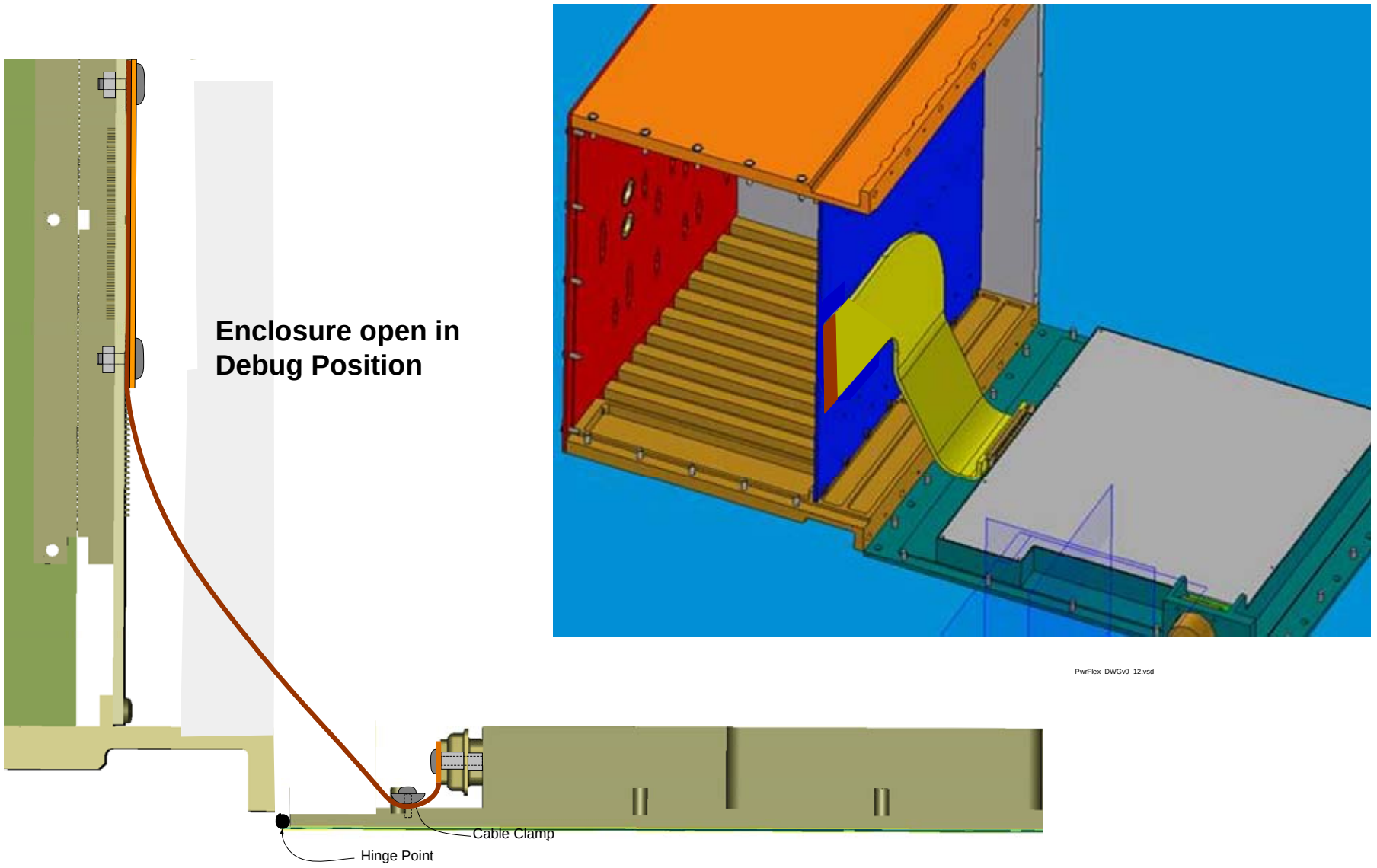


Figure 22 Power Flex Cable Specification - Part 3

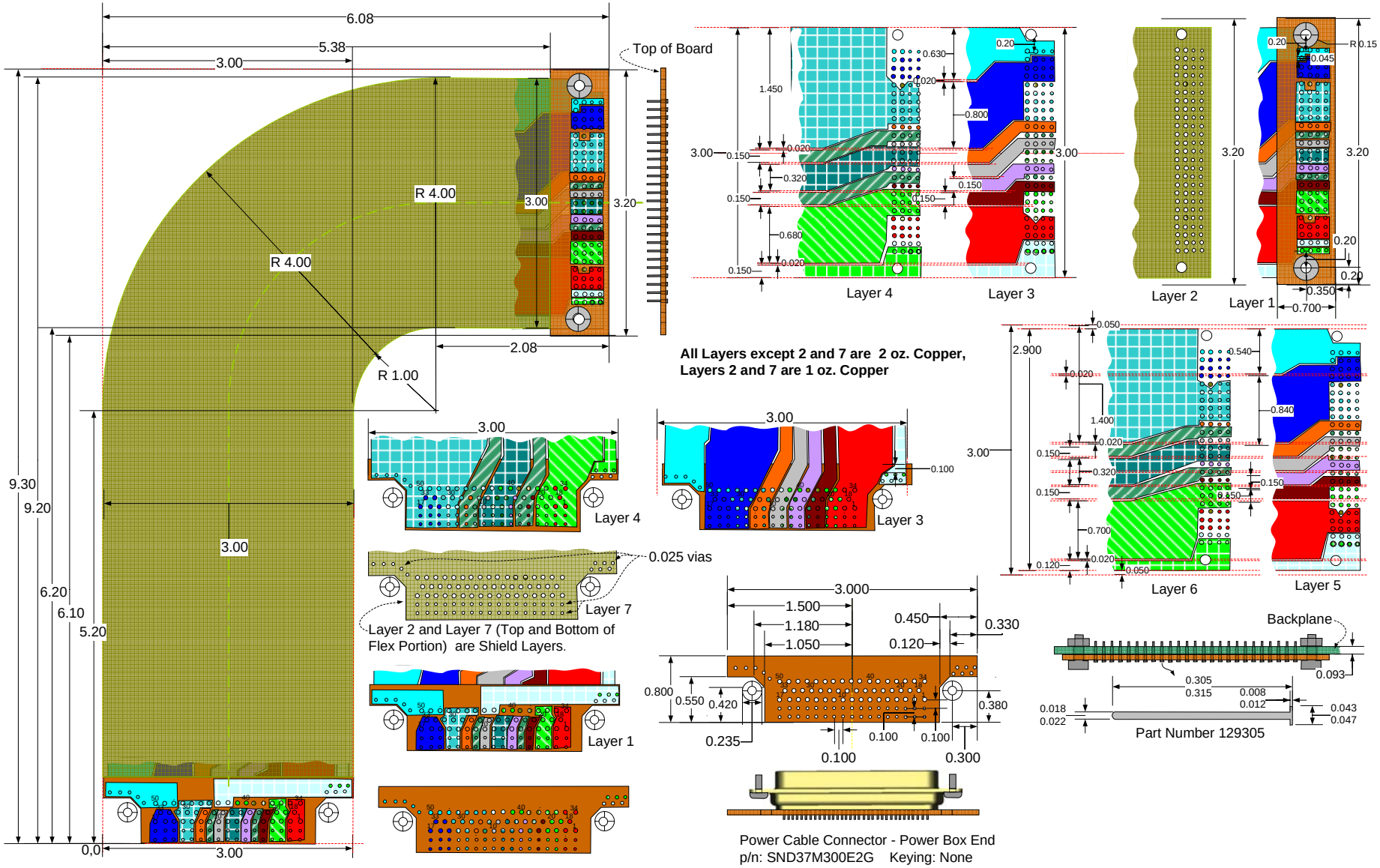


Figure 23 Power Flex Cable Specification - Part 4

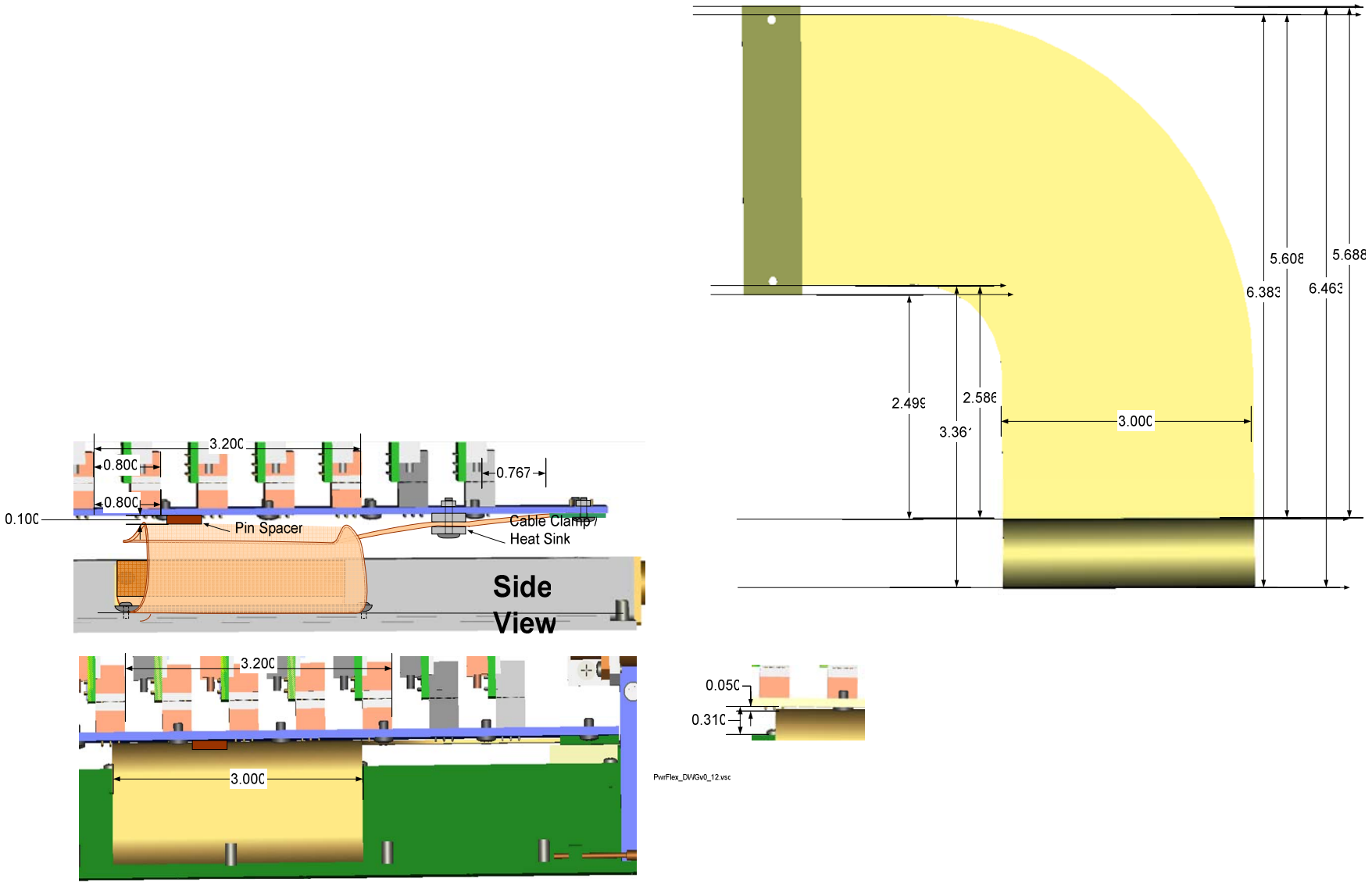


Figure 24 Power Flex Cable Specification - Part 5

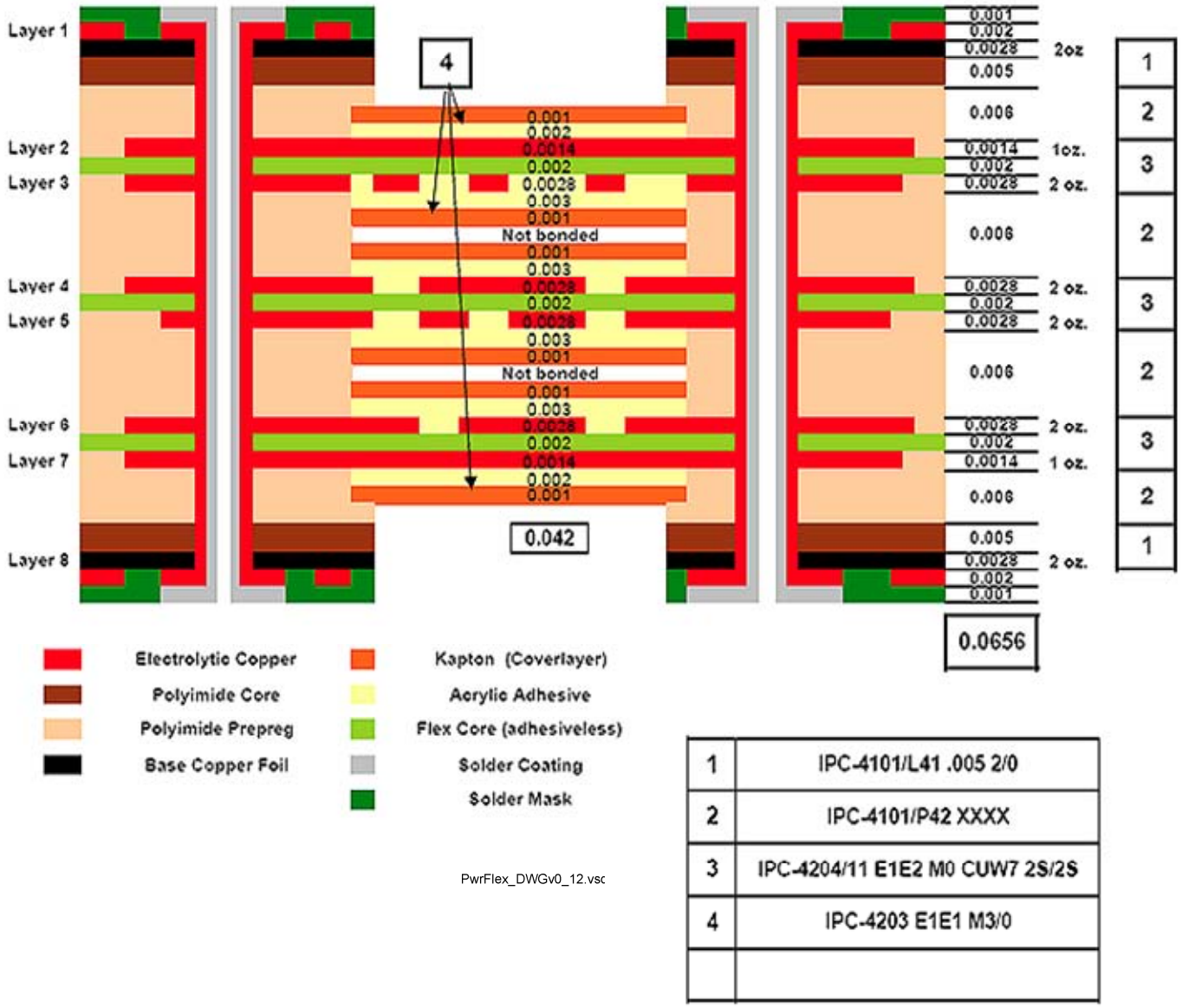
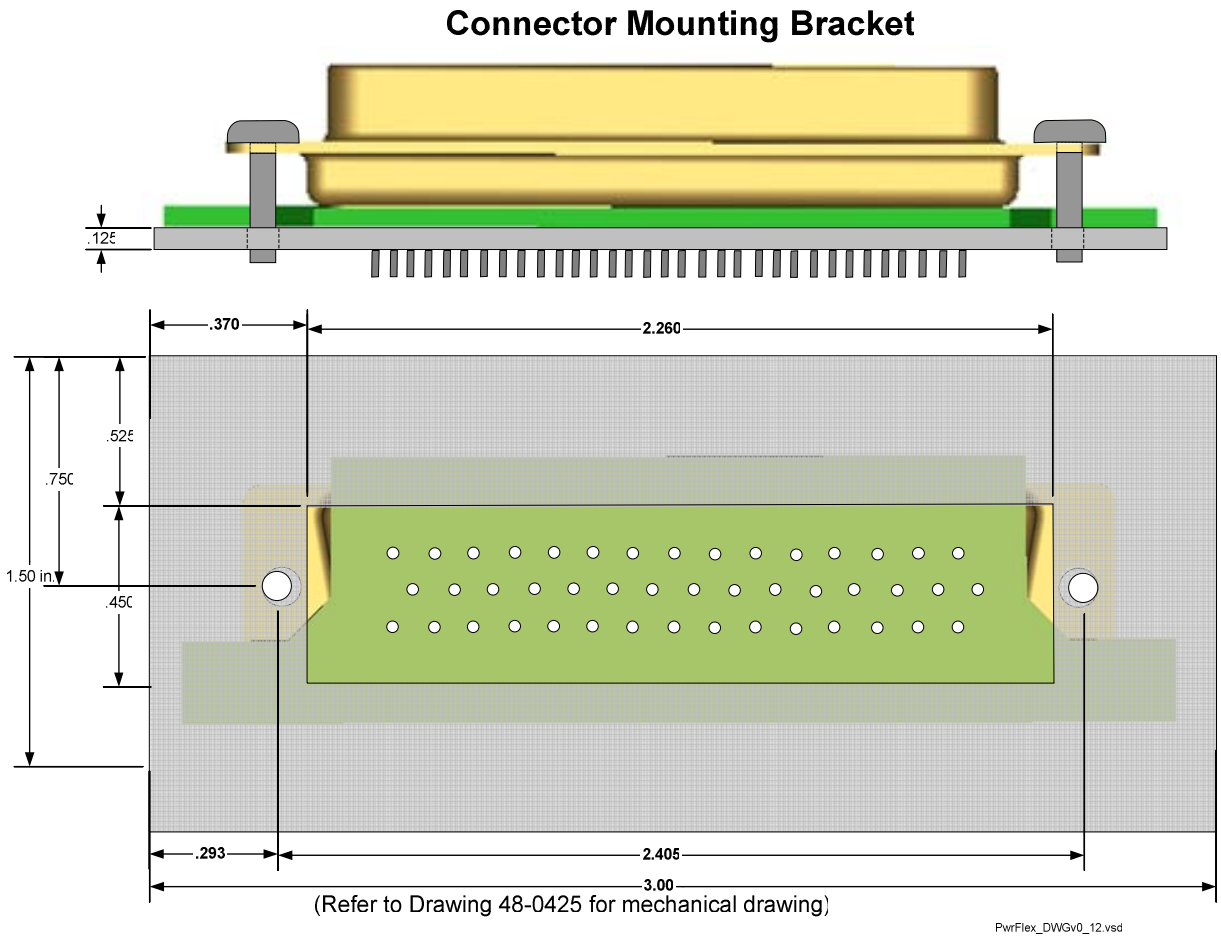


Figure 25 Power Flex Cable Specification - Part 6

Figure 26 specifies the bracket for holding the connector on the flex cable in the proper location during wave soldering.



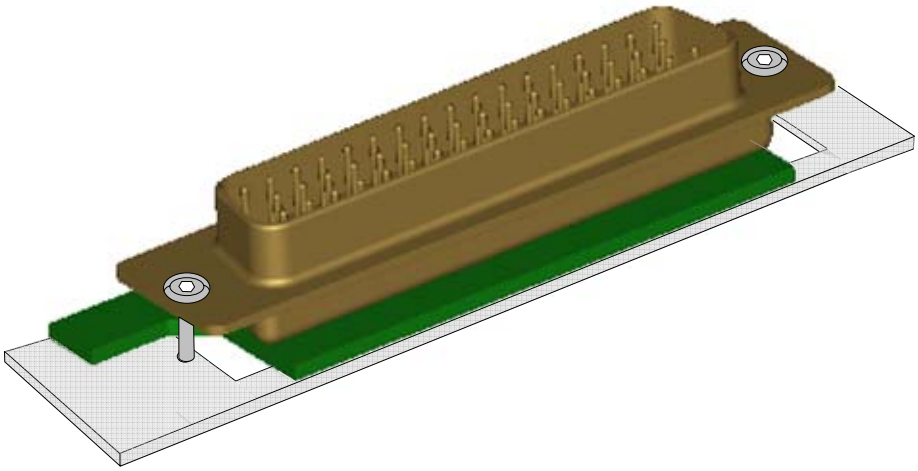


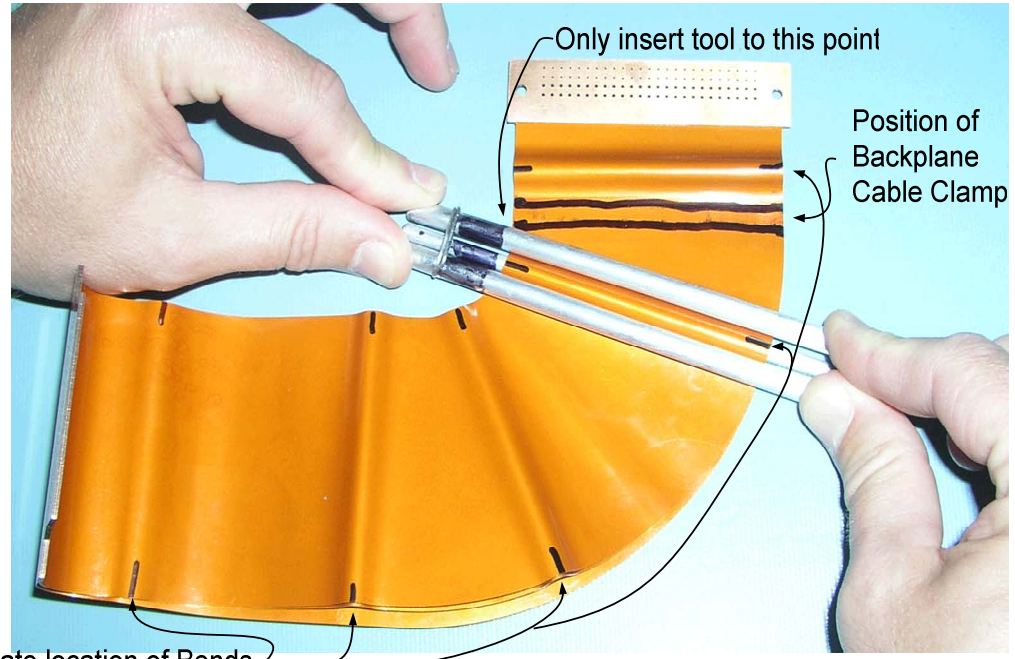
Figure 26 Power Flex Cable Specification - Part 7

The procedure for making the bends in the Flex Power Cable to compensate for the 270^{o} bend needed to connect to the Power Conditioning unit is shown in Figure 27 and Figure 28.

Flex Power Cable Bending Procedures - Part 1

Tool For making Bends

Top Layer Bent First - Tool Insertion



After First Layer Bends Complete

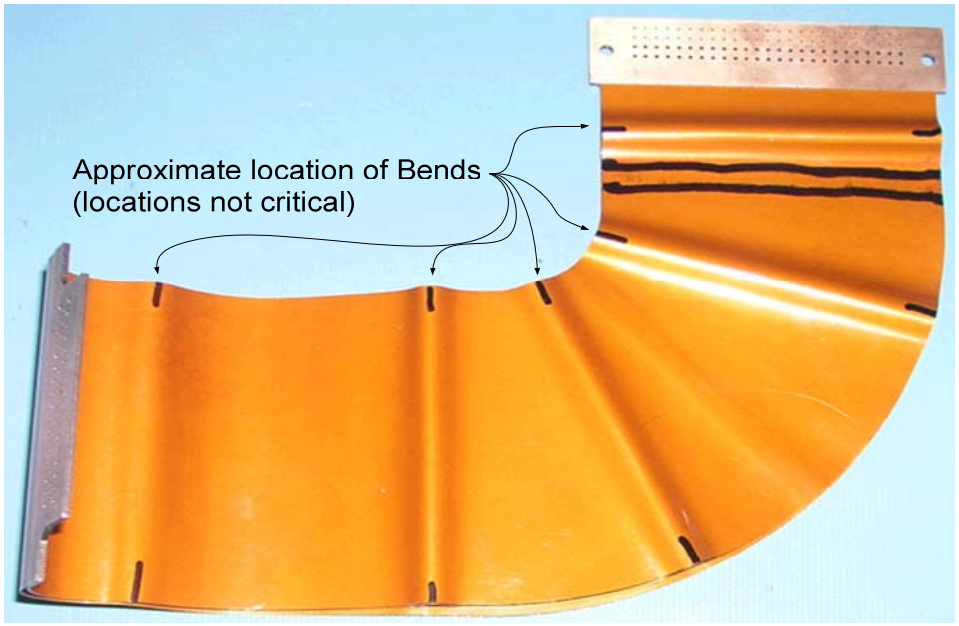
Only 1st Layer Bent

FlexCableVendV0.1.vsd

Figure 27 Flex Cable Bend Procedures - Part 1

Flex Power Cable Bending Procedures - Part 2

Making Second Layer Bend



All Bends Complete

After Second Layer Bends

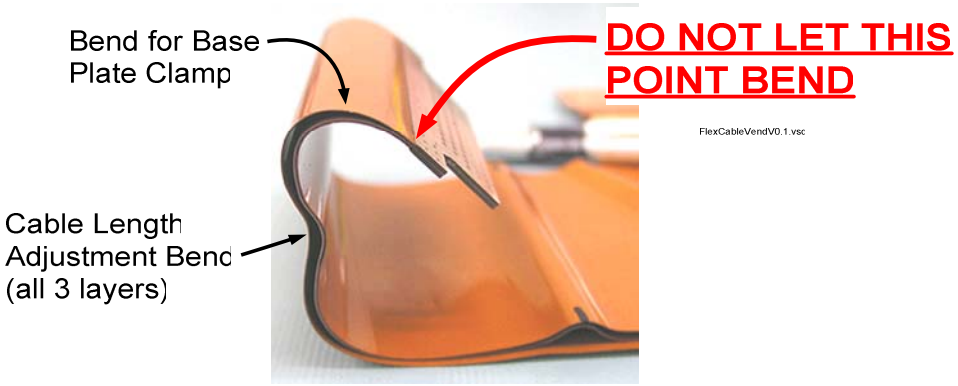
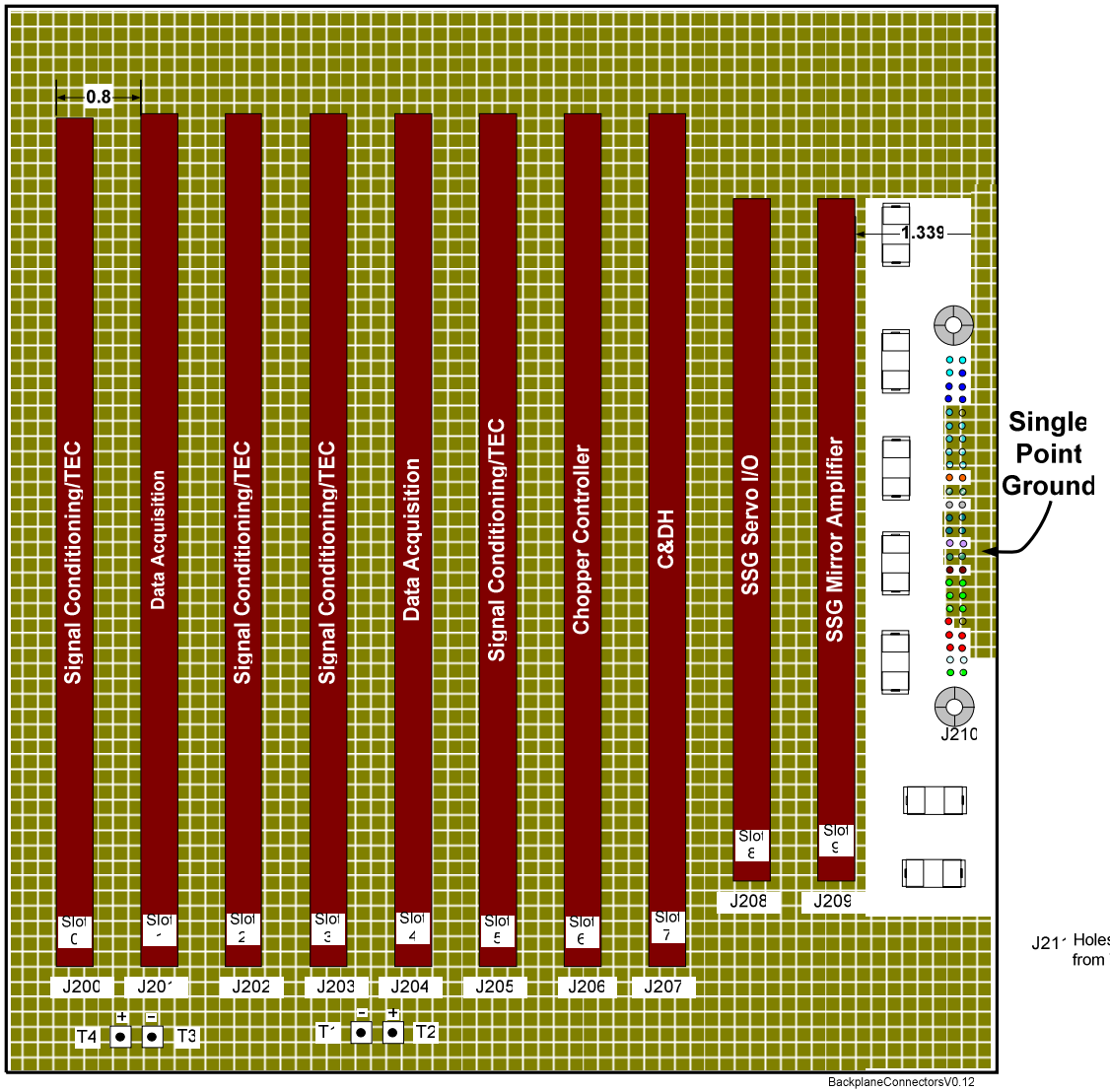


Figure 28 Flex Cable Bend Procedures - Part 2

6.2 Back Plane Board

The location and types of connectors for Electronics Unit Back Plane are shown are in Figure 29. The definition of the Electronics Unit's Back Plane Printed Circuit Board is shown in Figure 30. Figure 31 shows the power pin assignments for the Electronics Unit's Back Plane. The signals going between the connectors on the Back Plane are shown in Figure 32 and Figure 33. The detailed pin assignments for the Backplane connectors are shown in the Backplane Schematic (SDL drawing 48-0068). The Back Plane PCB layer definitions are shown in Figure 34.



J200 Board: Signal Conditioning/TEC 1 Keying: ´
p/n Proto: WG208SAD9SY-1-DO1 p/n Flight: WG208SAD9SY-1-DO1
Mate p/n: WG208PR9SY-1-DO1 p/n Flight: WG208PR9SY-1-DO´

J201 Board: Data Acquuisitior Keying: 5
p/n: WG208SAD9SY-5-DO´
Mate p/n: WG208PR9SY-5-DO1

J202 Board: Signal Conditioning/TEC 2 Keying: 2
p/n Proto: WG208SAD9SY-1-DO1 p/n Flight: WG208SAD9SY-2-DO1
Mate p/n: WG208PR9SY-1-DO1 p/n Flight: WG208PR9SY-2-DO´

J203 Board: Signal Conditioning/TEC 3 Keying: 3
p/n Proto: WG208SAD9SY-1-DO1 p/n Flight: WG208SAD9SY-3-DO1
Mate p/n: WG208PR9SY-1-DO1 p/n Flight: WG208PR9SY-3-DO´

J204 Board: Data Acquuisitior Keying: 6
p/n: WG208SAD9SY-6-DO´
Mate p/n: WG208PR9SY-6-DO1

J205 Board: Signal Conditioning/TEC 4 Keying: 4
p/n Proto: WG208SAD9SY-1-DO1 p/n Flight: WG208SAD9SY-4-DO1
Mate p/n: WG208PR9SY-1-DO1 p/n Flight: WG208PR9SY-4-DO´

J206 Board: Chopper Controller Keying: 9
p/n: WG208SAD9SY-9-DO´
Mate p/n: WG208PR9SY-9-DO1

J207 Board: Command & Data Handling (C&DH) Keying: 10
p/n: WG208SAD9SY-10-DO1
Mate p/n: WG208PR9SY-10-DO1

J208 Board: SSG Servo I/O Keying: 1´
p/n: WG160SAD9SY-11-DO1
Mate p/n: WG160PR9SY-11-DO´

J209 Board: SSG Mirror Amplifier Keying: 12
p/n: WG160SAD9SY-12-DO1
Mate p/n: WG160PR9SY-12-DO´

Board: 208 Pin Extender Carc Keying: 65
p/n Top: WG208SOR9SY-65-DO´
p/n Bottom: WG208PR9SY-65-DO1

Board: 160 Pin Extender Carc Keying: 65
p/n Top: WG160SOR9SY-65-DO´
p/n Bottom: WG160PR9SY-65-DO1

J210 Power Connector
p/n: SND37M300TG
Keying: None

J21´ Holes for 4 discrete wires coming from Temperature Sensors

Figure 29 Back Plane Connector Location and Part Numbers

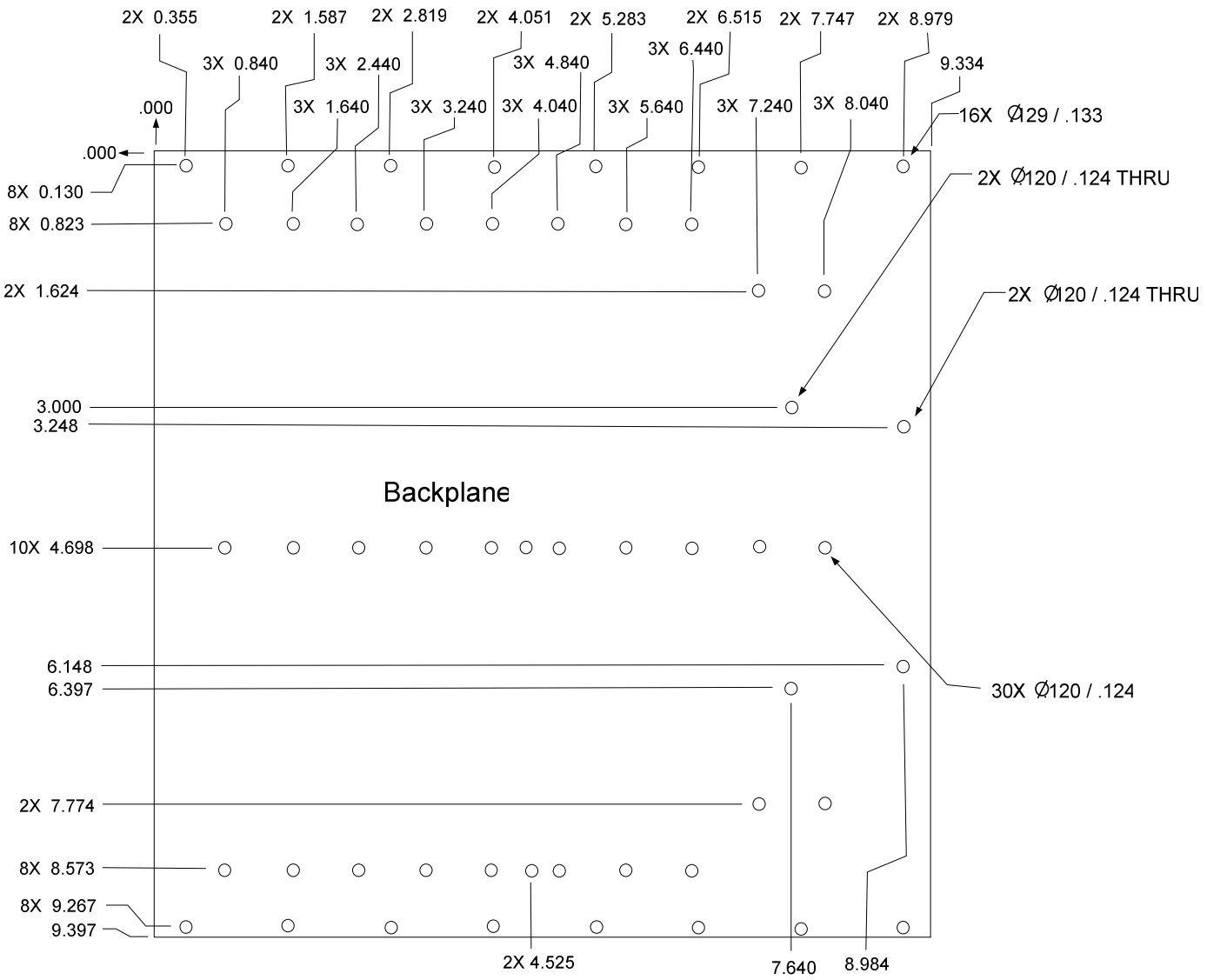


Figure 30 Instrument Unit Backplane PCB Definition

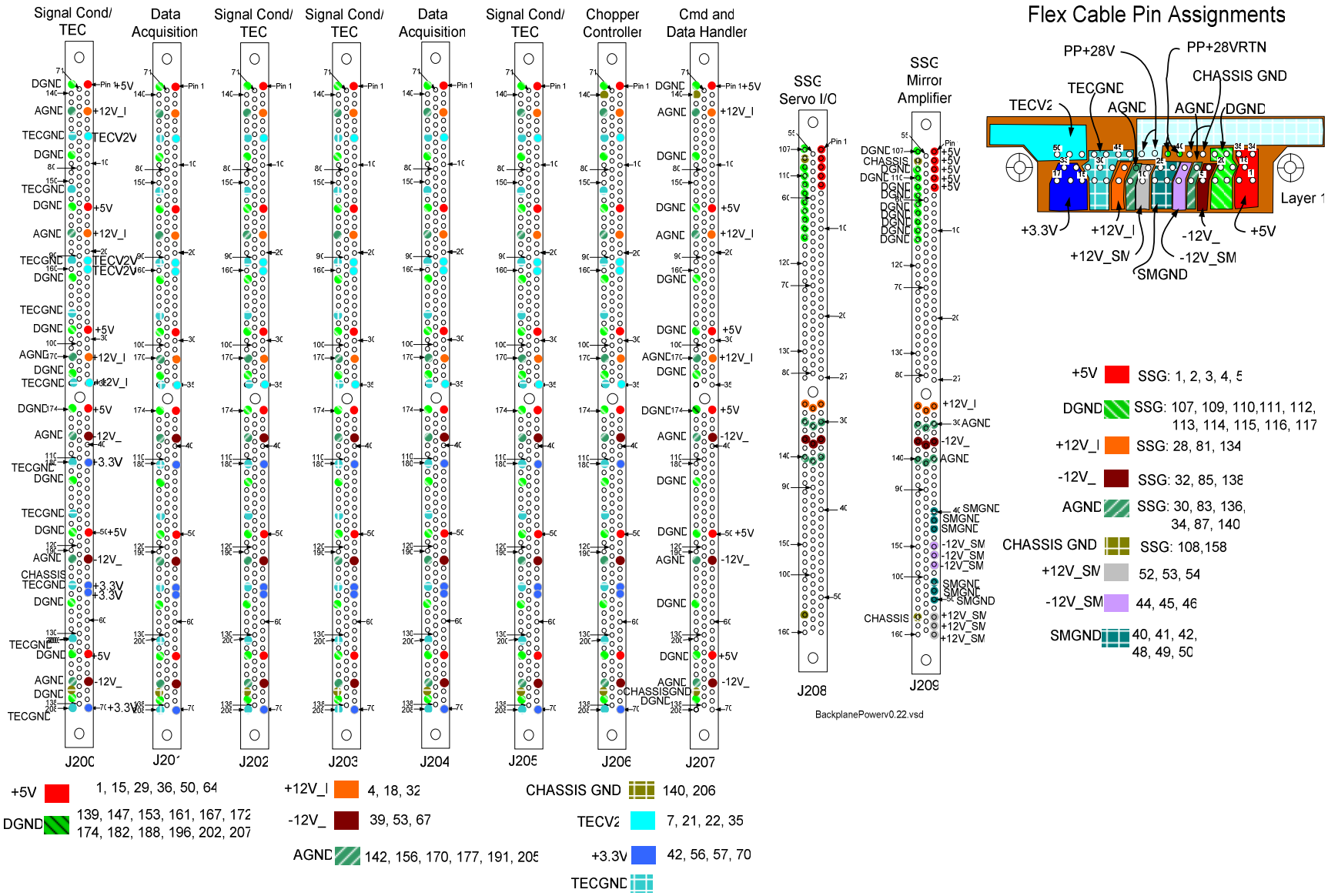


Figure 31 Back Plane Power Pin Assignments

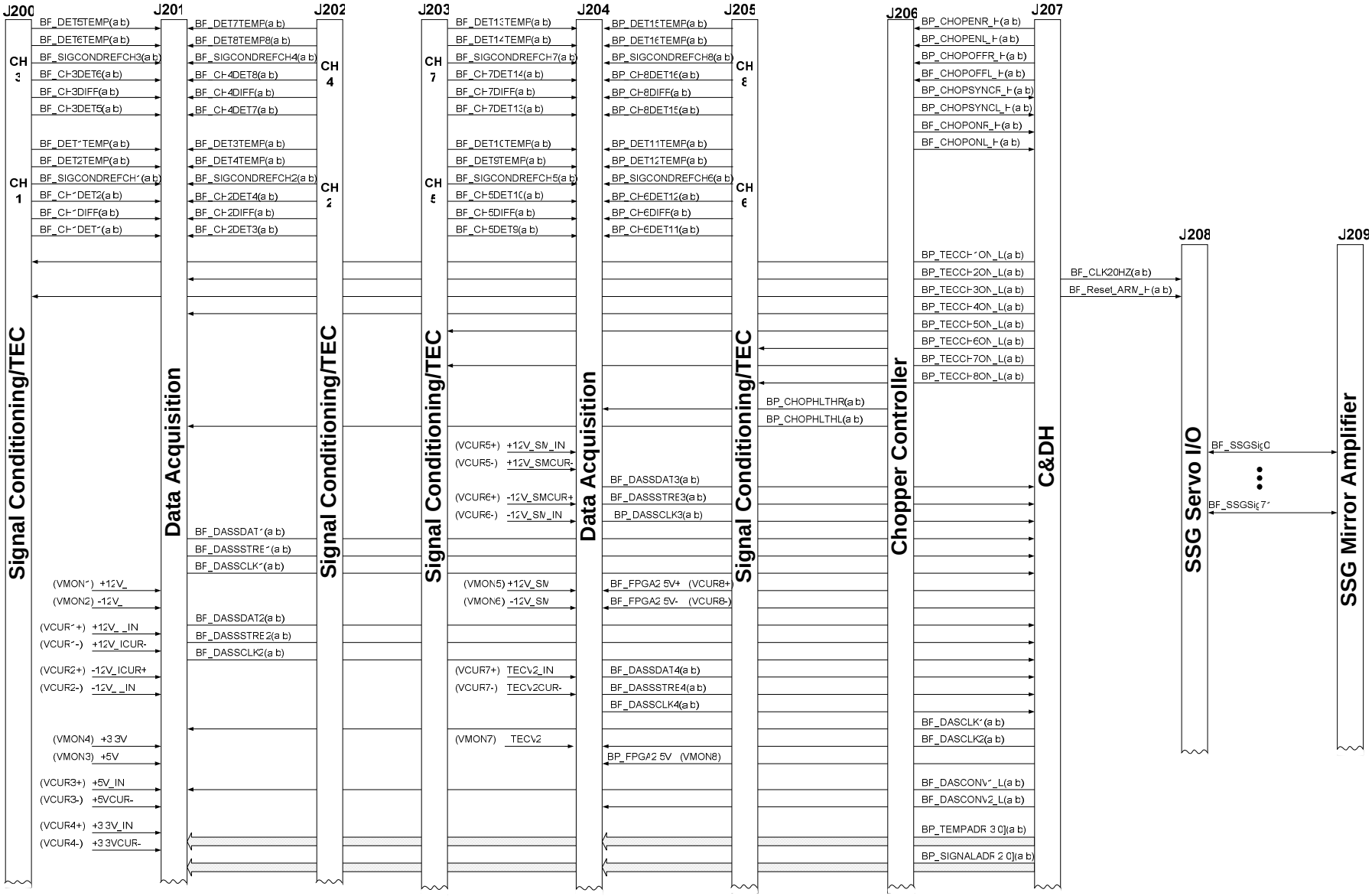


Figure 32 Back Plane Signals - Part 1

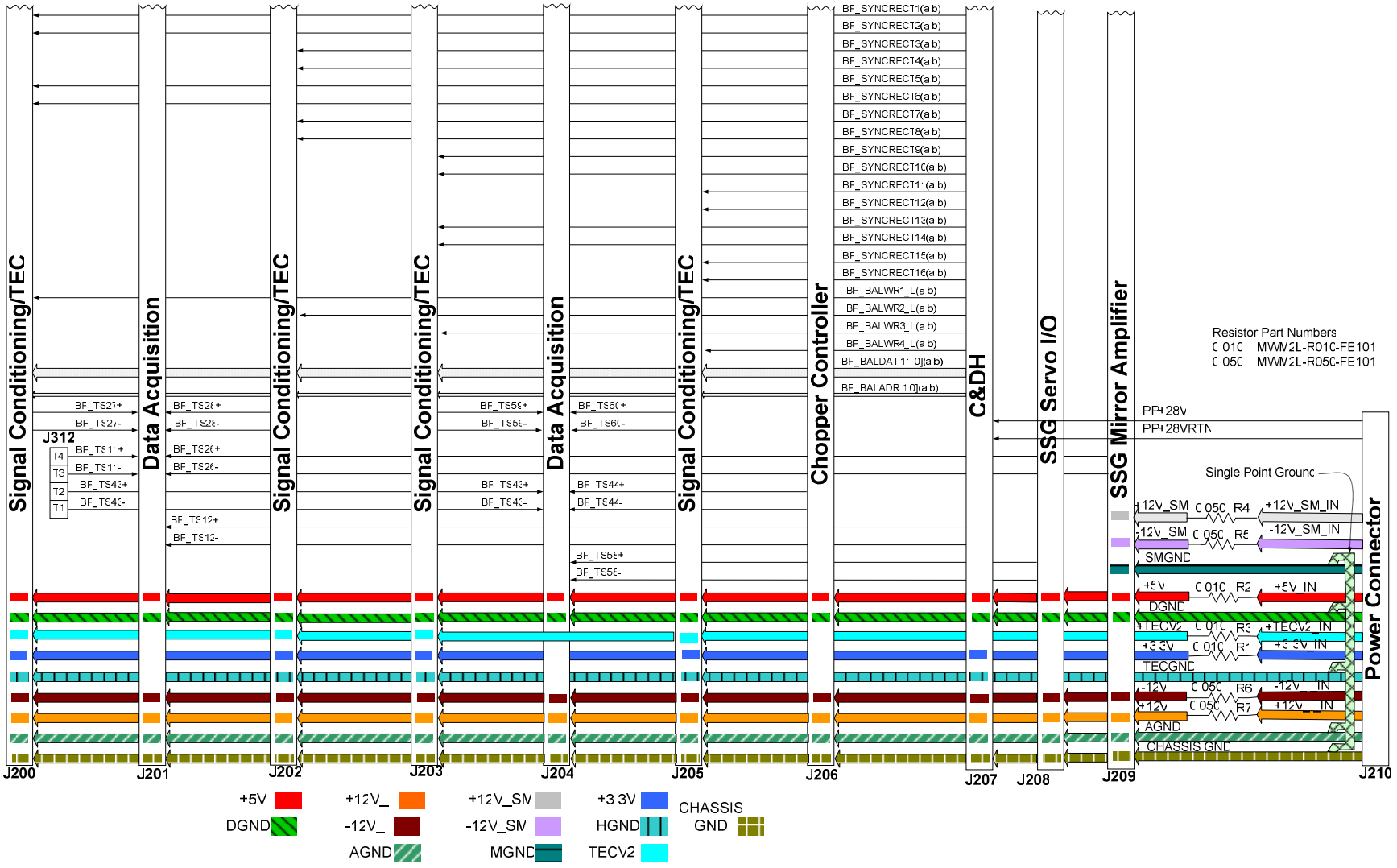


Figure 33 Back Plane Signals - Part 2

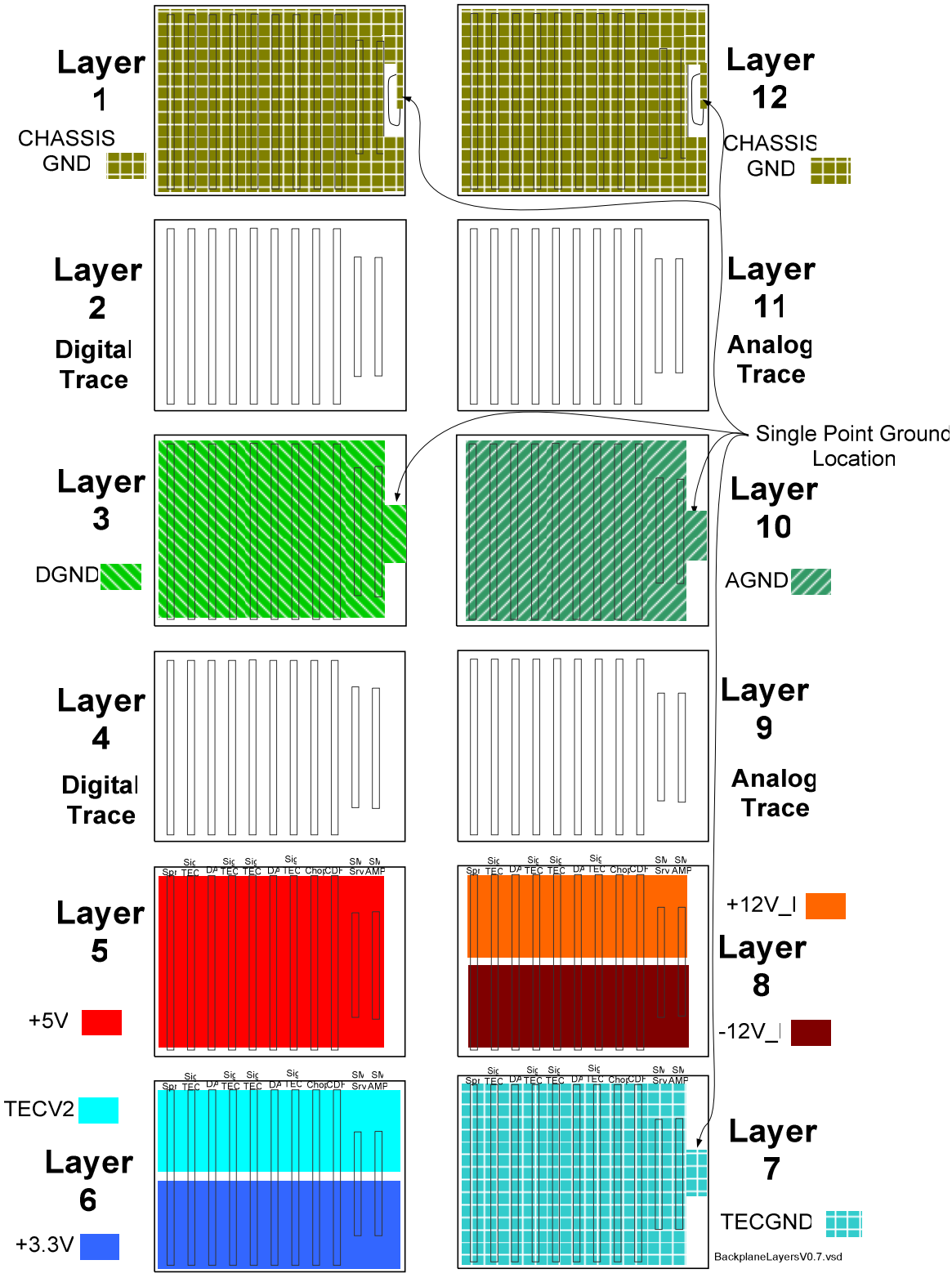


Figure 34 Back Plane Layer Definitions

6.3 Electronics Unit PC Boards Description

The 3-D model of the SOFIE Electronics Unit in Figure 35 shows the location and types of Printed Circuit Boards in the Electronics Unit. The boards share a common specification that is described in the following section.

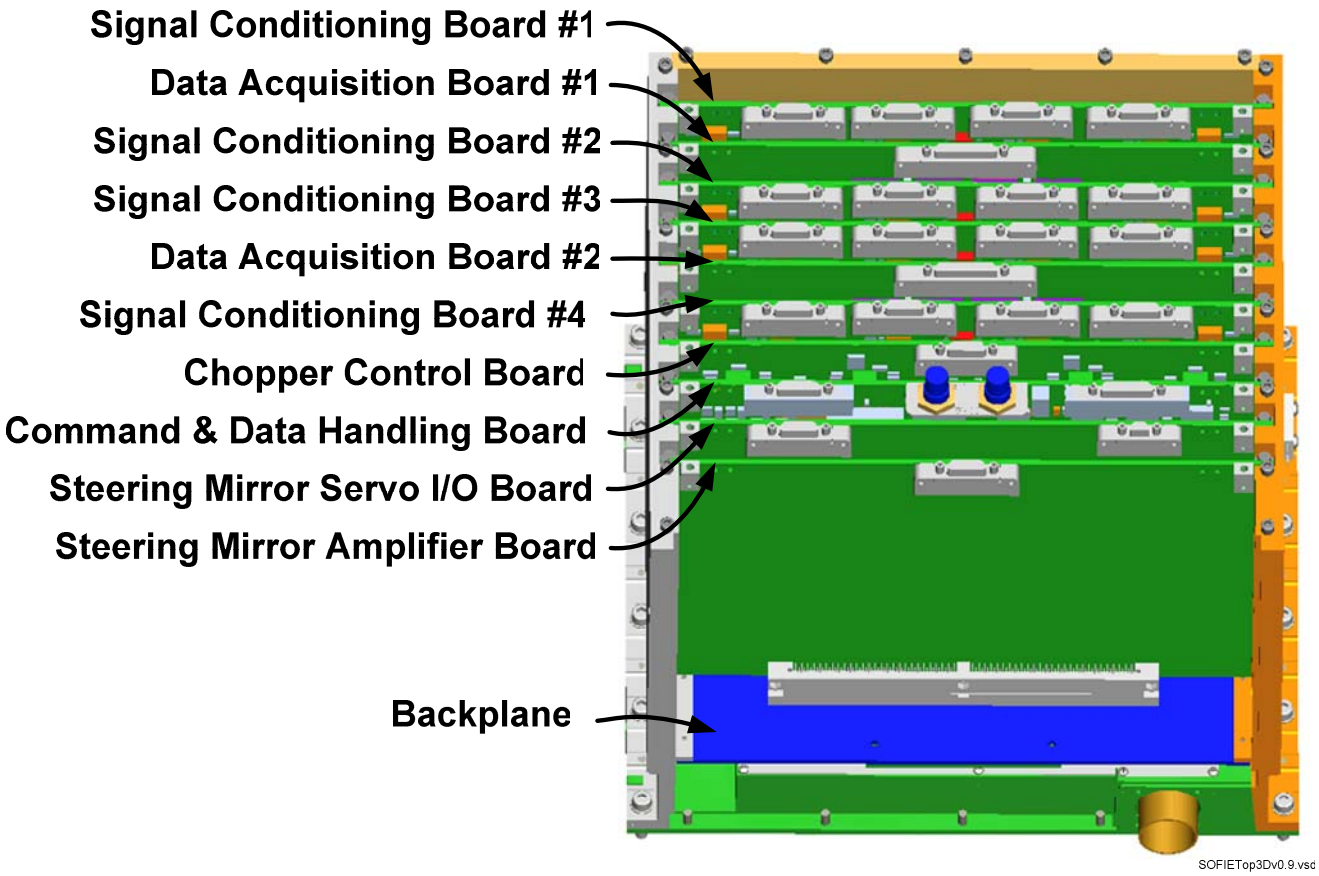


Figure 35 Instrument Unit PC Board Position

6.4 Electronics Unit Printed Circuit Board Definition

The specification for the Electronics Unit Printed Circuit Boards is shown in Figure 36. The locations for the top connectors are different for each type of board. The locations for the top connectors are shown in Figure 37.

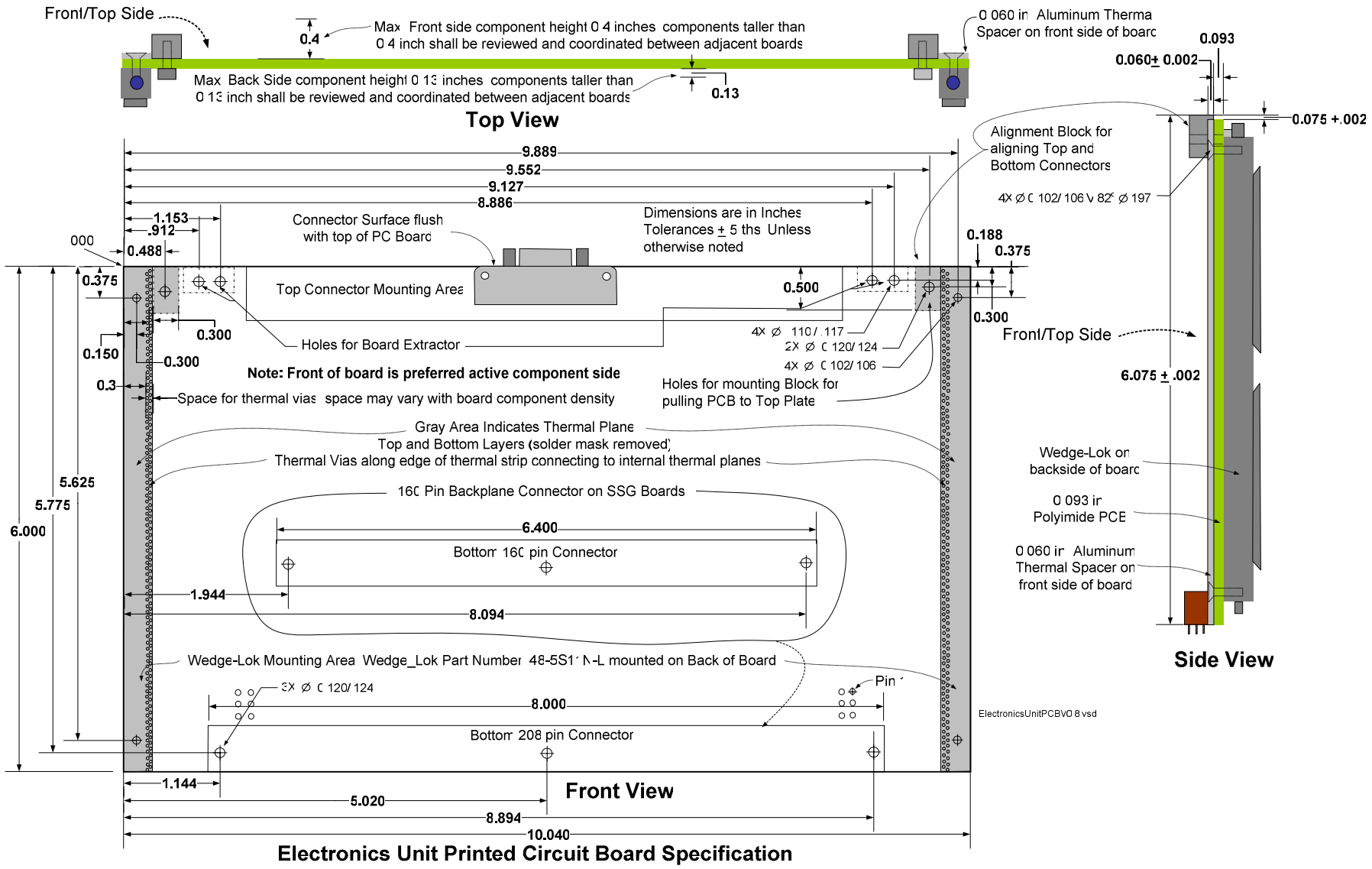
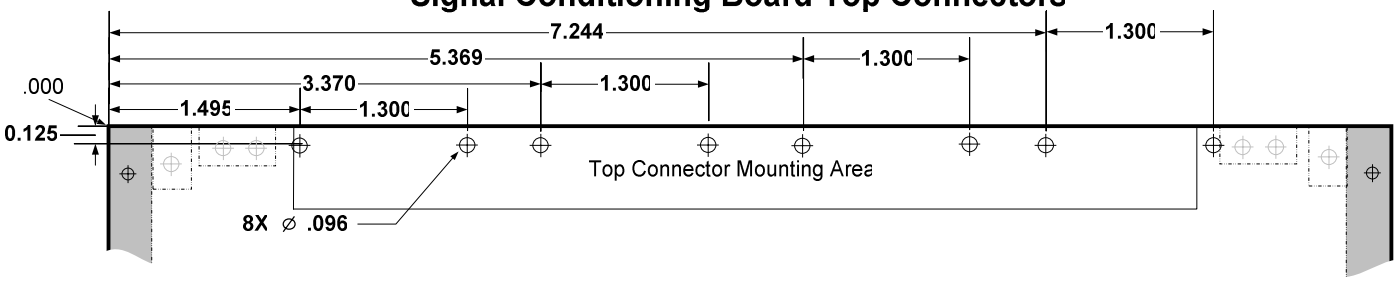
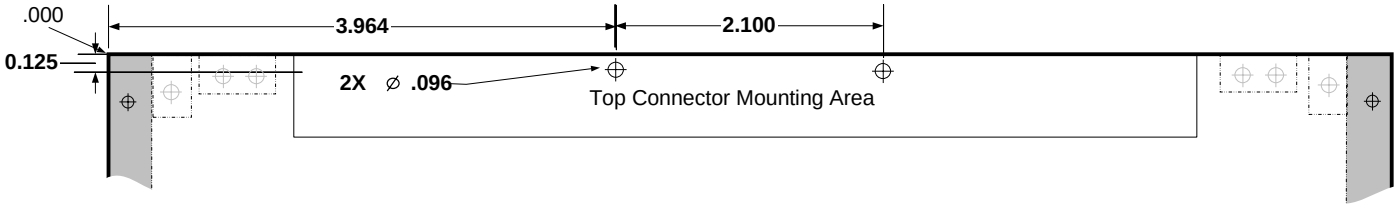


Figure 36 Electronics Unit PCB Specification

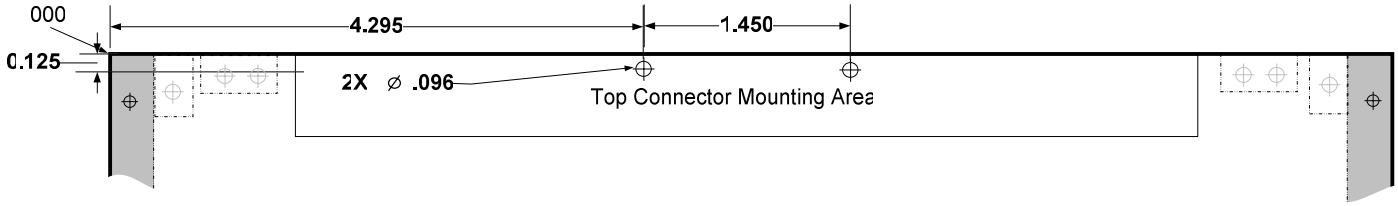
Signal Conditioning Board Top Connectors



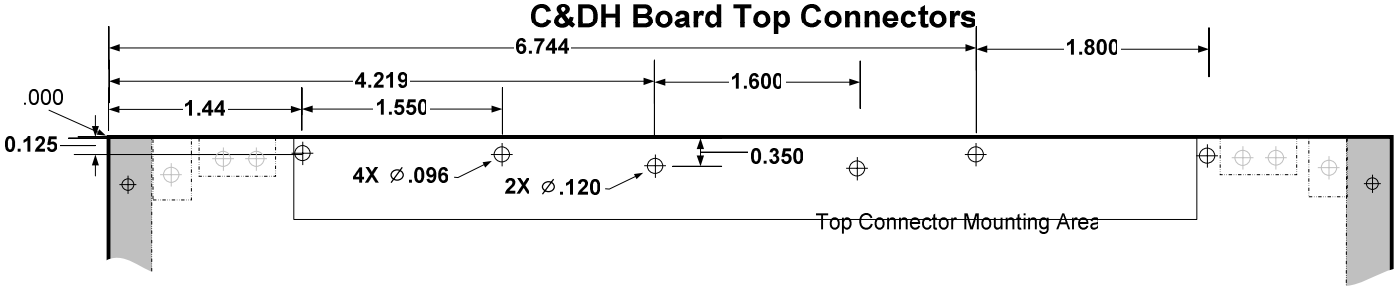
Data Acquisition Board Top Connectors



Chopper Board Top Connectors



C&DH Board Top Connectors



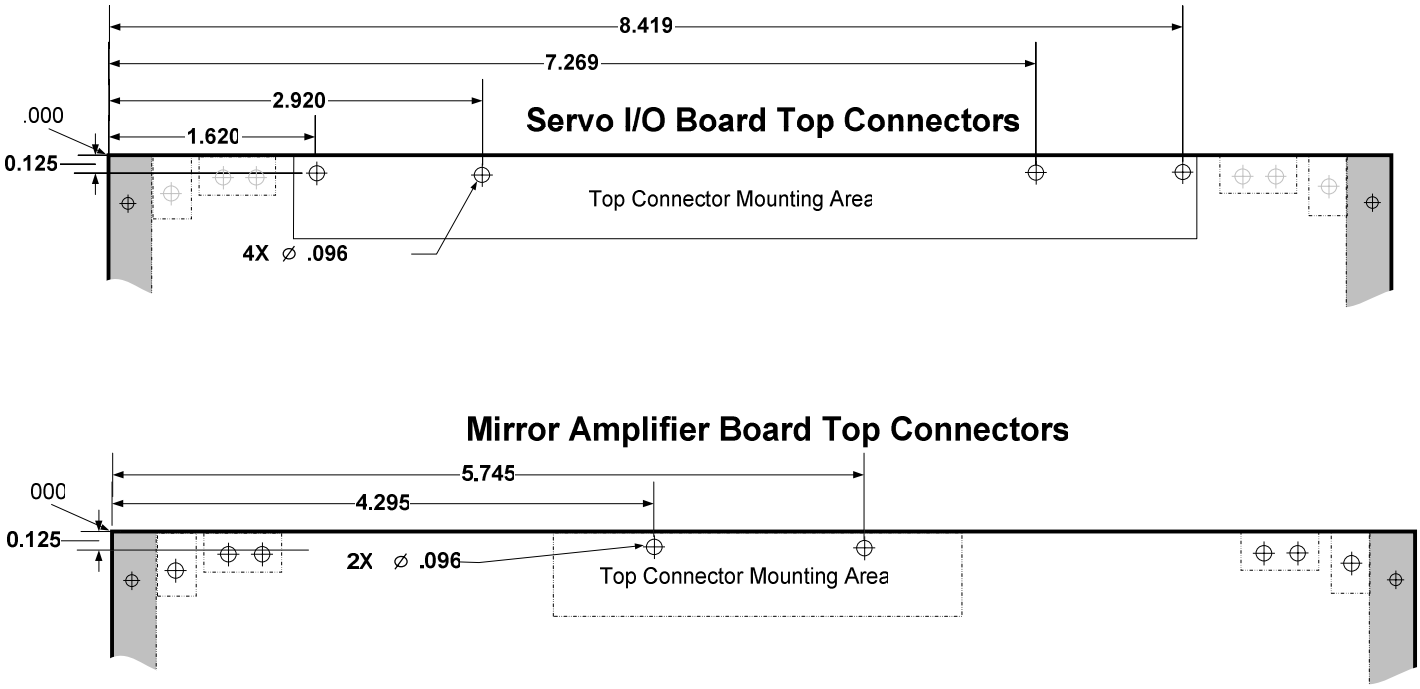


Figure 37 Electronics Unit Top Connectors Locations

6.5 Electronics Unit PCB Top Connector Definitions

This section defines the connectors on the top of the Electronics Unit PCBs and the signals in each connector. Figure 38 shows the top connector locations and specifies part numbers for the connectors. Figure 39 through Figure 43 show the mounting of the top connectors and the analysis for determining the gap between the board bottom connector and the Back Plane connector. An alignment fixture will be used to provide the proper gap during manufacturing. Figure 44 and Figure 45 show the signals on each of the top connectors. The detailed pin assignments for the signals in each connector are specified in Section **Error! Reference source not found.**

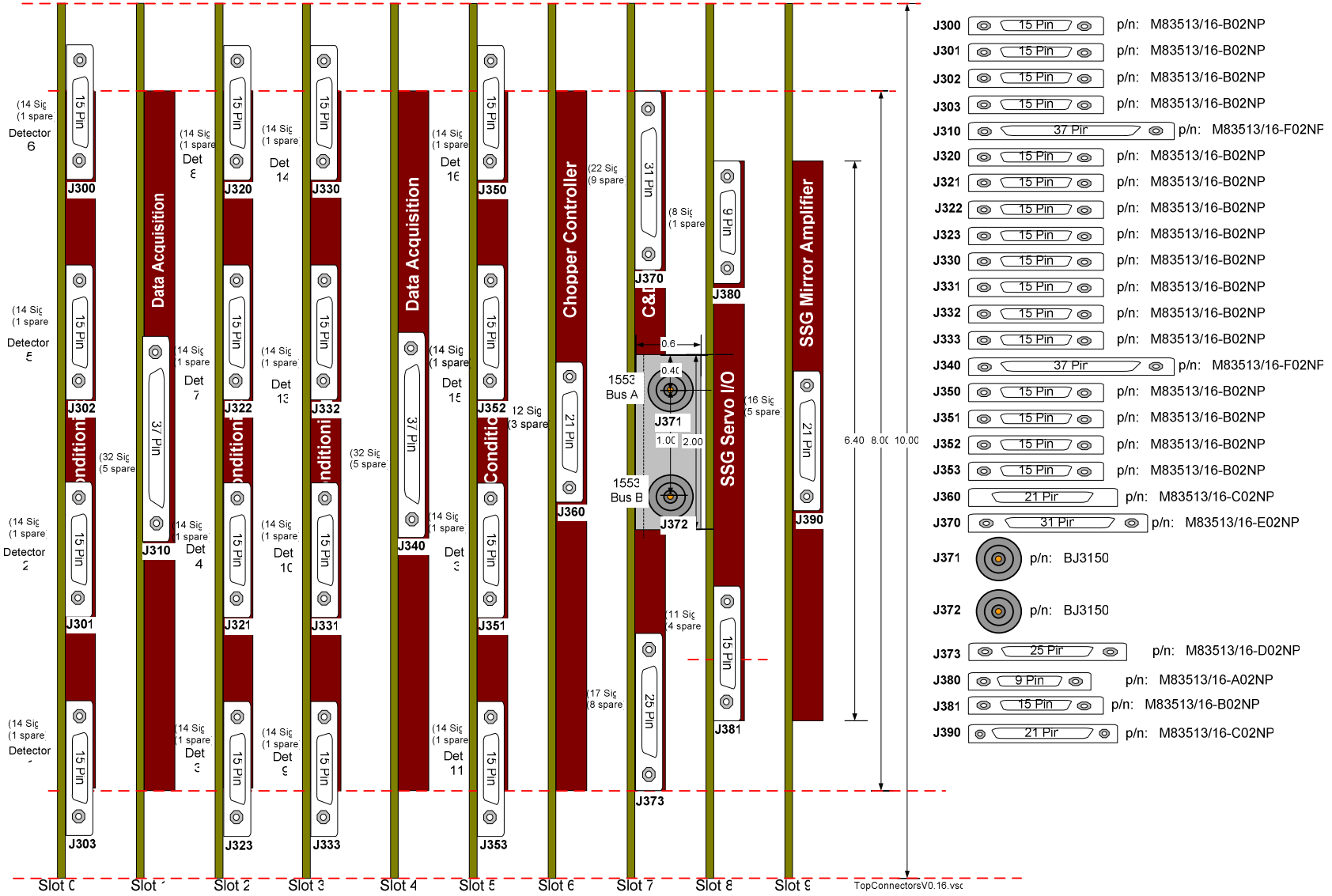
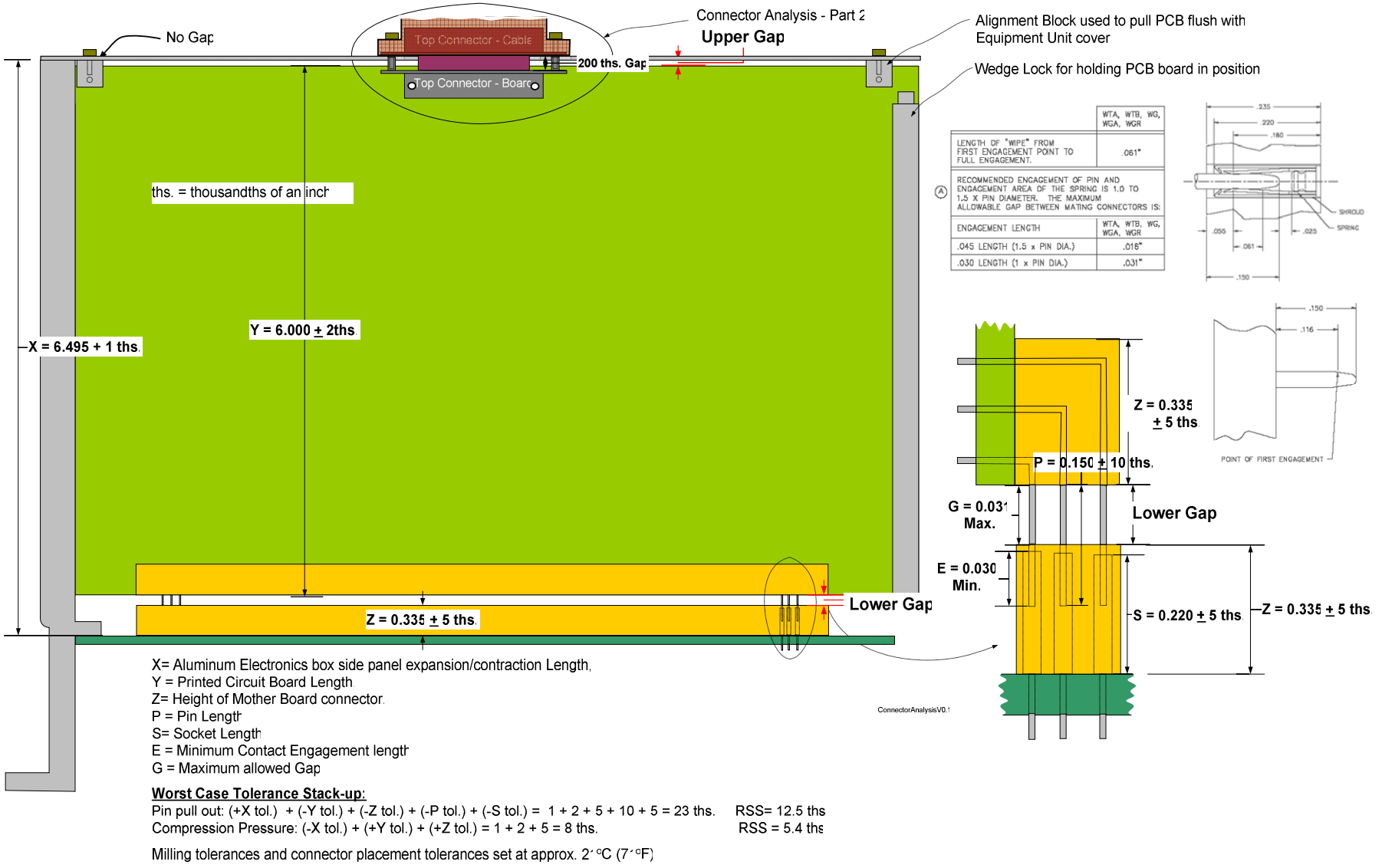


Figure 38 Electronics Unit Top Connectors Placement and Part Numbers



X= Aluminum Electronics box side panel expansion/contraction Length.
Y = Printed Circuit Board Length
Z= Height of Mother Board connector.
P = Pin Length
S= Socket Length
E = Minimum Contact Engagement length
G = Maximum allowed Gap

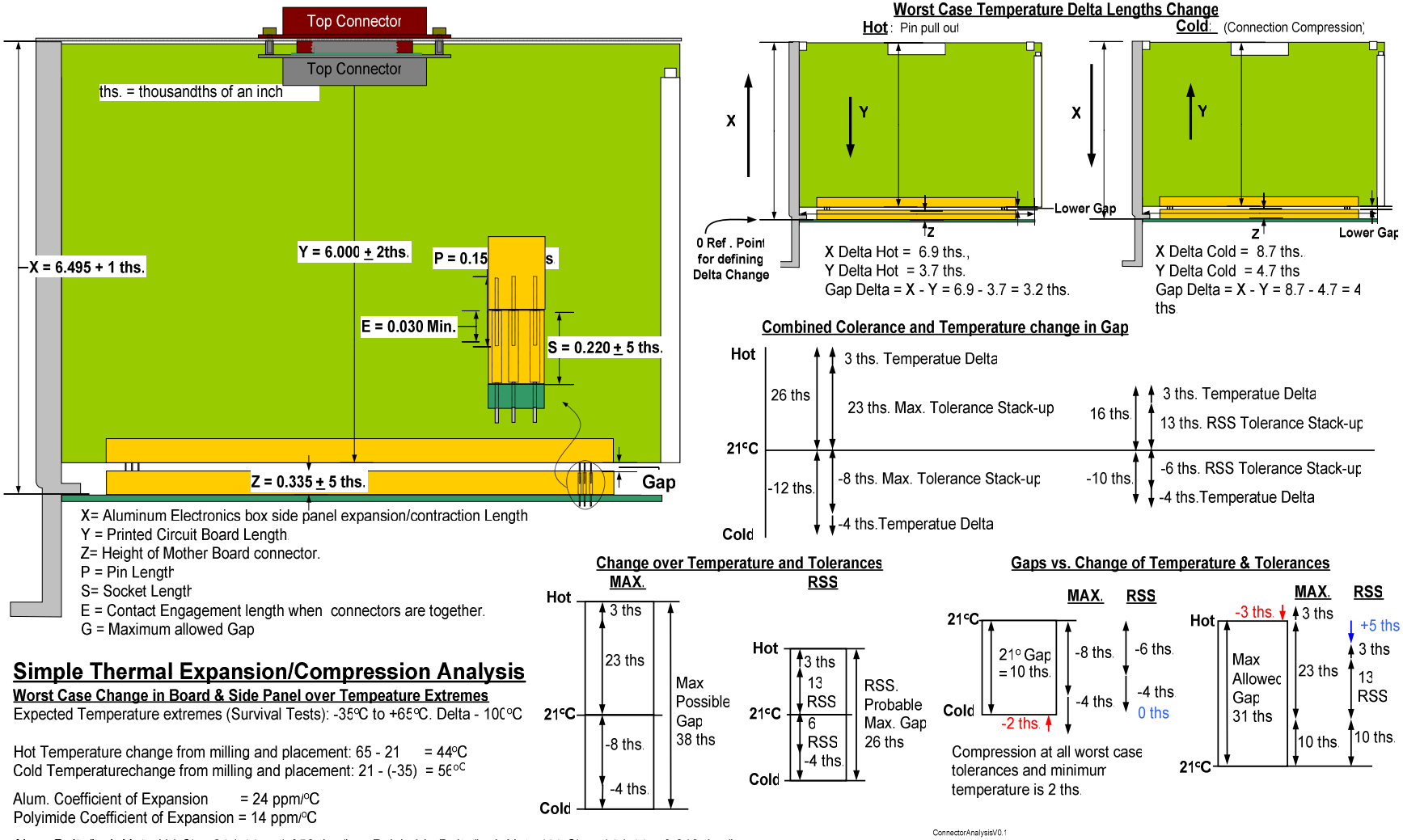
Worst Case Tolerance Stack-up:

Pin pull out: (+X tol.) + (-Y tol.) + (-Z tol.) + (-P tol.) + (-S tol.) = 1 + 2 + 5 + 10 + 5 = 23 ths. RSS= 12.5 ths

Compression Pressure: (-X tol.) + (+Y tol.) + (+Z tol.) = 1 + 2 + 5 = 8 ths. RSS = 5.4 ths

Milling tolerances and connector placement tolerances set at approx. 2´°C (7´°F)

Figure 39 Connector Mounting and Gap Calculations - Part 1



Simple Thermal Expansion/Compression Analysis

Worst Case Change in Board & Side Panel over Tempeature Extremes

Expected Temperature extremes (Survival Tests): -35°C to +65°C. Delta - 100°C

Hot Temperature change from milling and placement: 65 - 21 = 44°C
Cold Temperaturechange from milling and placement: 21 - (-35) = 56°C

Alum. Coefficient of Expansion = 24 ppm/°C
Polyimide Coefficient of Expansion = 14 ppm/°C

Alum. Delta/inch Hot (44°C) = 24 * 44 = 1.056 ths./in., Polyimide Delta/inch Hot (44°C) = 14 * 44 = 0.616 ths./in.
Alum. Delta/inch Cold (56°C) = 24 * 56 = 1.344 ths./in., Polyimide Delta/inch Cold (56°C) = 14 * 56 = 0.784 ths./in.

Alum. Length = 6.495in., PCB Length = 6.000 in

Alum. Delta Hot = 6.495 * 1.056 =6.9 ths., PCB Delta Hot = 6.0 * 0.616 = 3.7 ths. PCB Delta Hot = 10.0 * 0.616 = 6.16 ths.
Alum. Delta Cold = 6.495 * 1.344 = 8.7 ths., PCB Delta Cold = 6.0 * 0.784 = 4.7 ths. PCB Delta Cold = 10.0 * 0.784 = 7.84 ths

Figure 40 Connector Mounting and Gap Calculations - Part 2

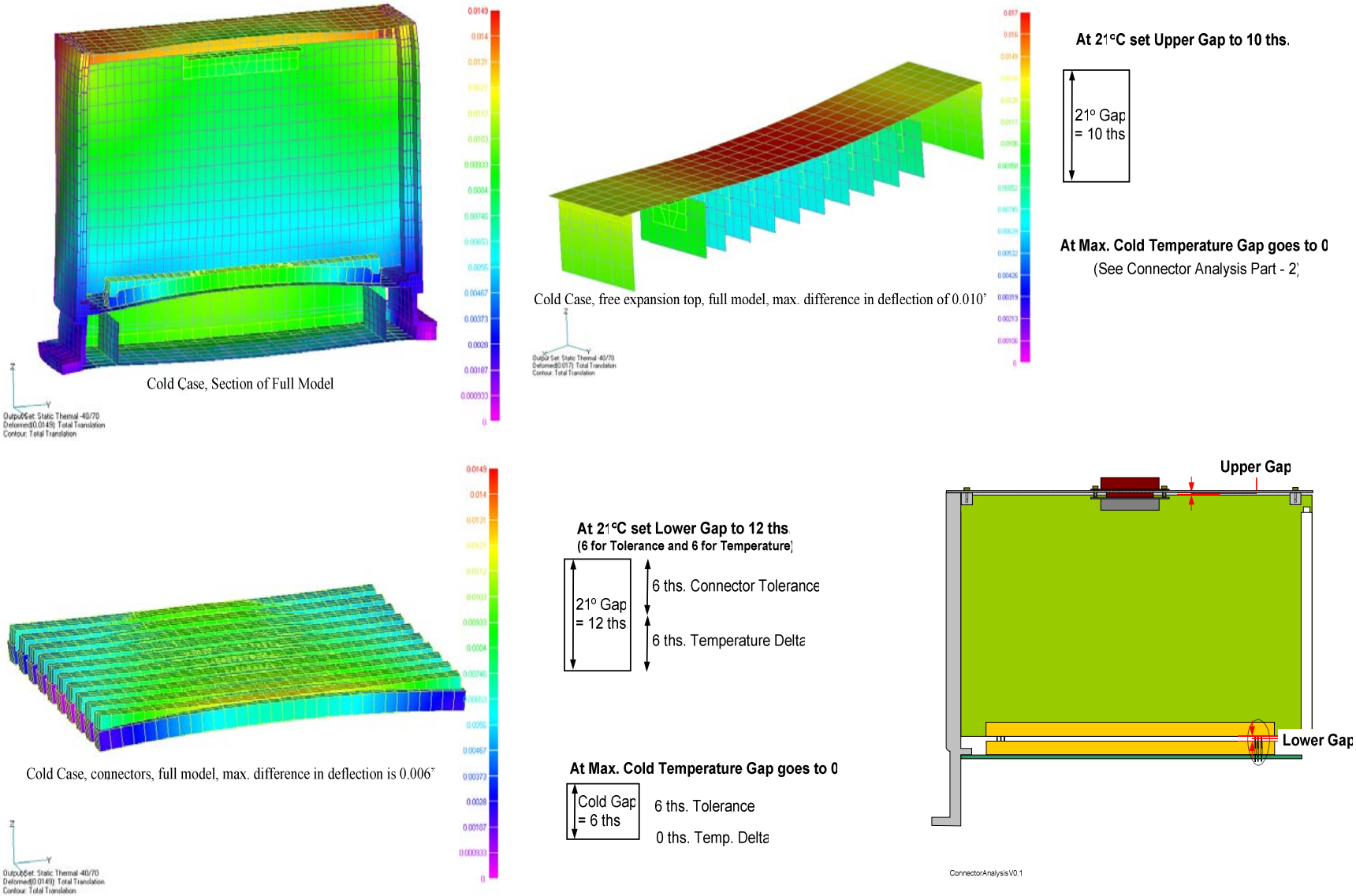


Figure 41 Connector Mounting and Gap Calculations - Part 3

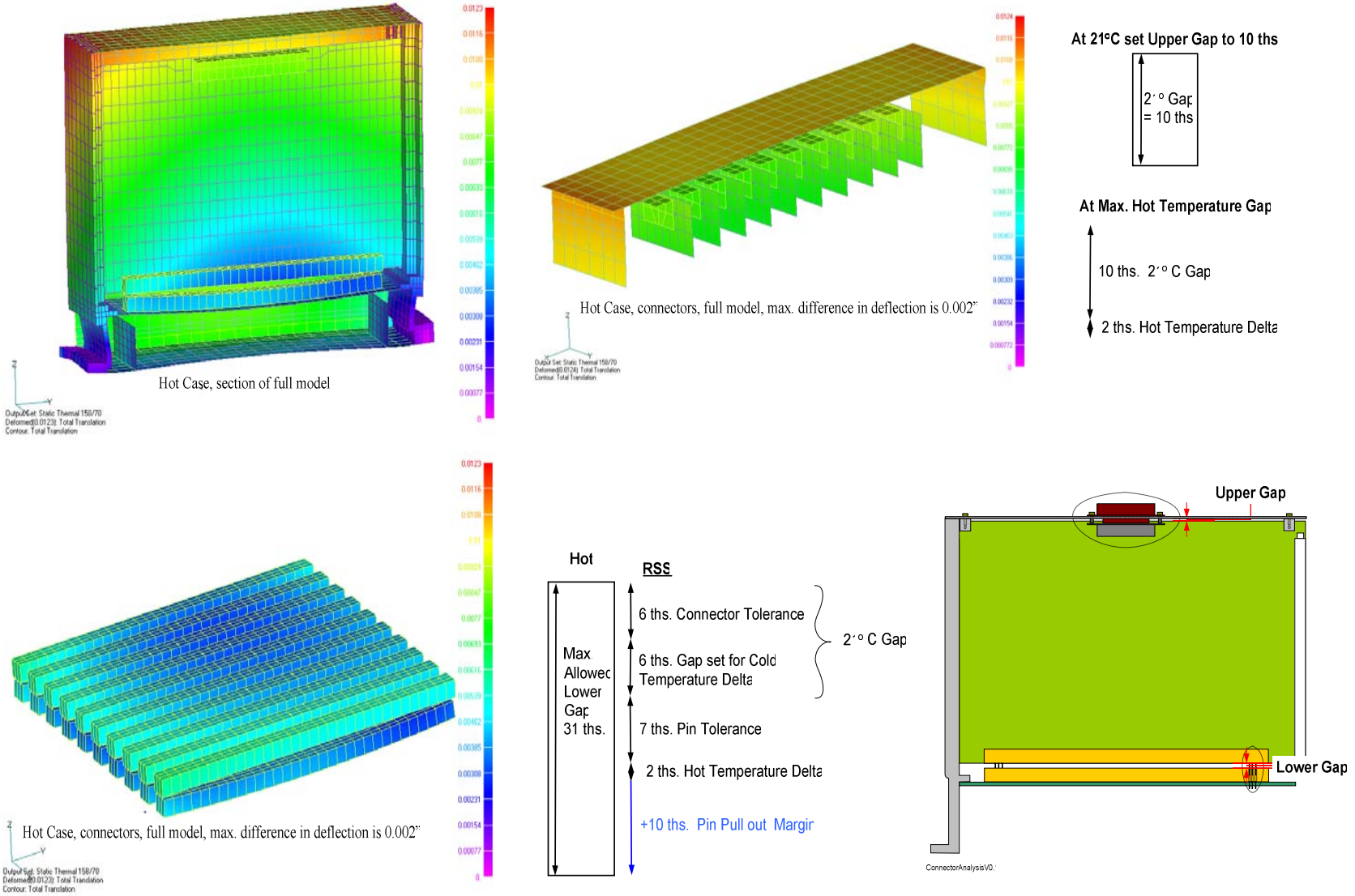


Figure 42 Connector Mounting and Gap Calculations - Part 4

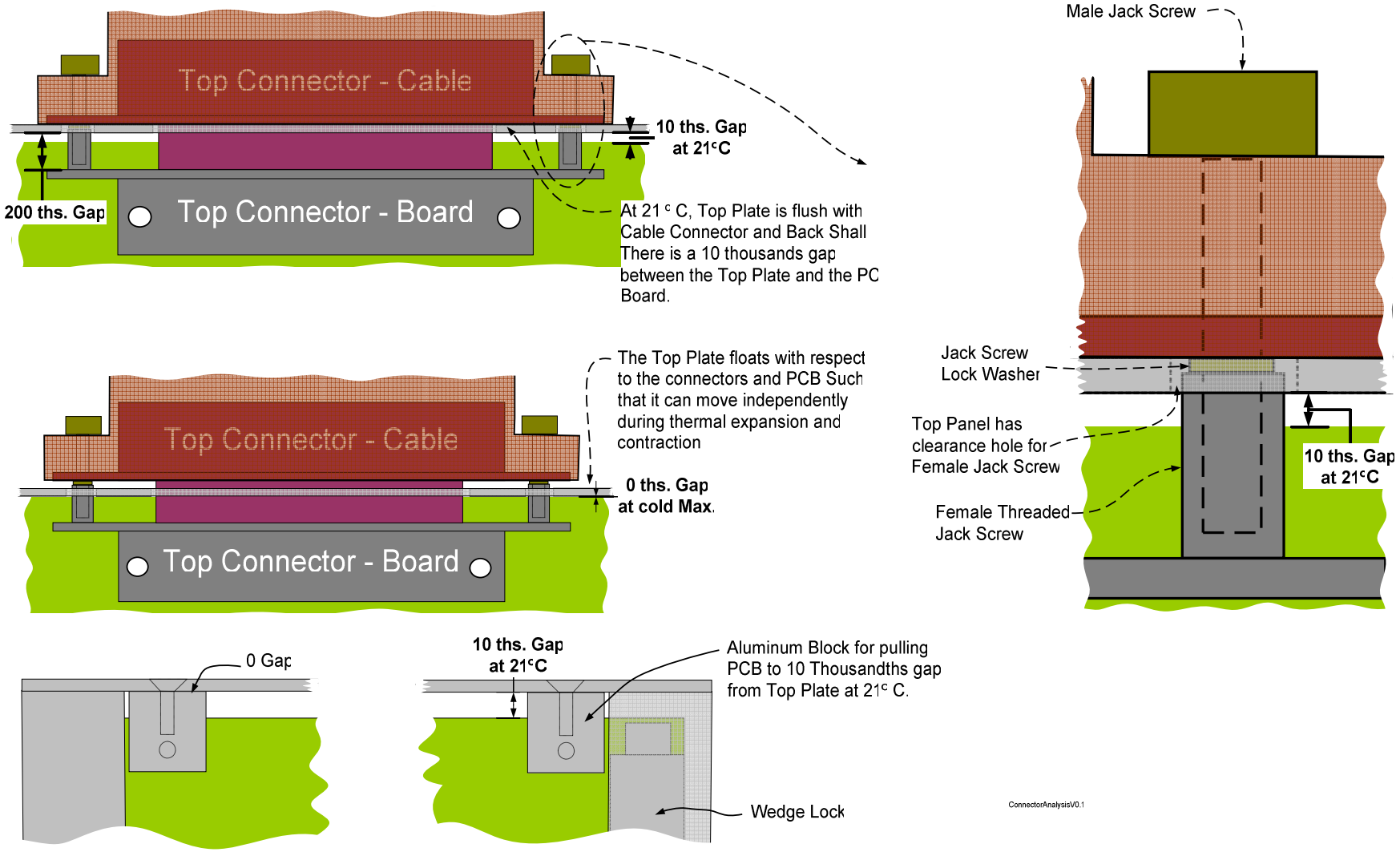


Figure 43 Connector Mounting and Gap Calculations - Part 5

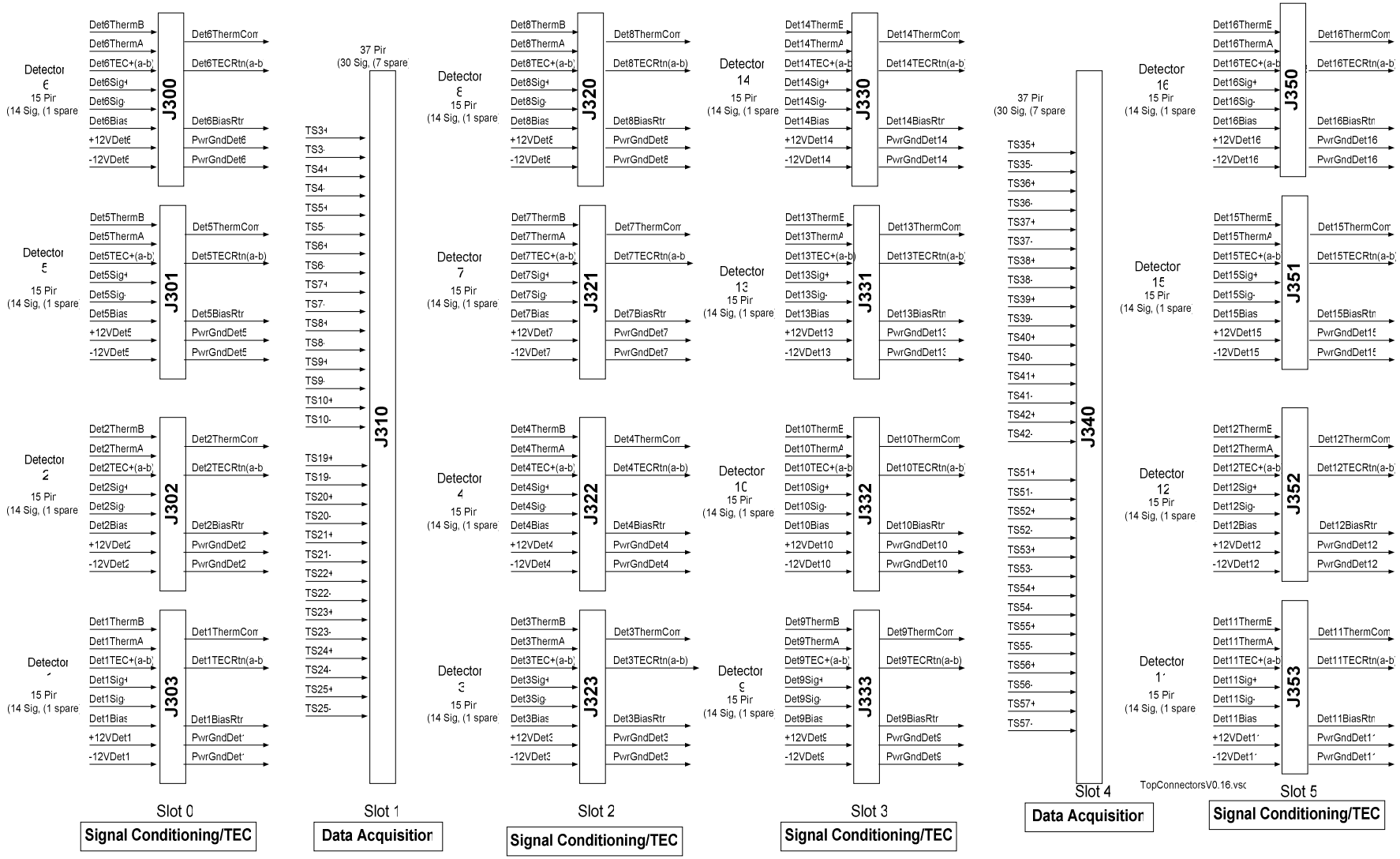


Figure 44 Top Connectors Signals - Part 1

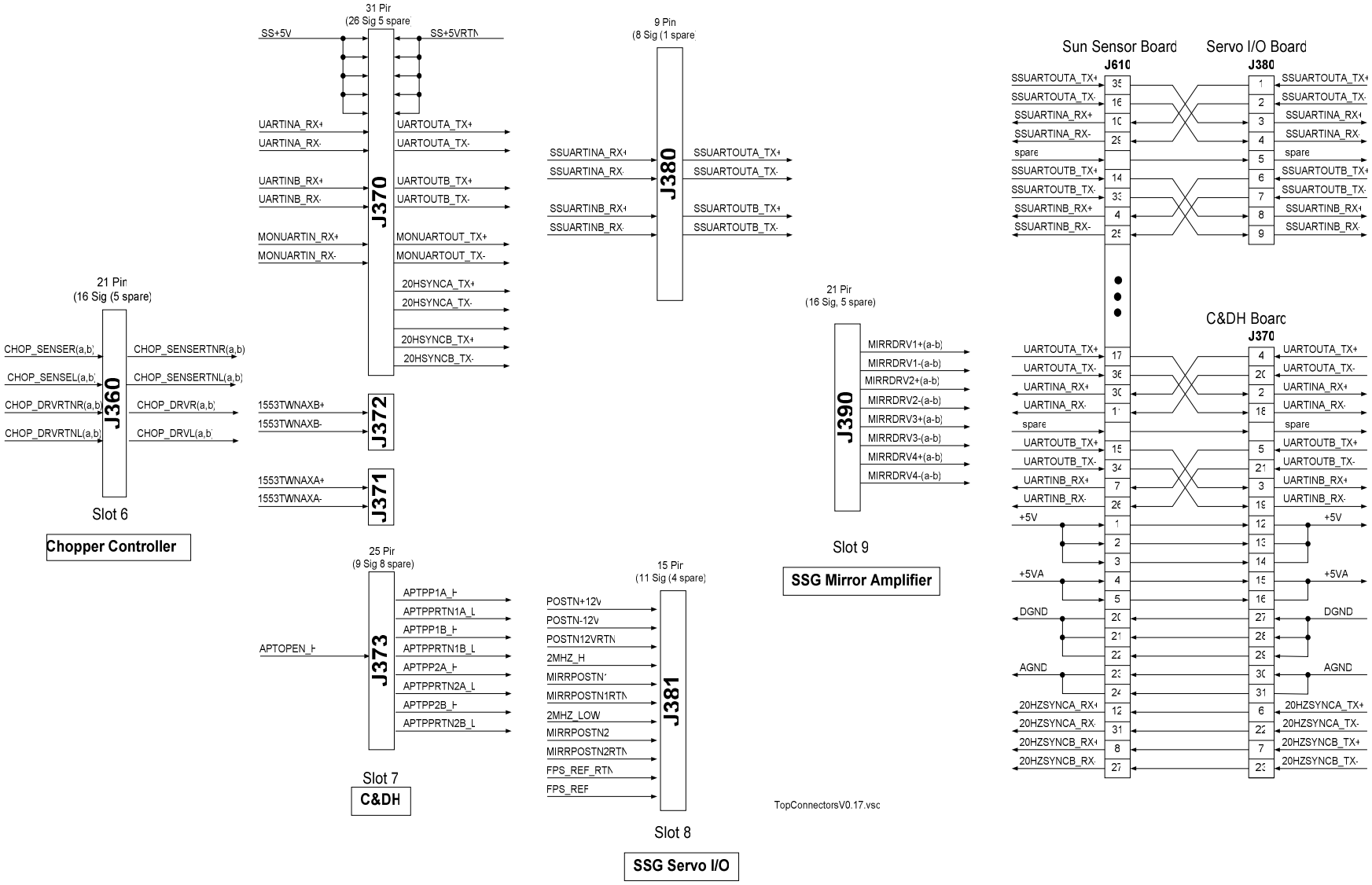


Figure 45 Top Connectors Signals - Part 2

7. SOFIE INSTRUMENT UNIT TO ELECTRONIC UNIT INTERFACE

The SOFIE System Functional Partition shown in Figure 46 provides a high level view of the components within the SOFIE system and the information flowing between them. The functional interfaces (what information flows) between the two major components is described in this section as well as the physical interfaces (signal names, cables, connectors, etc.) that transfer the information.

The detailed interface signals between the SOFIE Instrument Unit and the SOFIE Electronics Unit are shown in Figure 47 and Figure 48. The communication between the Command and Data Handling and the Sun Sensor boards utilizes a RS-422 serial communication link. The communication between the SSG Servo I/O and Sun Sensor boards also utilizes a RS-422 serial interface. The physical interface for these communication paths and the commands used in this communication are defined in section 11.1.1 SOFIE Serial Communication RS-422 Physical Layer Interface Definition.

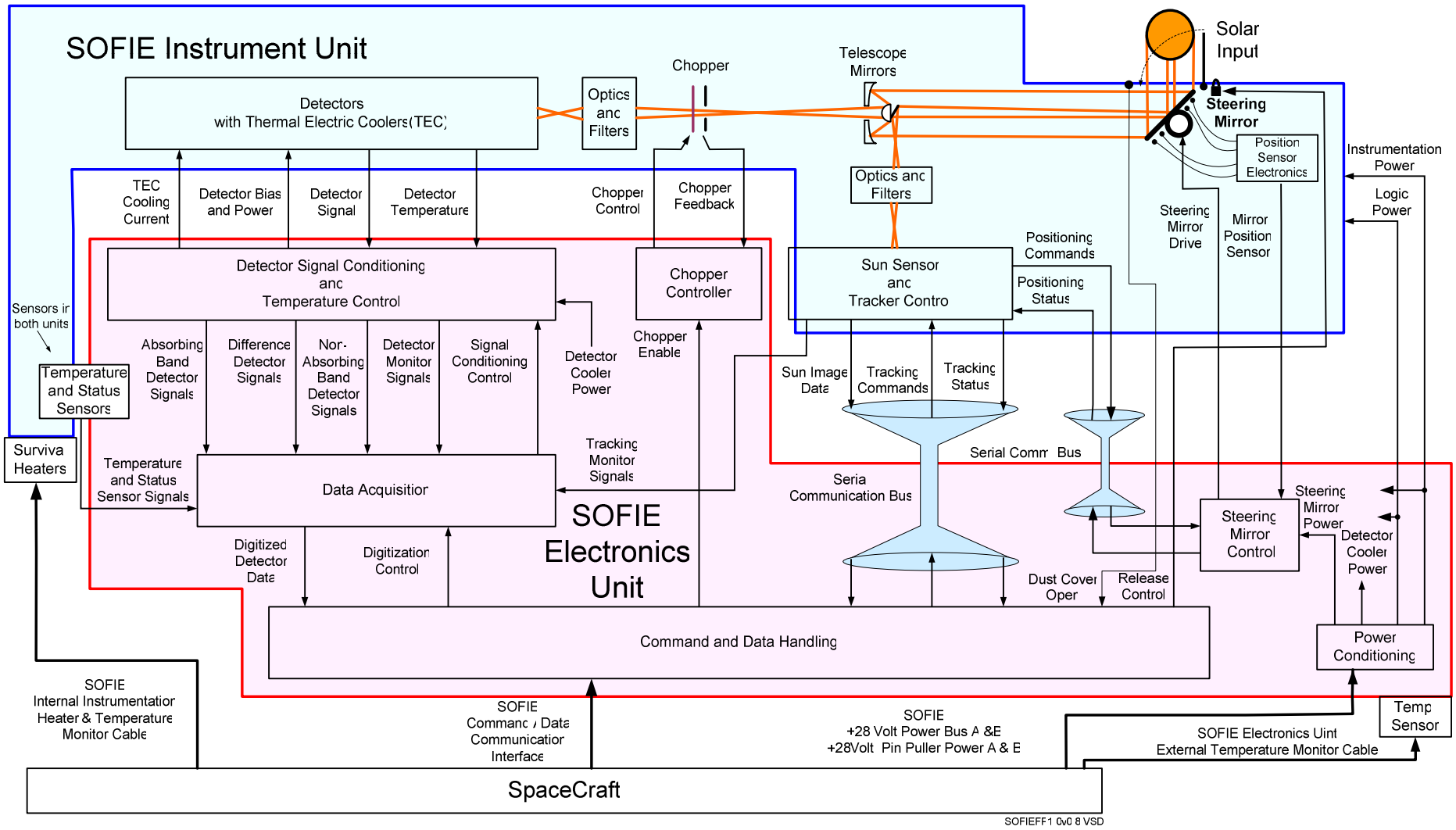


Figure 46 SOFIE System Functional Partition

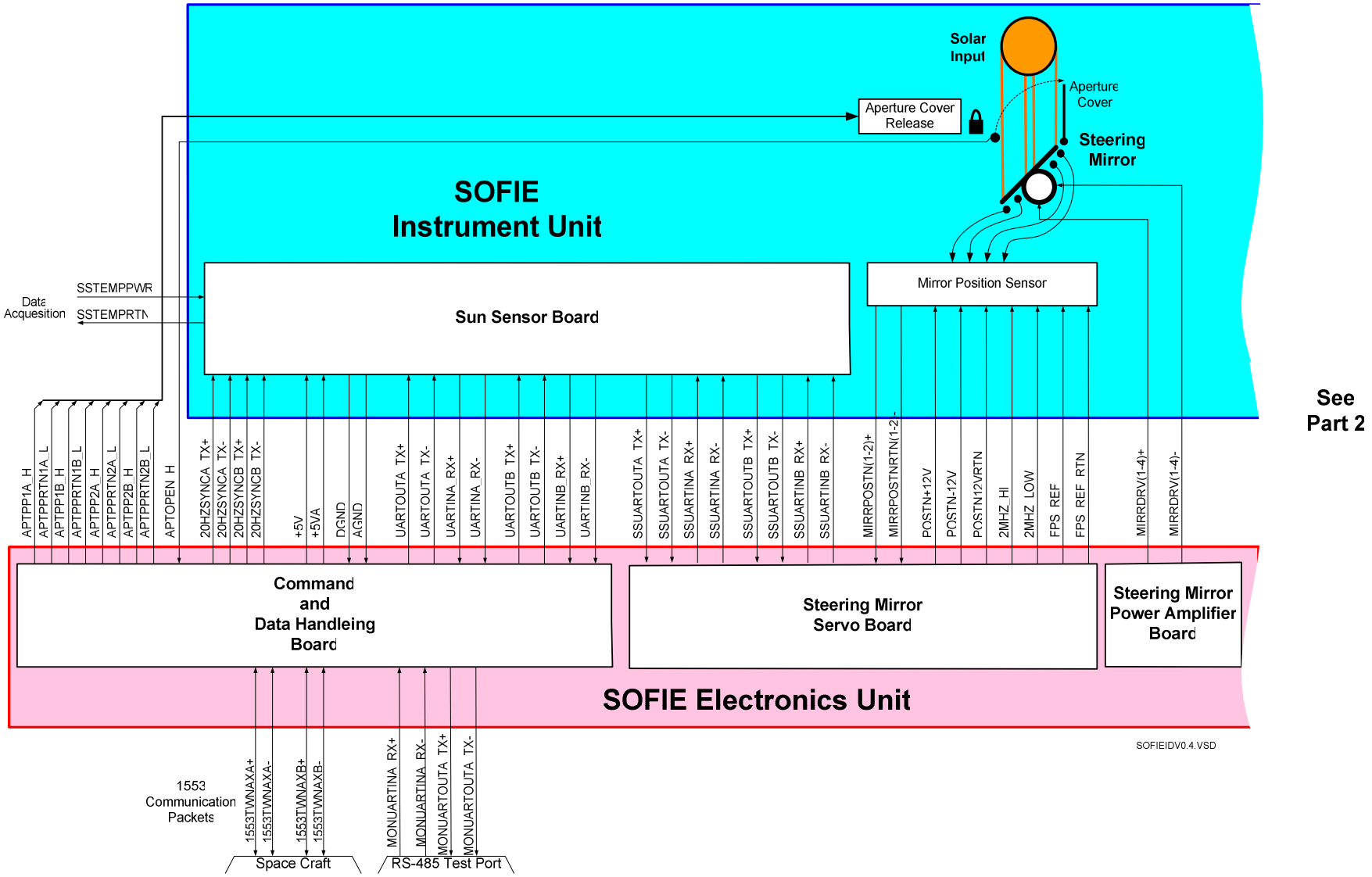


Figure 47 SOFIE Interface Diagram - Part 1

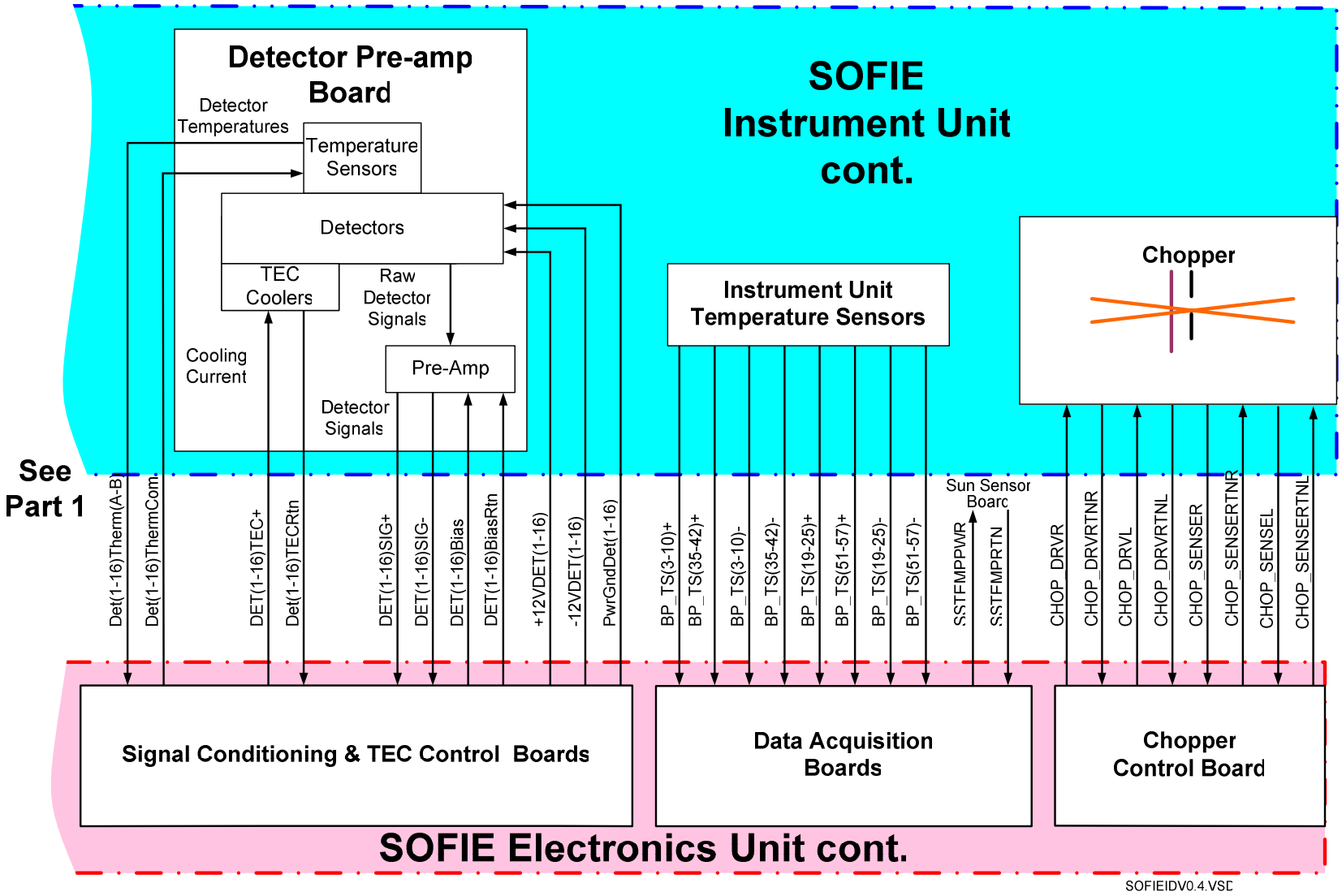


Figure 48 SOFIE Interface Diagram - Part

8. SOFIE INSTRUMENT UNIT INTERNAL INTERFACES

As shown in the SOFIE System Functional Partition in Figure 49, there is no direct electrical communication between the functional elements within the Instrument Unit. Each sub-system within the Instrument Unit communicates with its corresponding section in the SOFIE Electronics Box. All of these interfaces have been described in the previous section. The following sections describe the interfaces between the boards within the Electronics Unit.

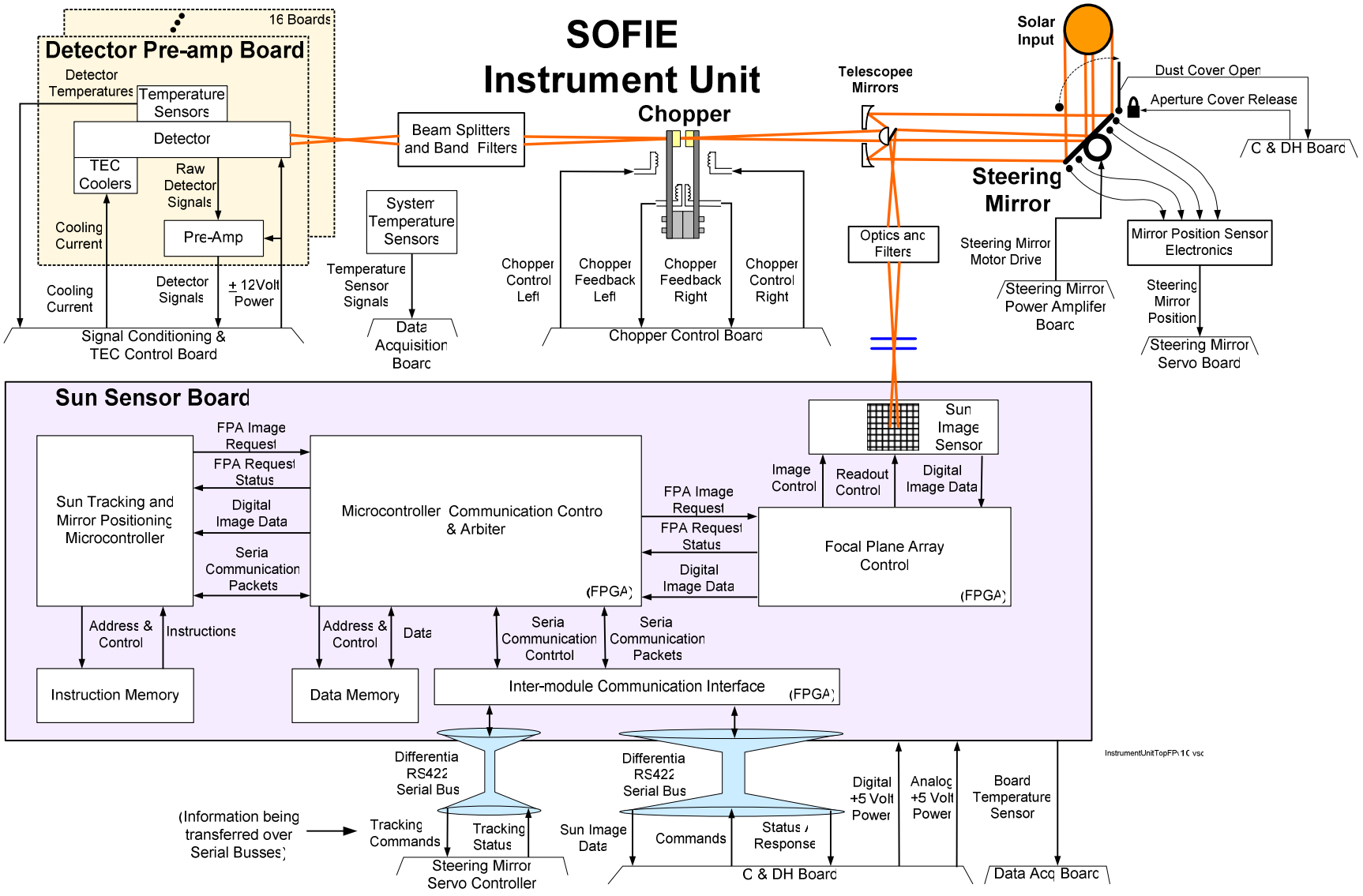


Figure 49 Instrument Unit Top Level Functional Partition

9. ELECTRONICS UNIT INTERNAL FUNCTIONAL INTERFACES

The Electronics Unit Top Level Functional Partition is shown Figure 50. This drawing shows the functions within the Electronics Unit as they are partitioned into Printed Circuit Boards (PCB). It also provides a high level view of the information going between the different boards.

The SOFIE Electronics Unit is partitioned into the following physical components:

- Signal Conditioning/TEC Controller Board (4 boards)
- Data Acquisition Board (2 boards)
- Chopper Board
- C&DH Board
- SSG Servo I/O Board
- SSG Mirror Amplifier Board
- Back Plane Board
- Power Conditioning Input/Slow Start Board
- Power Conditioning Output Board

Theses boards and the detailed Electronics Unit interface signals are shown on the Electronics Unit Interface Diagrams shown in Figure 51 and Figure 52.

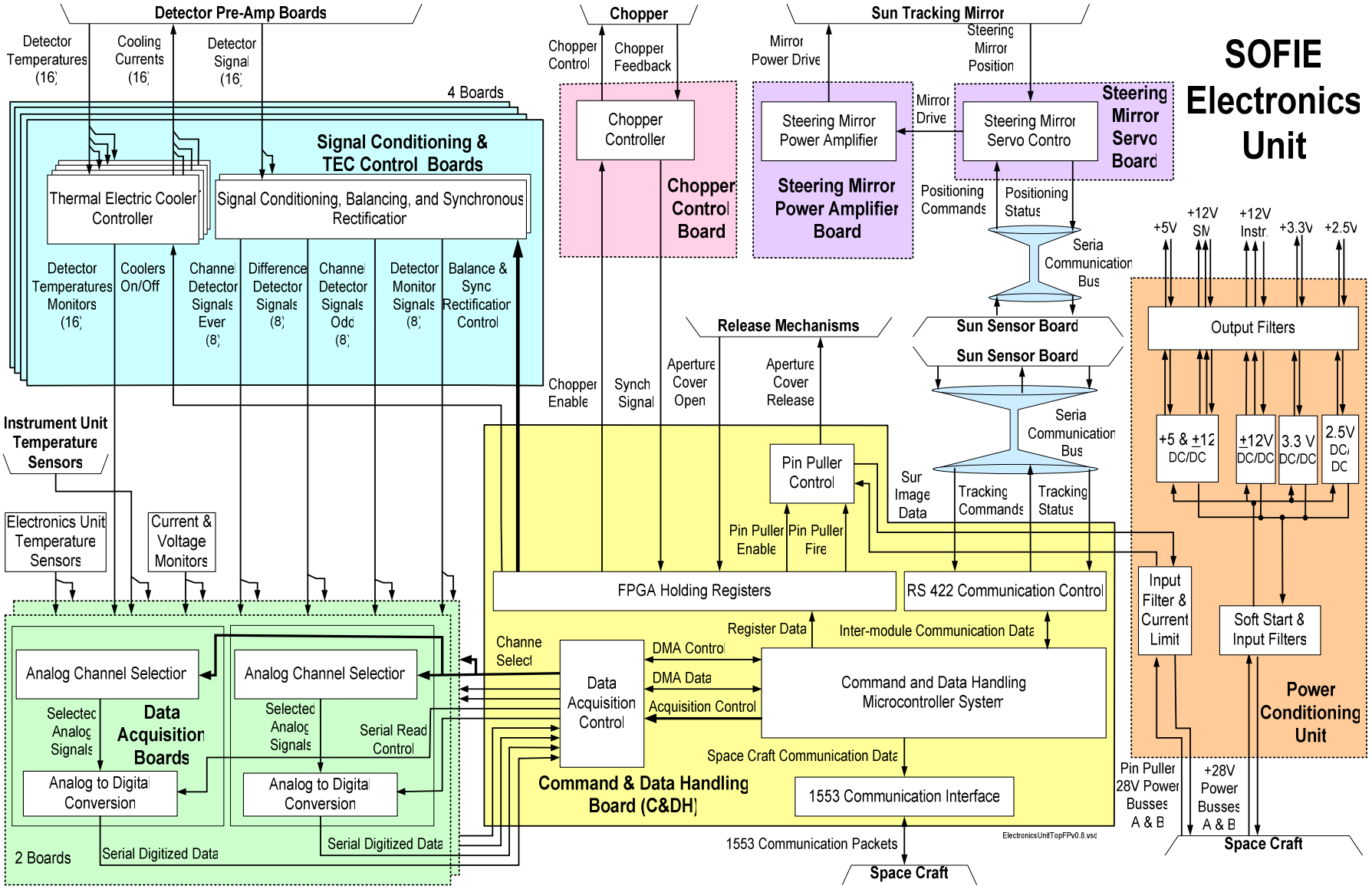


Figure 50 Electronics Unit Detailed Functional Partition

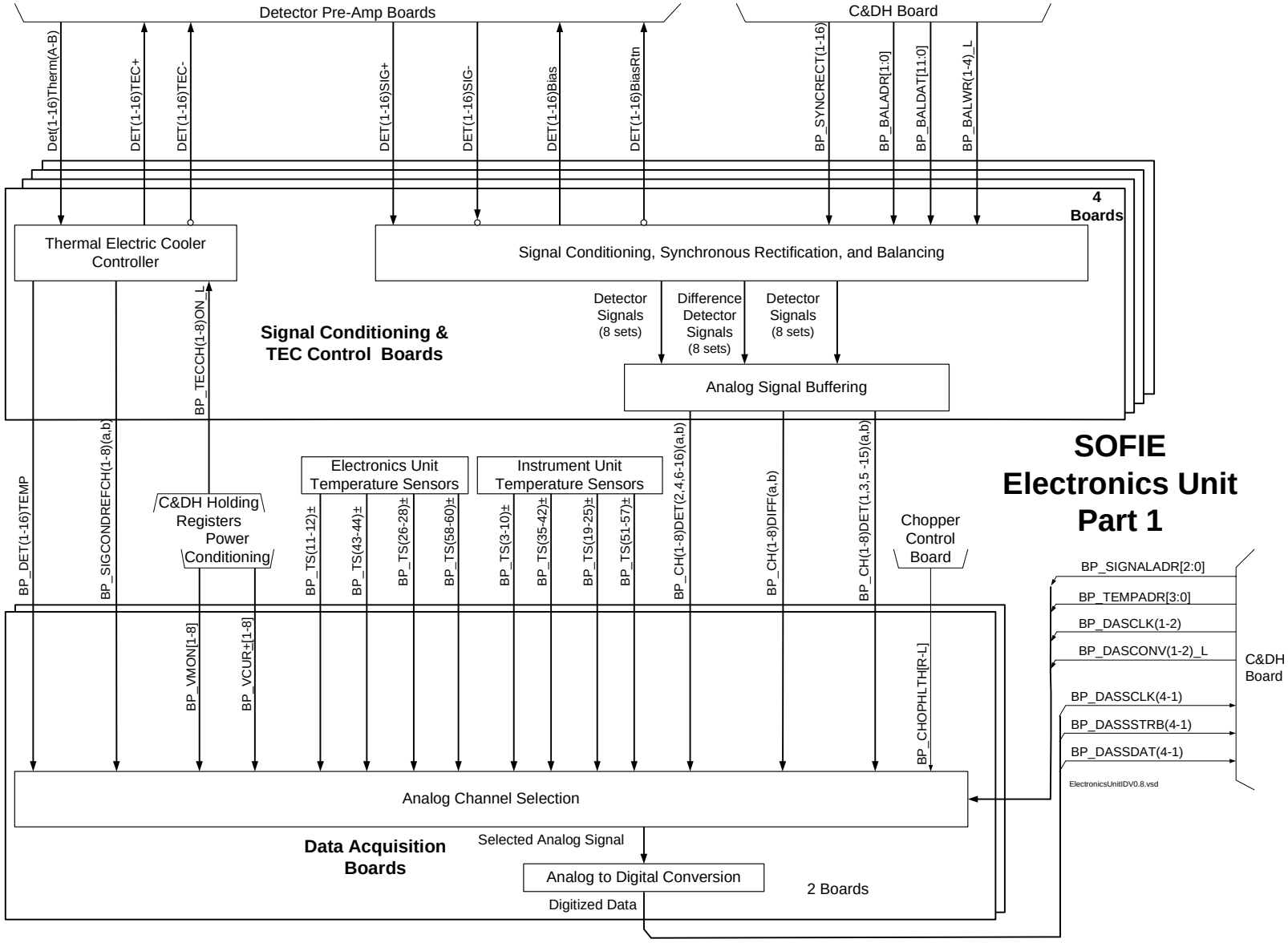


Figure 51 Electronics Unit Interface Diagram - Part 1

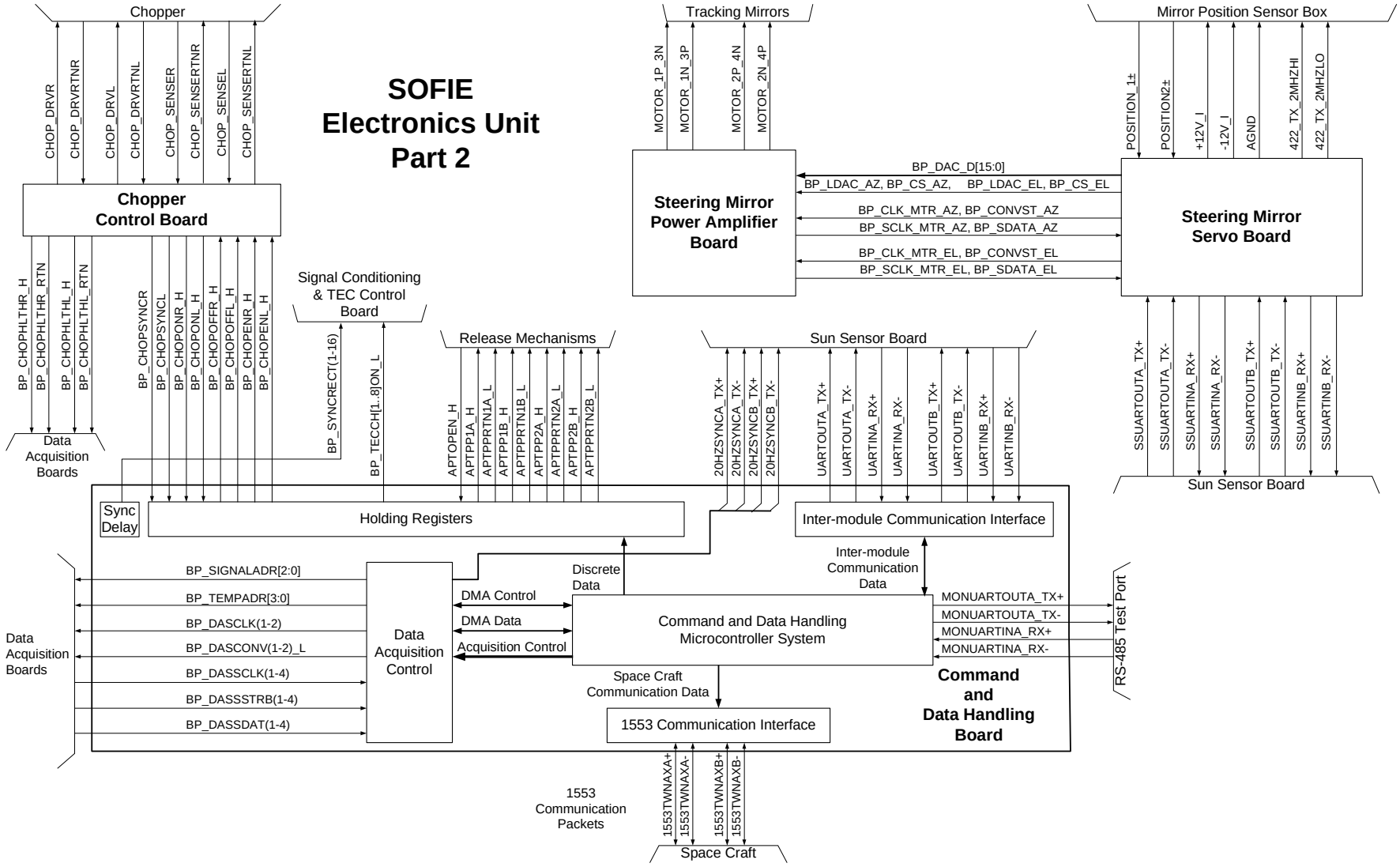


Figure 52 Electronics Unit Interface Diagram - Part 2

10. FPGA INTERFACES

10.1 Command and Data Handling FPGA Partitioning

The Command and Data Handling (C&DH) board contains two FPGAs that perform its interface and control functions. The two FPGAs are the Arbiter FPGA and the Data Acquisition FPGA. The top level block diagram of the C&DH FPGA partitioning is shown in Figure 53. The detailed FPGA Interface signals for these FPGAs are shown in Figure 54 and Figure 55. The Timing Analysis for the FPGA interface signals is included in Appendix A.

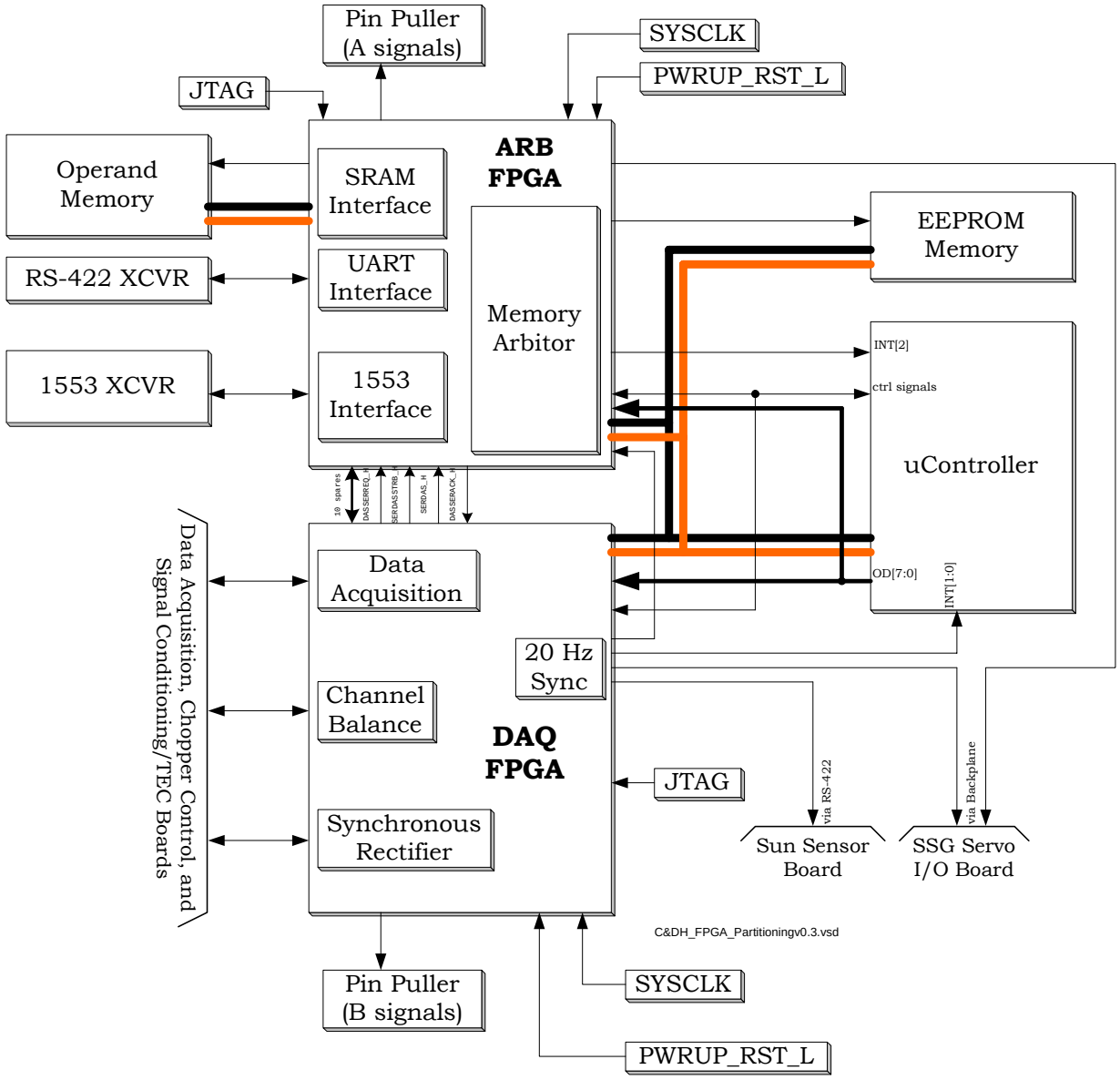


Figure 53 C&DH FPGA Partitioning

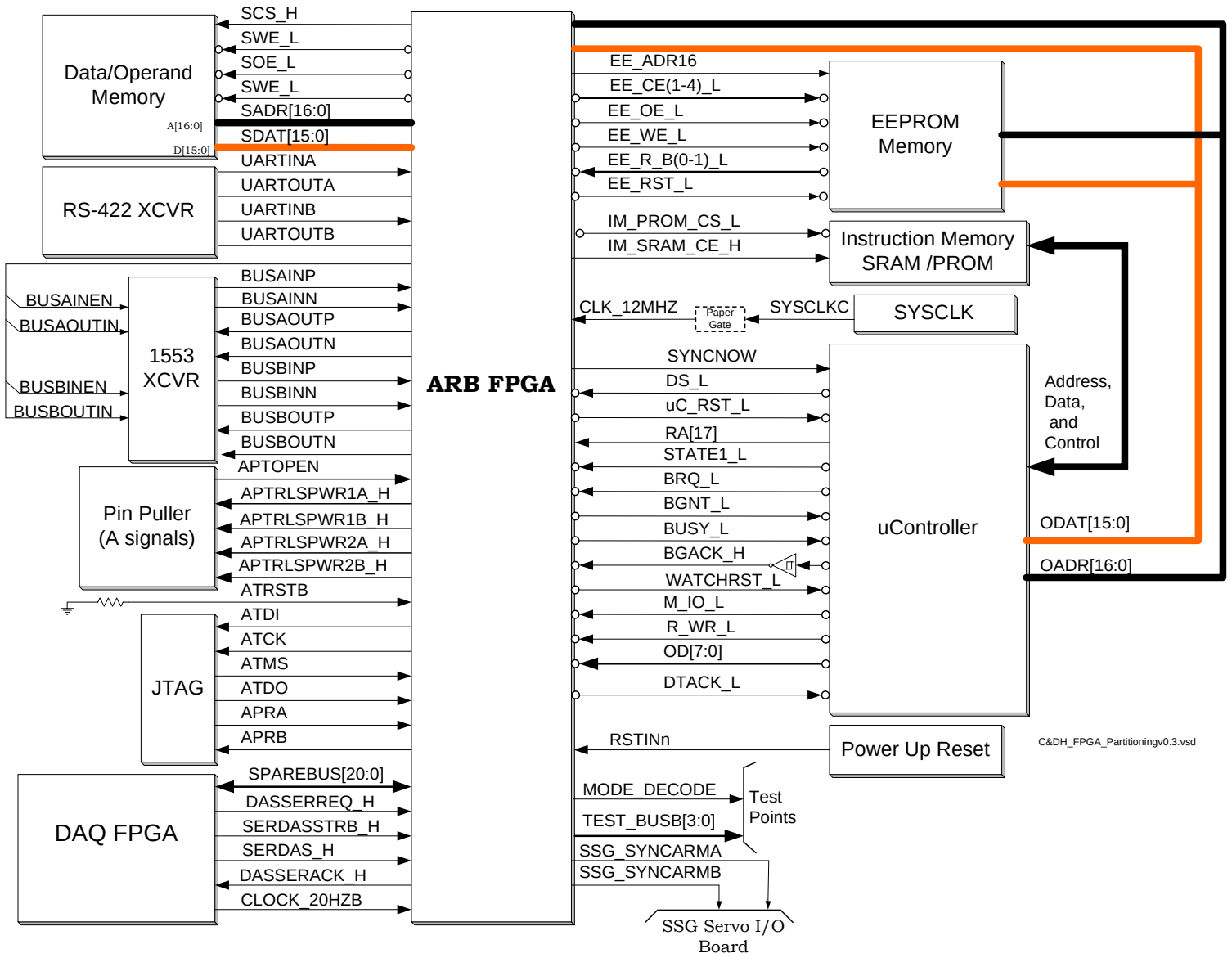


Figure 54 Arbiter FPGA Interface Diagram

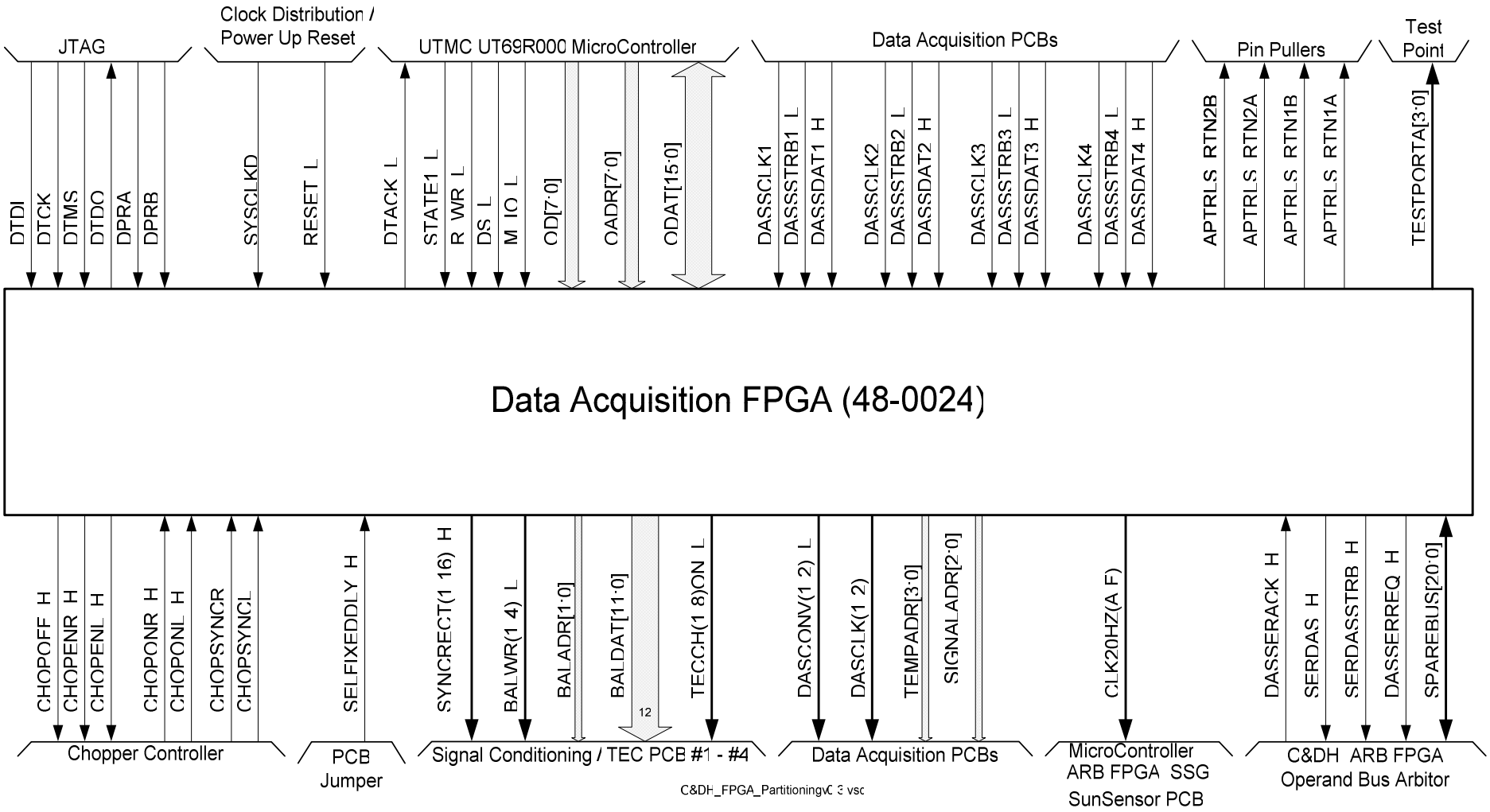


Figure 55 Data Acquisition FPGA Interface Diagram

10.2 Sun Sensor FPGA Partitioning

The Sun Sensor board contains one FPGA that performs its interface and control functions. The FPGA interface signals for the Sun Sensor FPGA are shown in Figure 56. The Timing Analysis for the FPGA interface signals is included in Appendix A.

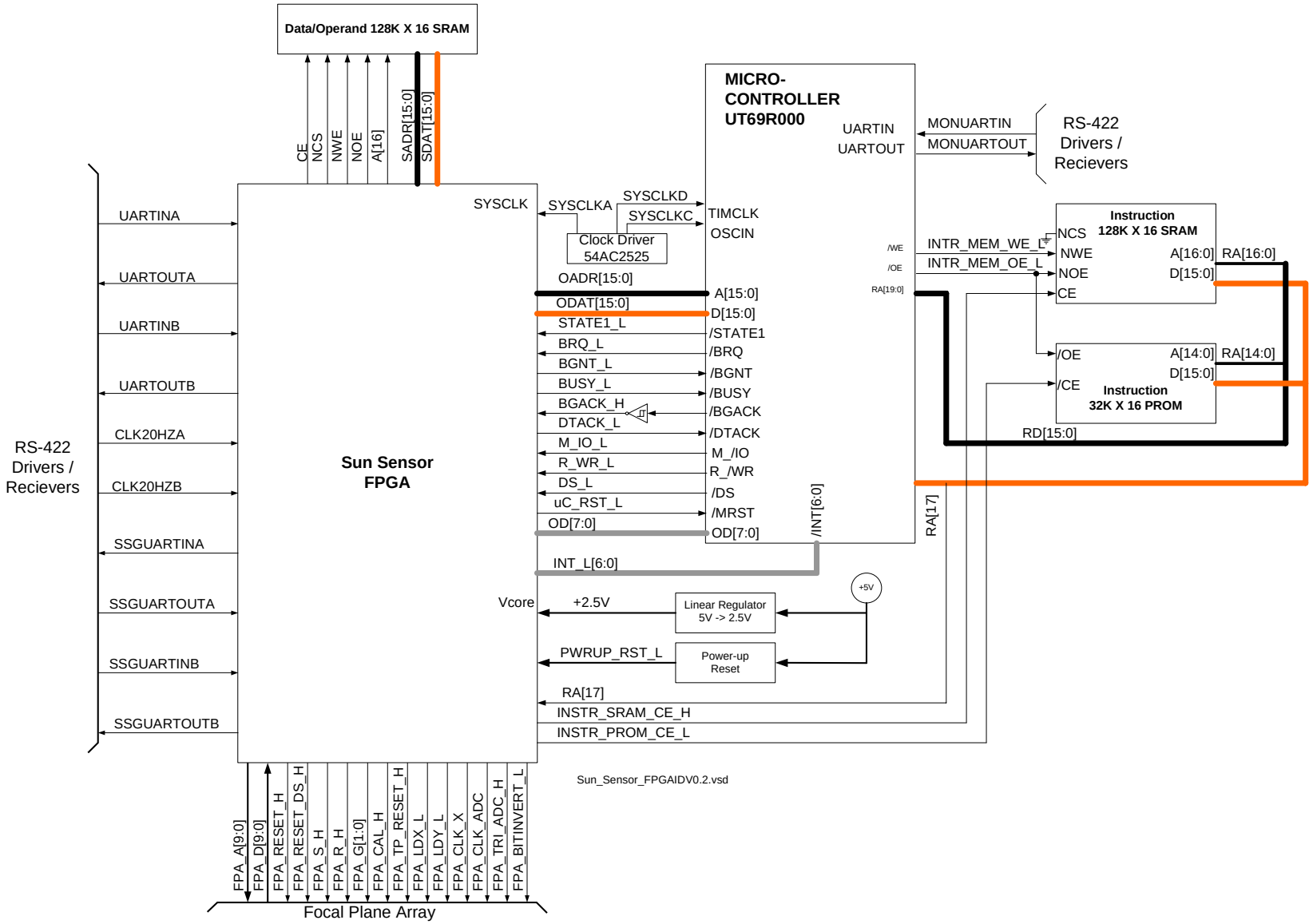


Figure 56 Sun Sensor FPGA Interface Diagram

11. SOFIE HARDWARE/SOFTWARE ICD

This section presents the interfaces between the software systems and the SOFIE electronics. The microcontroller architecture, memory maps, data acquisition maps, and external registers are described in this section. Refer to document number SDL/03-413 for a description of the SOFIE to SSG Steering Mirror Hardware / Software Interface.

The SOFIE Instrument contains two microcontrollers, the Sun Sensor microcontroller and the Command and Data Handling microcontroller. These microcontrollers communicate via a serial communication bus. The physical layer and protocol layer for these interfaces is defined in the following section.

11.1 SOFIE Serial Communication Description

11.1.1 SOFIE Serial Communication RS-422 Physical Layer Interface Definition

The digital communication link between the Sun Sensor and the SSG Servo I/O boards and between the C&DH and the Sun Sensor boards shall be defined as follows:

Interface driver, receiver type:	RS-422
Cable impedance (twisted shielded pair):	100 ohms
Resistance in series with driver outputs:	50 ohms +/- 5 %
Receiver Input Impedance:	~ 10 k (on or off)
Logic 0:	“Low” voltage at driver input, receiver output
Logic 1:	“High” voltage at driver input, receiver output
Start bit:	Logic 0,
Speed:	57600 Baud
Data size:	8-bit
Serial stream:	Least significant bit (LSb) first
Parity bit:	Odd
Stop bit:	Logic 1
Word size:	2 bytes; least significant byte (LSB) sent first

To maintain word alignment, all serial communications must be 16-bit words, but to ensure PC compatibility, as shown above, the UART data size is still 8-bits. In other words, every communication must consist of two 8-bit transfers to make one 16-bit word value. The least significant byte (LSB) shall always be sent first.

Data is broken up into packets and subpackets. The maximum size of a subpacket is 511 16-bit words. There can be up to 65,535 subpackets created to represent one packet of data. If the number of data words to be sent is 504 or less, only 1 subpacket is required. If the number of data words is larger than 504, multiple subpackets are required (see Figure 57 below for subpacket details).

UART Sub-packet Calculations

Baud Rate: 57600

Note: **Least significant bit sent first**

Description	*Value*	Minimum Sub-packet *Width (bytes)*	Maximum Sub-packet *Width (bytes)*
Start Sync Word	AAAAh	2	2
Opcode / Mode	xxxxh	2	2
Sub-packet Number (Current)	1 - 64k	2	2
Sub-packet Total (Count)	1 - 64k	2	2
Payload Length (N words)	0 - 504	2	2
Data Word (1)	xxxxh		2
.	.		.
.	.		.
.	.		.
Data Word (N)	xxxxh		2
CheckSum	xxxxh	2	2
End Sync Word	7777h	2	2
	Bytes:	14	1022
	RS-422 Overhead:	11 bits/byte	11 bits/byte
	Total bits/packet:	154	11242
	Baud Rate:	57600	57600
	Time/packet:	2.67E-03	0.20
	Packets/sec:	374.03	5.12

Figure 57 Sun Sensor to SSG Servo I/O Communication Subpacket Description

To help with re-alignment, there must always be dead time on the communication interface between subpackets. Normally, there is not dead time between bytes within a subpacket. Dead time is defined as 5 bit periods of silence, or 86.81 µs following a stop bit.

The checksum calculation is an XOR operation on all words (2-byte) of the packet from the "Opcode/Mode" field to the last "Data Word" field (Start and End Sync Words and the Checksum field are not included in the checksum calculation). The resulting checksum will be one word (2 bytes).

Note: If communicating with a PC UART, there may be dead time between bytes within a subpacket. Dead time followed by a start sync word will be the start of a subpacket. Dead time not followed by a start sync word is somewhere within the current subpacket. For re-alignment, if necessary, wait until dead time is followed by a start sync word, a valid opcode, sub-packet header information, and a correct checksum.

An example timing diagram is shown in Figure 58.

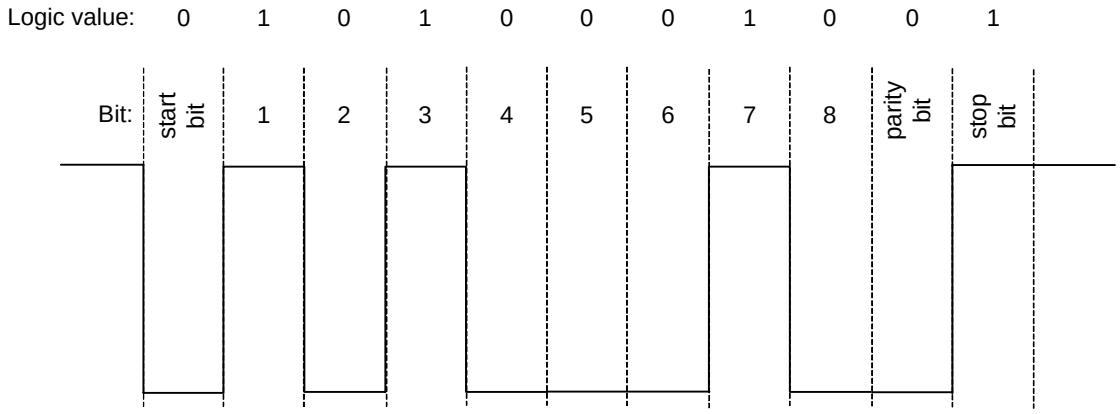


Figure 58 Timing Diagram (example)

The SOFIE Sun Sensor Board and the C&DH board will utilize Intersil radiation hardened quad differential line drivers and receivers:

Driver Part No.	HS9-26CT31RH-Q (5962F9563201QXC)
Receiver Part No.	HS9-26CT32RH-Q (5962F9563101QXC)

Source termination shall be with a 50 ohm 0805 resistor package in series out of each driver output. However, a potential shunt termination network shall be implemented by building a 0805 pad in series with a 1210 pad (See Figure 59).

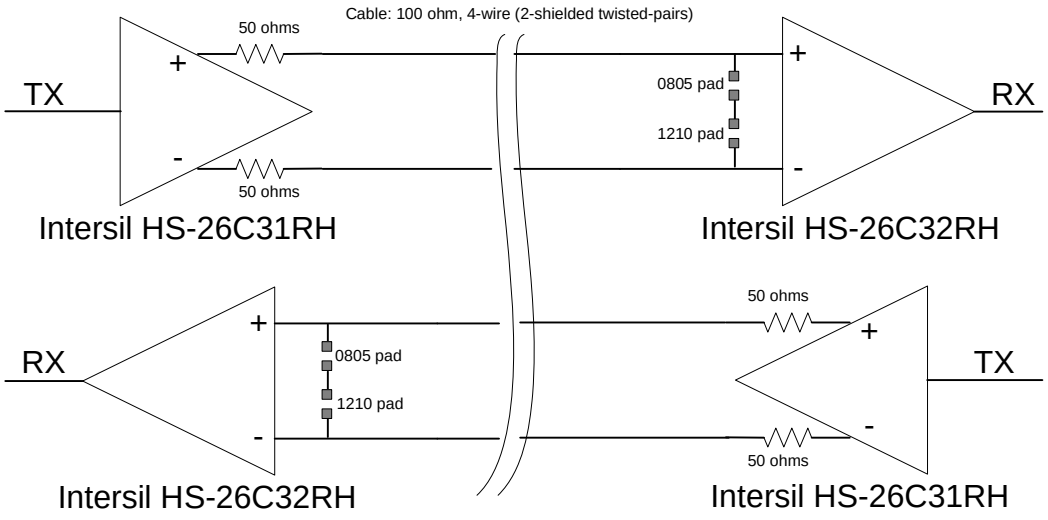


Figure 59 Schematic Representation of Data Link

The data link cable will be contained in the SOFIE cable bundle between the electronics box and the instrument. SDL/SOFIE will ensure that the cable is manufactured according to the above specifications. .

The communication interface shall be redundant RS-422. The UART shall transmit data on both redundant channels (A and B) at all times. The UART should also be configurable to receive on either side. Two driver and receiver pairs shall be implemented exactly as described above. The transmit side of one UART connects to the receive side of the other unit as show in Figure 60. The swap of transmit to receive occurs in the cable as shown in Refer to the cabling section for specific pin number assignments.

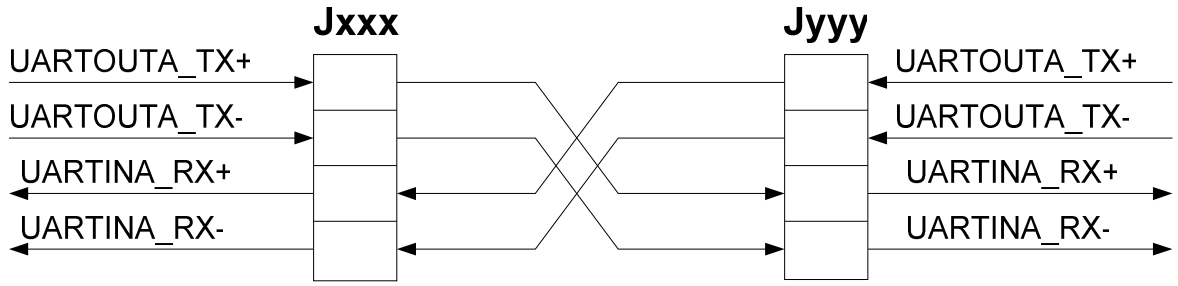


Figure 60 Data Link Cable Wiring

11.1.2 Serial RS-422 Communication Queues

The data to be transmitted and the received data is stored in circular transmit and receive queues. These queues, along with the UART control registers, are shown in Figure 61 UART Control Registers and Queues.

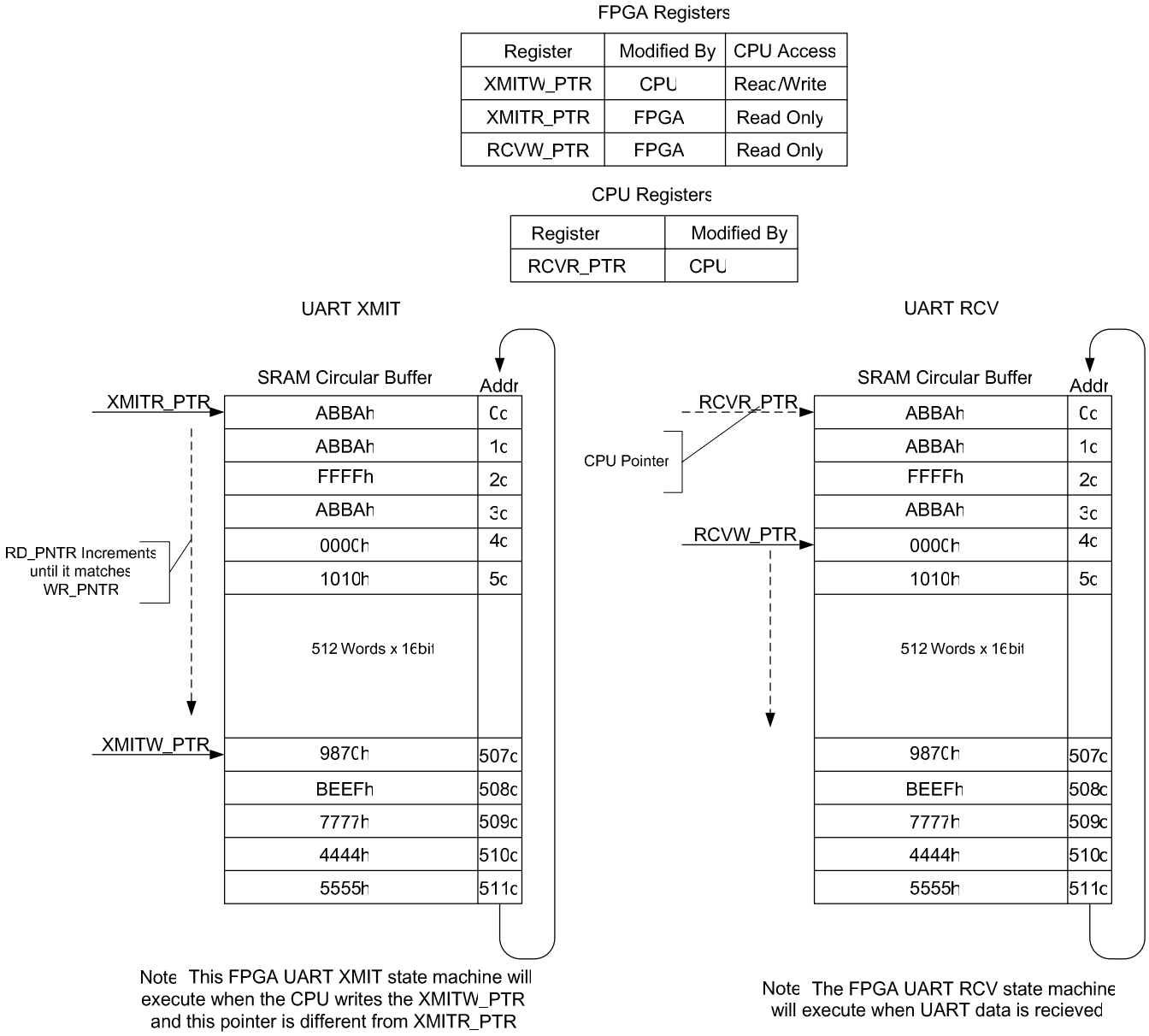


Figure 61 UART Control Registers and Queues

The Transmit and Receive Queues are controlled by four memory mapped control registers. These registers contain pointers for writing data into and reading data from the queues.

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11.1.3 Internal Serial Communication Command Definition

The microcontrollers communicate with each other by sending commands and data via the serial RS-422 communication busses described previously. The following sections describe the commands between the C&DH and the Sun Sensor microcontrollers. Reference the SOFIE Command and Telemetry Handbook (SDL/05-936) for a full command set. The commands

between the Sun Sensor microcontroller and the SSG Servo I/O board are described in the SSG ICD (SDL/03-0413).

11.2 Time Synchronization Description

Time synchronization shall occur between the C&DH, Sun Sensor, and SSG Servo I/O boards. A 16-bit FRT (free running timer) shall be maintained in each board's FPGA with a resolution of 100 µs. The FRT should roll over every 6.5535 seconds. Synchronization is accomplished using an arm signal and the CLK20HZ signal. The CLK20HZ sync clock signal comes from the C&DH board to the Servo I/O board across the backplane on two redundant pins. The pins on the Backplane connector are:

BP_CLK20HZa on J208-120
BP_CLK20HZb on J208-121

The arm signal is also on redundant pins. The pins on the Backplane connector are:

BP_RESET_ARM_Ha on J208-122
BP_RESET_ARM_Hb on J208-123

A command is sent to the Sun Sensor Processor which generates the Arm signal on the Sun Sensor board. The 20 Hz Clock Signal is sent to the Sun Sensor board on the Cable between the C&DH board and the Sun Sensor Board. The pin assignments are:

C&DH Signal	C&DH Pin	Sun Sensor Signal	Sun Sensor Pin
20HZSYNCA_TX+	J370-12	20HZSYNCA_RX+	J610-6
20HZSYNCA_TX-	J370-31	20HZSYNCA_RX-	J610-22
20HZSYNCB_TX+	J370-8	20HZSYNCB_RX+	J610-7
20HZSYNCB_TX-	J370-27	20HZSYNCB_RX-	J610-23

The Reset Arm signal tells the Servo I/O board and the Sun Sensor board to reset its Free Running Timer and 100 microsecond Clock Generator on the falling edge of the next 20 Hz sync clock signal. The CLK20HZ and the RESET_ARM signals shall be synchronized to the local 12 MHz system clock using dual rank synchronizers. An edge detect circuit shall be used to detect the falling edge of the 20 HZ clock because it is a 50% duty cycle clock.

The Free Running Timer shall have a snapshot holding register that shall be updated on the falling edge of each CLK20HZ clock. This snapshot holding register shall be reset when the Free Running Timer is reset.

An overview of the Time Synchronization is shown in Figure 62 and a detailed block diagram is shown in Figure 63. The timing diagram for the Time Synchronization is shown in Figure 64.

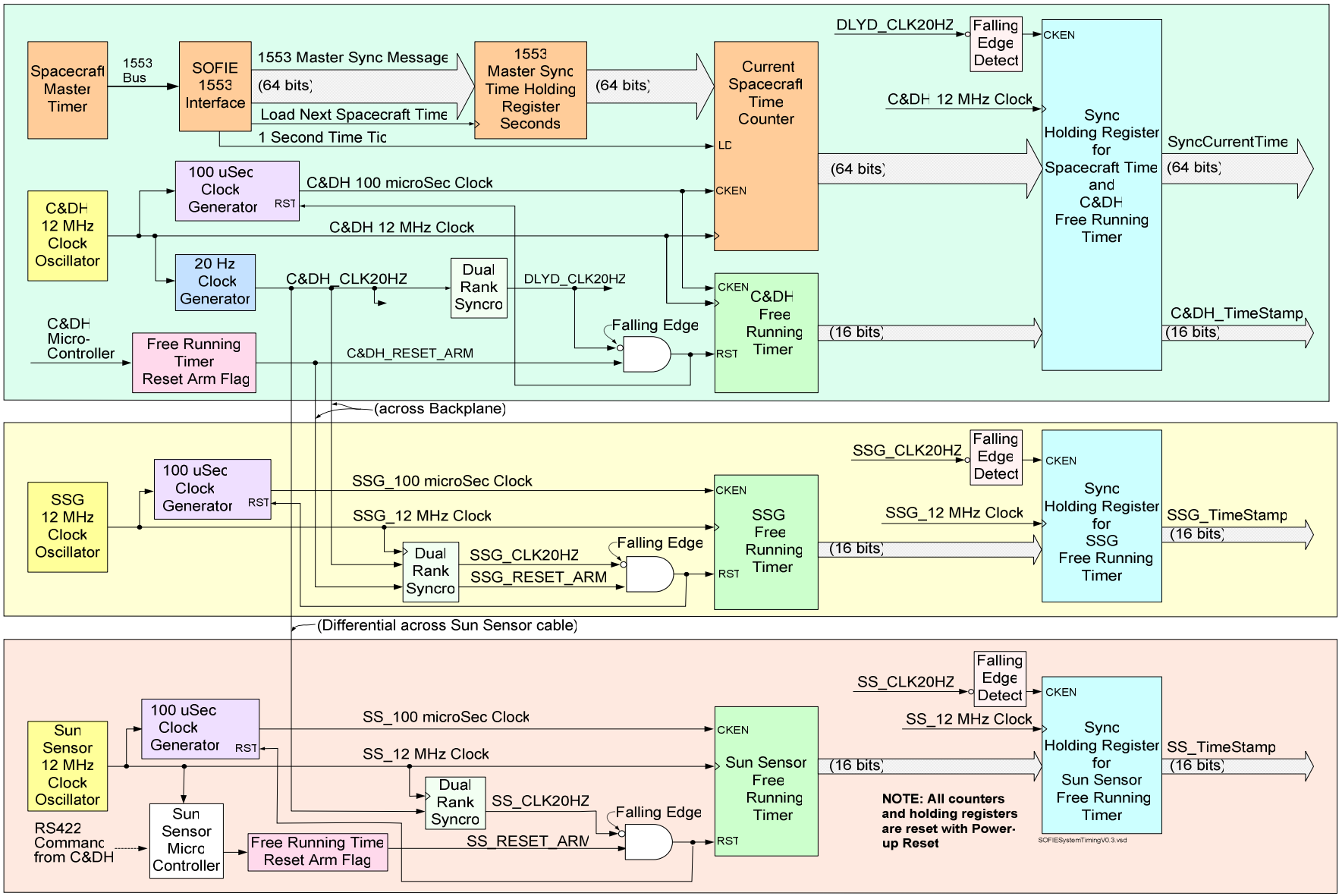


Figure 62 Time Synchronization Overview

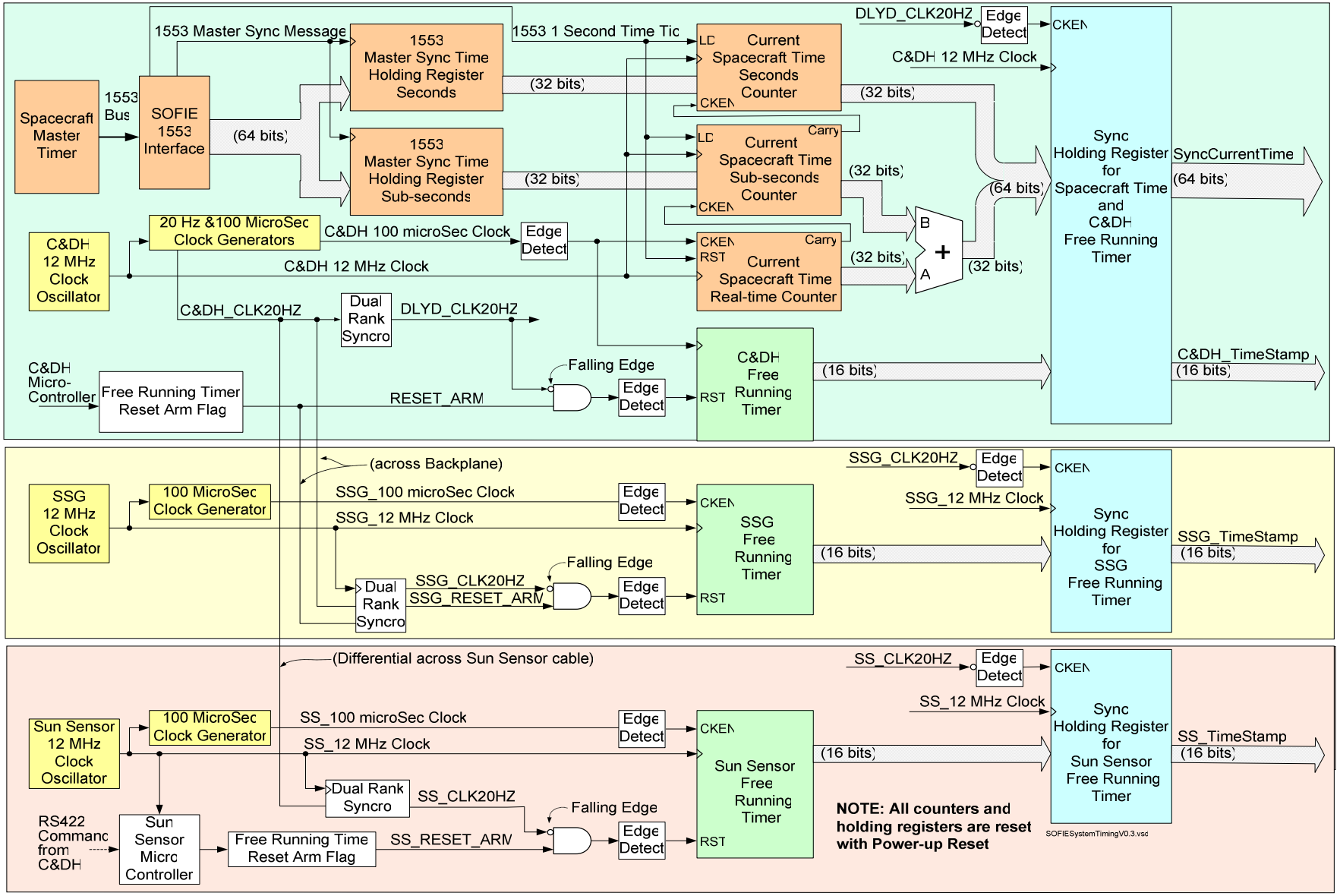


Figure 63 Time Synchronization Block Diagram

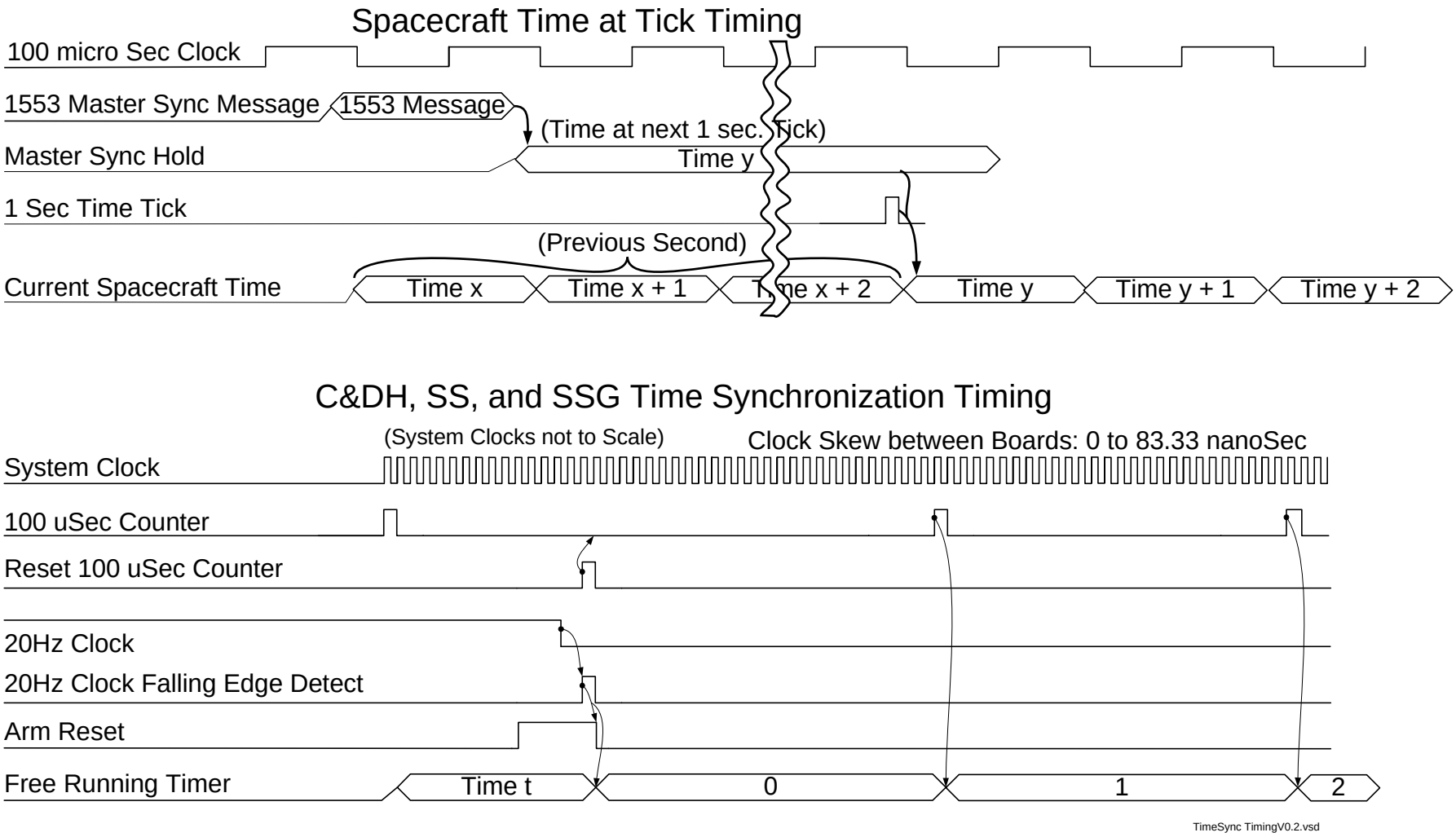


Figure 64 Time Synchronization Timing

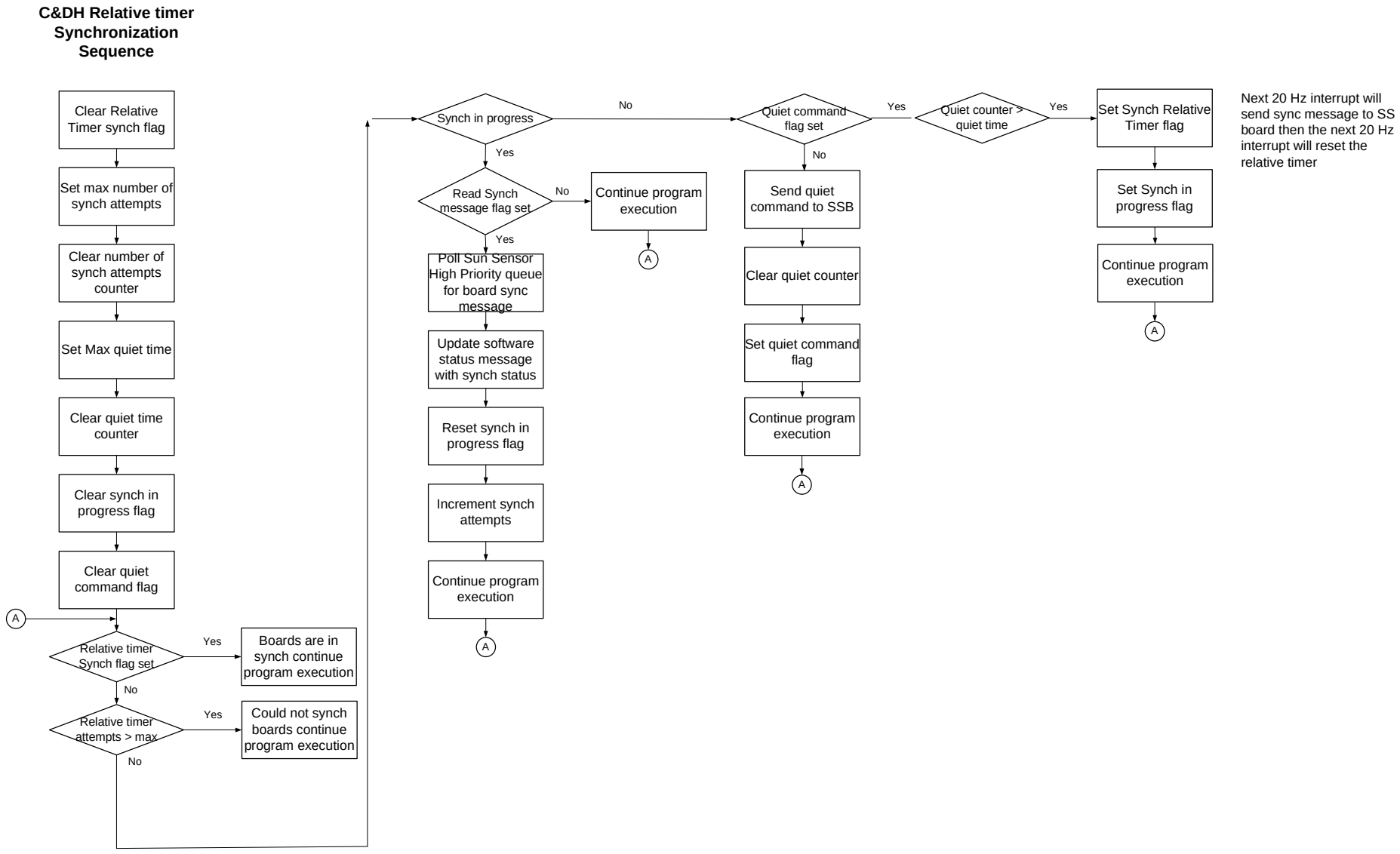


Figure 65 C&DH Relative Timer Synchronization Sequence

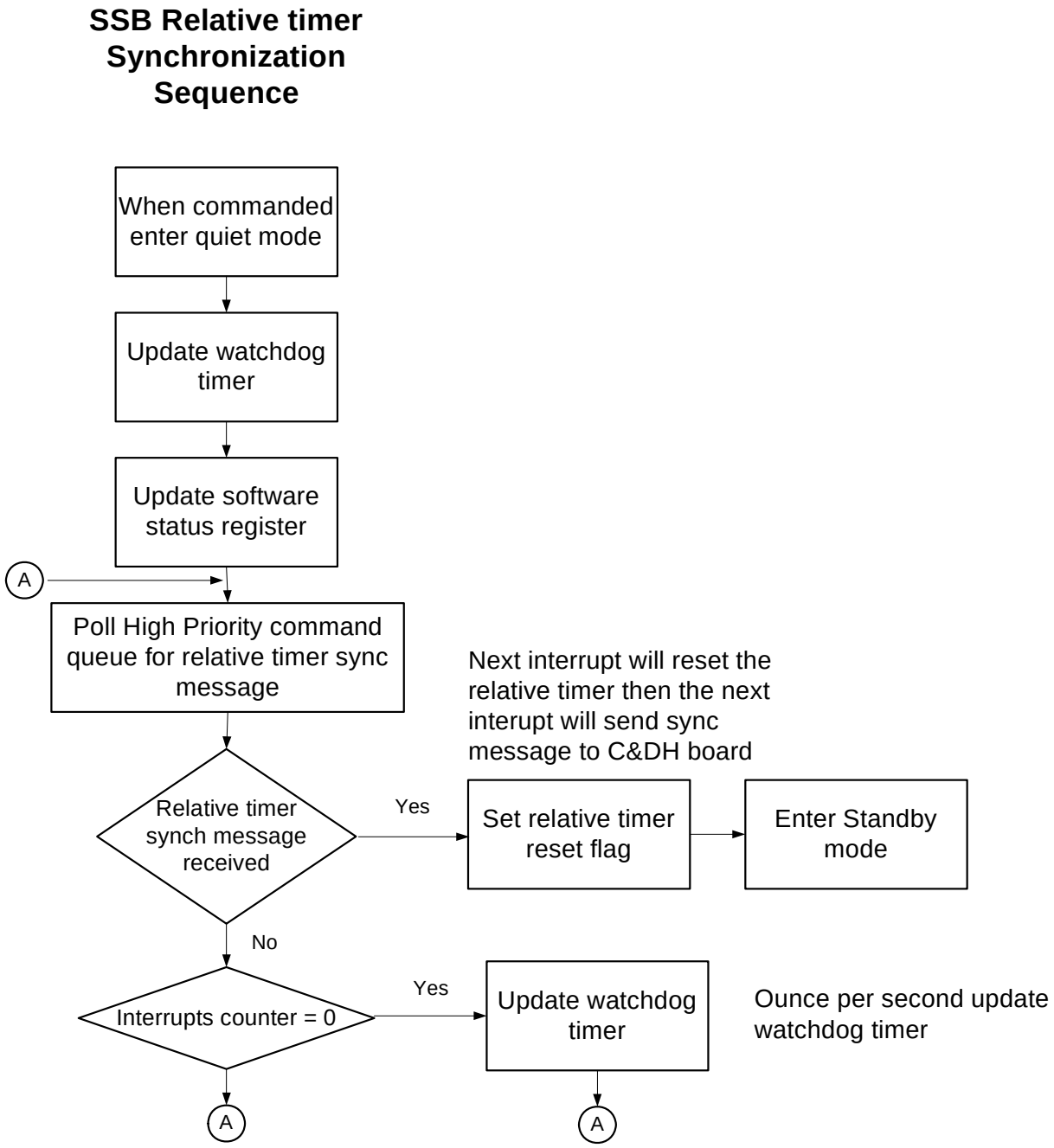


Figure 66 Sun Sensor Board Relative Timer Synchronization SequenceStart-upSequence Description

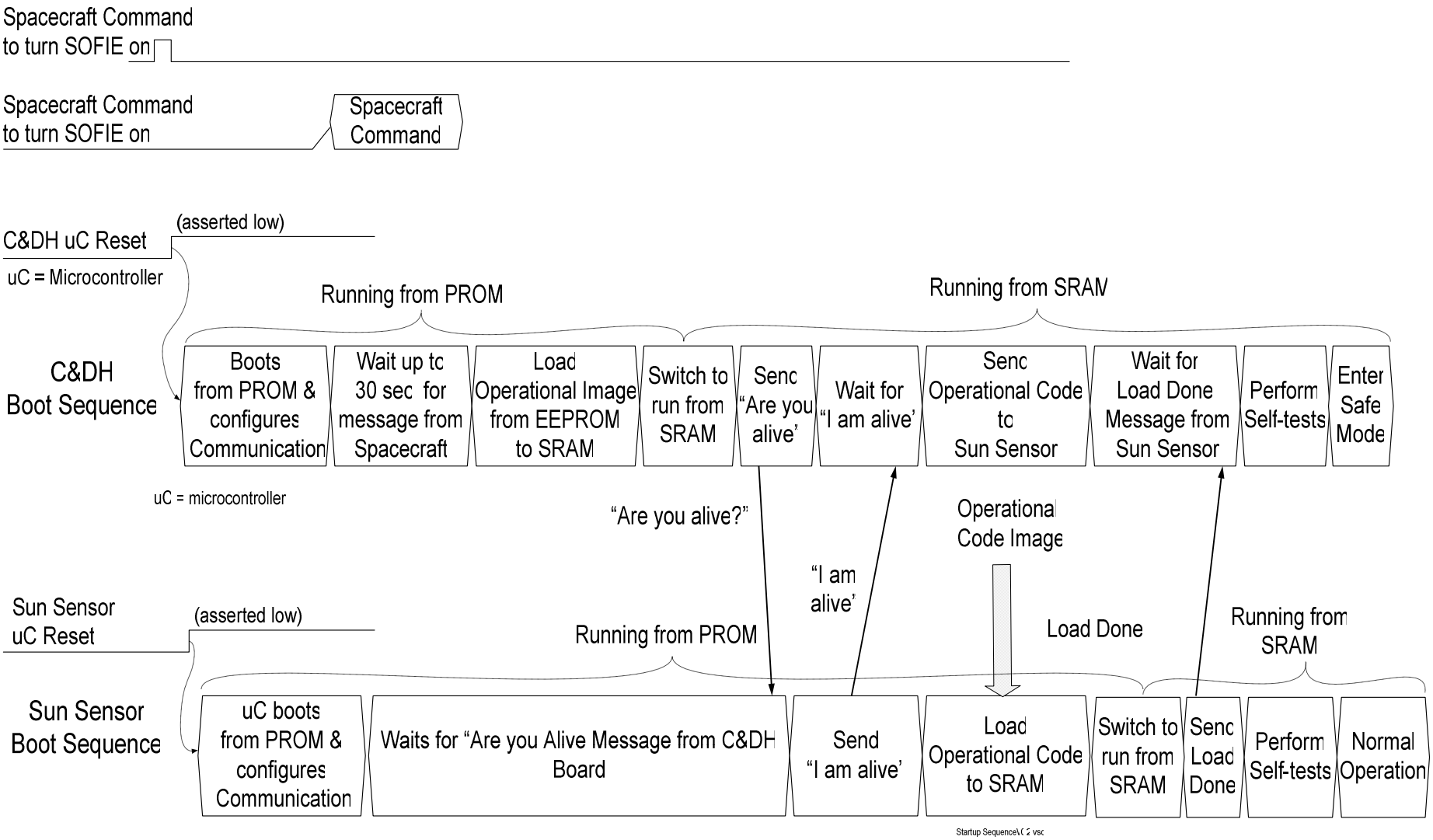


Figure 67 SOFIE Startup Sequence Overview

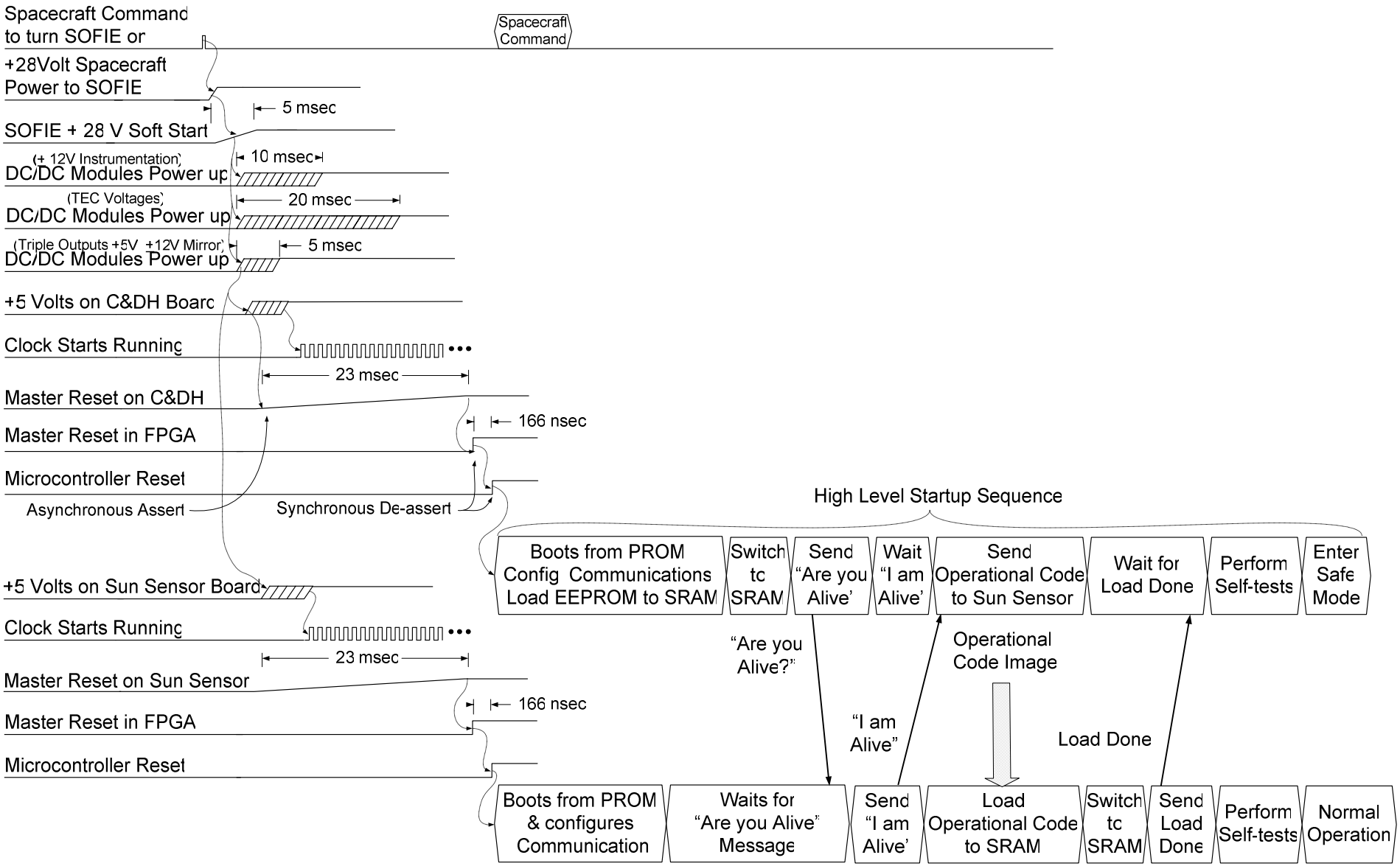


Figure 68 SOFIE Start-up Timing

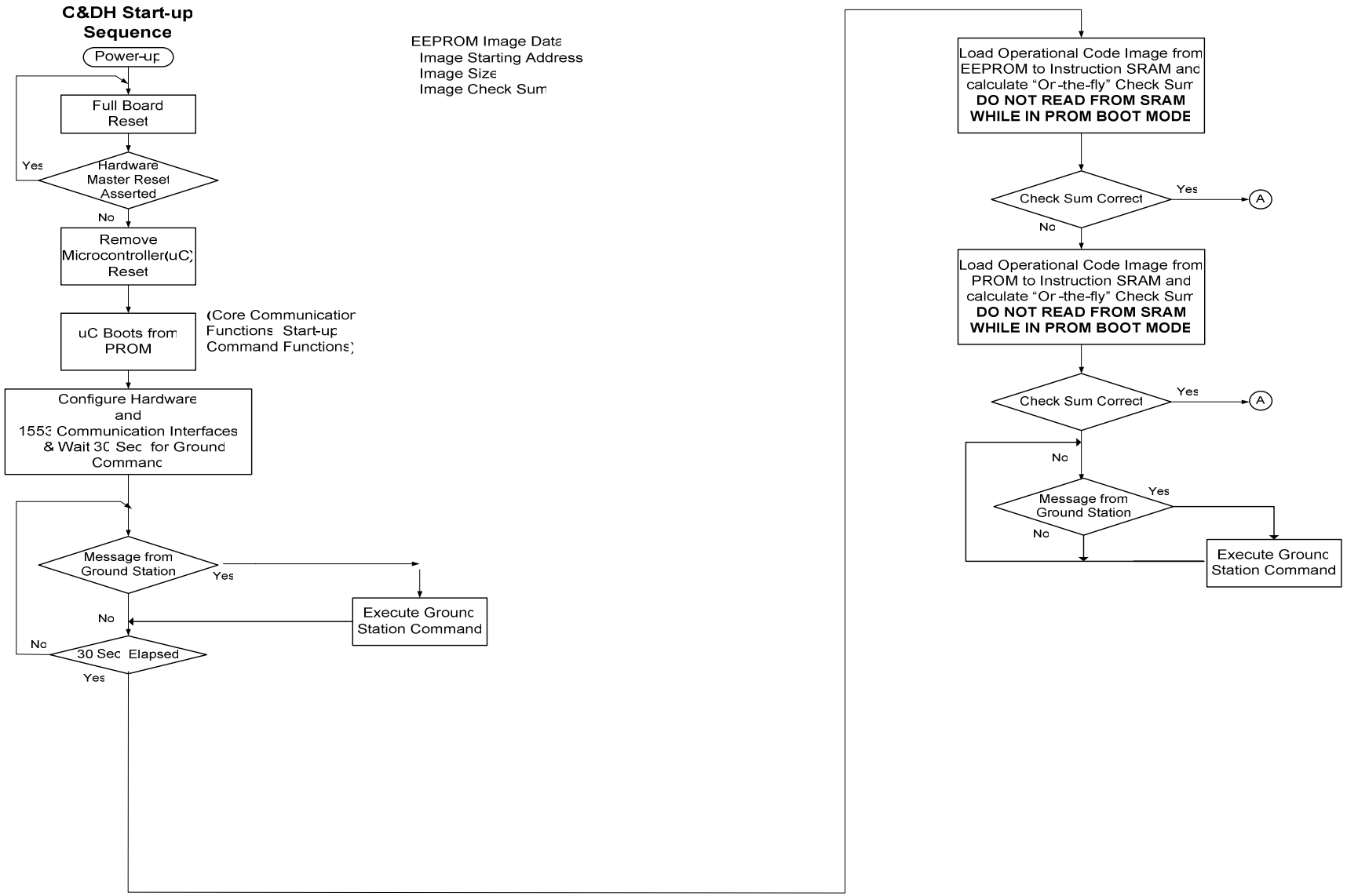


Figure 69 Detailed Startup Sequence - Part 1

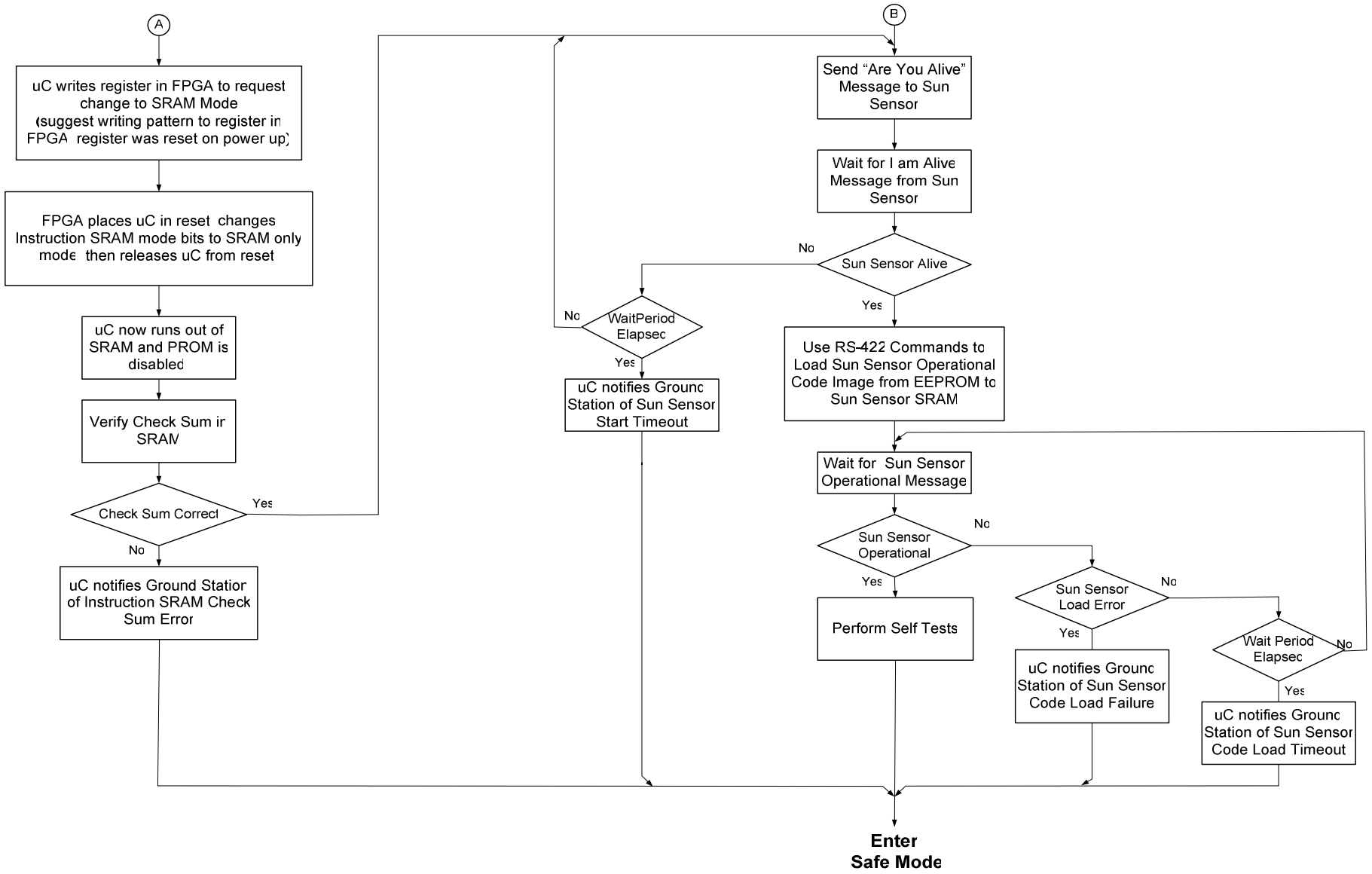


Figure 70 Detailed Startup Sequence - Part 2

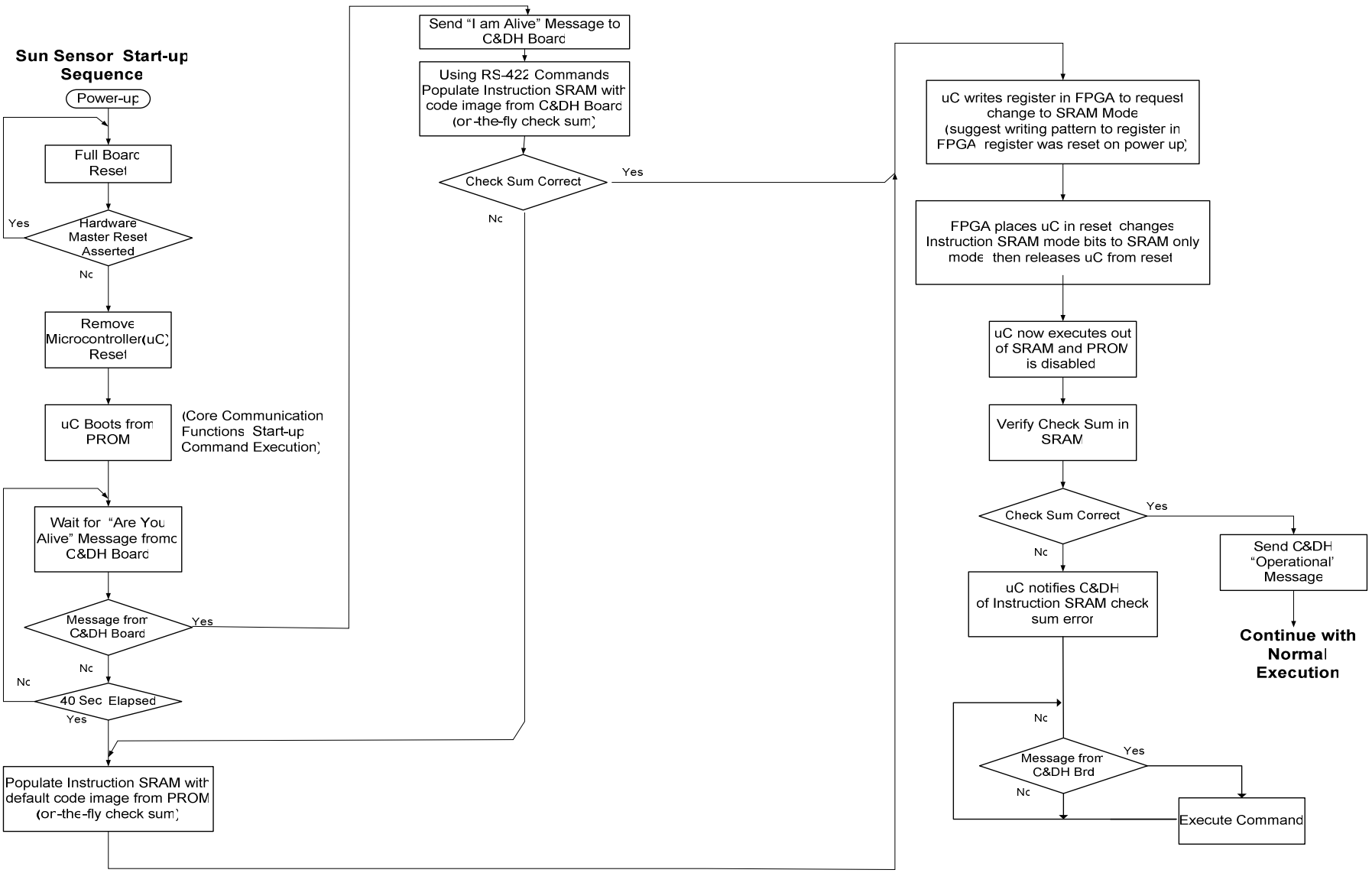


Figure 71 Detailed Startup Sequence - Part 3

11.3 Sun Sensor 100 HZ Loop Description

A timing diagram for the 100 Hz Steering Mirror control loop is shown in Figure 72.

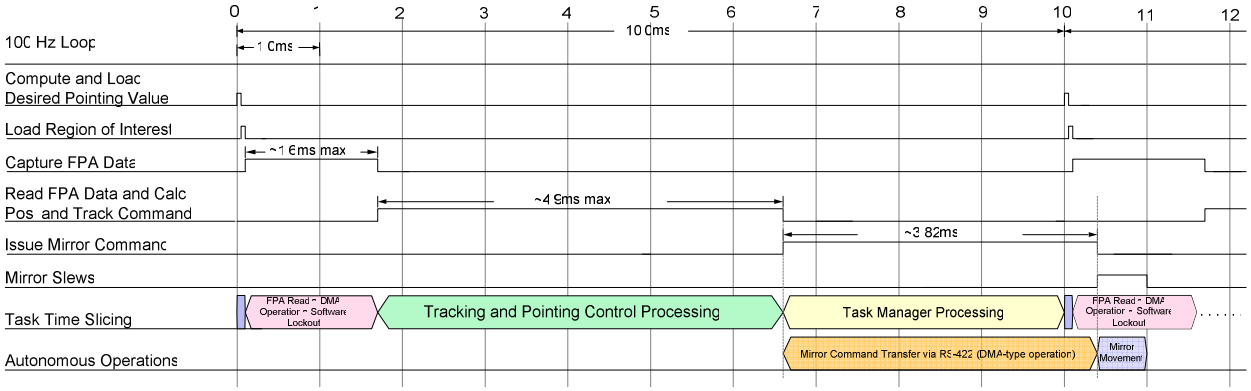


Figure 72 Steering Mirror 100 Hz Control Loop Timing

11.4 Pin Puller "No Fire Description"

A block diagram for the Pin Puller Circuit is shown in Figure 73. The Pin Puller Firing Sequence is shown in Figure 74

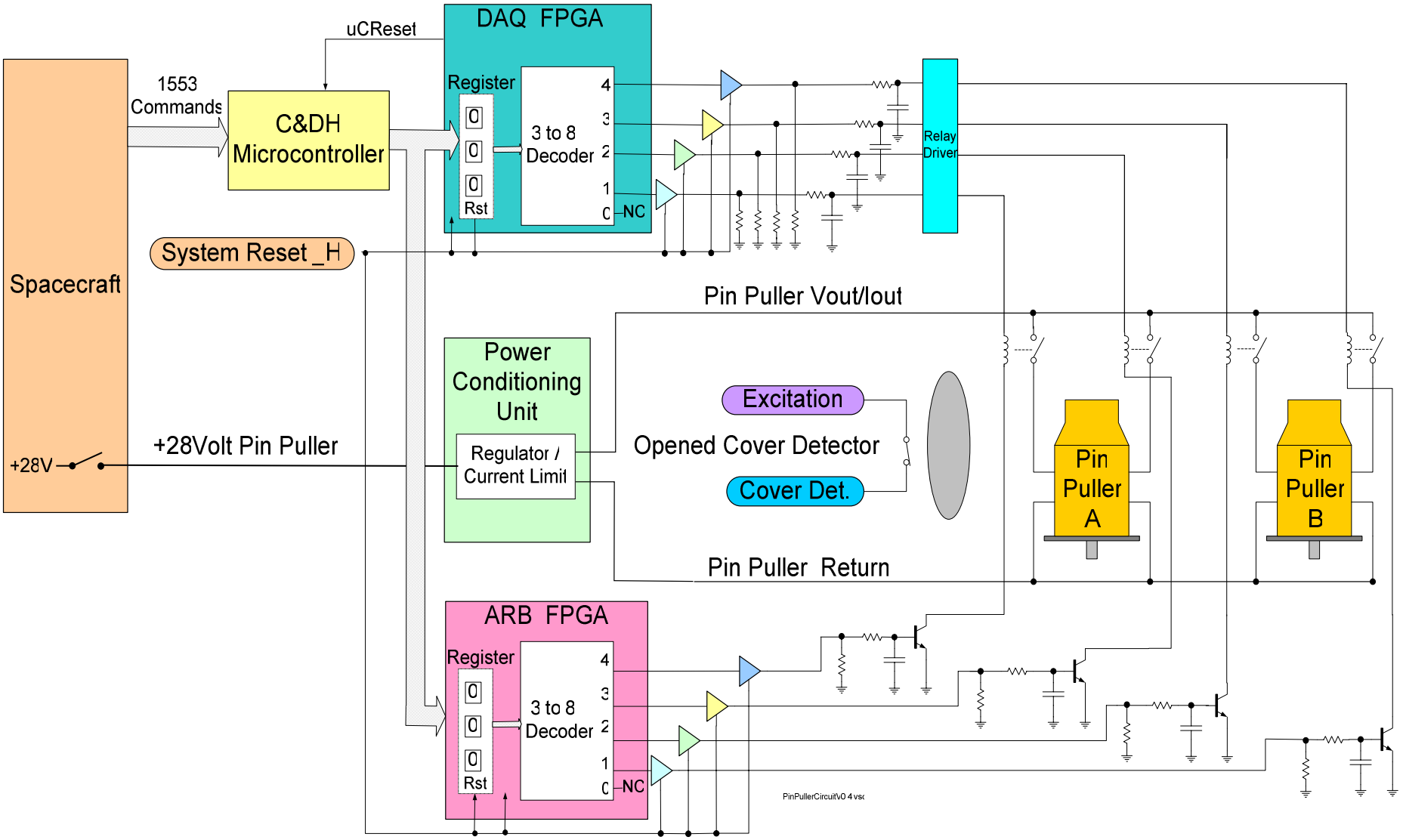


Figure 73 Pin Puller Circuit Block Diagram

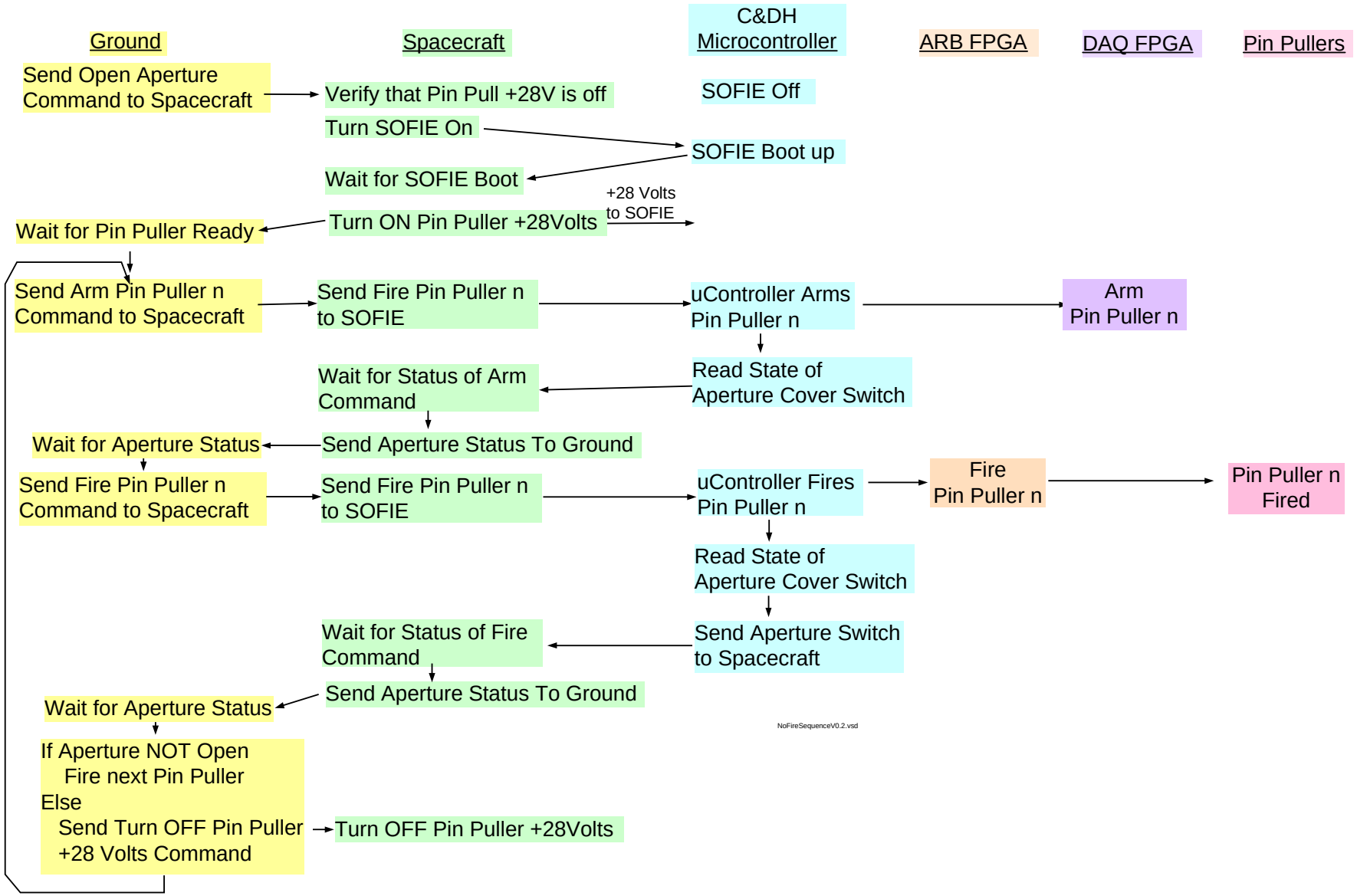


Figure 74 Pin Puller “No Fire” Sequence

11.5 Sun Sensor Hardware/Software Interface

The Sun Sensor microcontroller interfaces with the FPA, the SSG Steering Mirror Servo I/O, and the C&DH Board. The interface to the FPA is through an FPGA on the Sun Sensor board. The interfaces to the SSG Servo I/O board and the C&DH board are through serial RS-422 interfaces. The previous section defines the serial RS-422 communication.

The Sun Sensor Memory Architecture / Programmers Model is shown in Figure 75. This diagram shows the processing and storage elements comprising the Sun Sensor System. The Sun Sensor system is composed of:

- 16-bit radiation-hardened microcontroller, the Aeroflex/UTMC UT69R000
- Instruction Memory
- Data/Operand Memory
- Processor Bus Arbiter
- External registers implemented in an FPGA
- Watch Dog Timer
- RS-422 Communication Interfaces
- RS-422 Microcontroller Serial Monitor Port

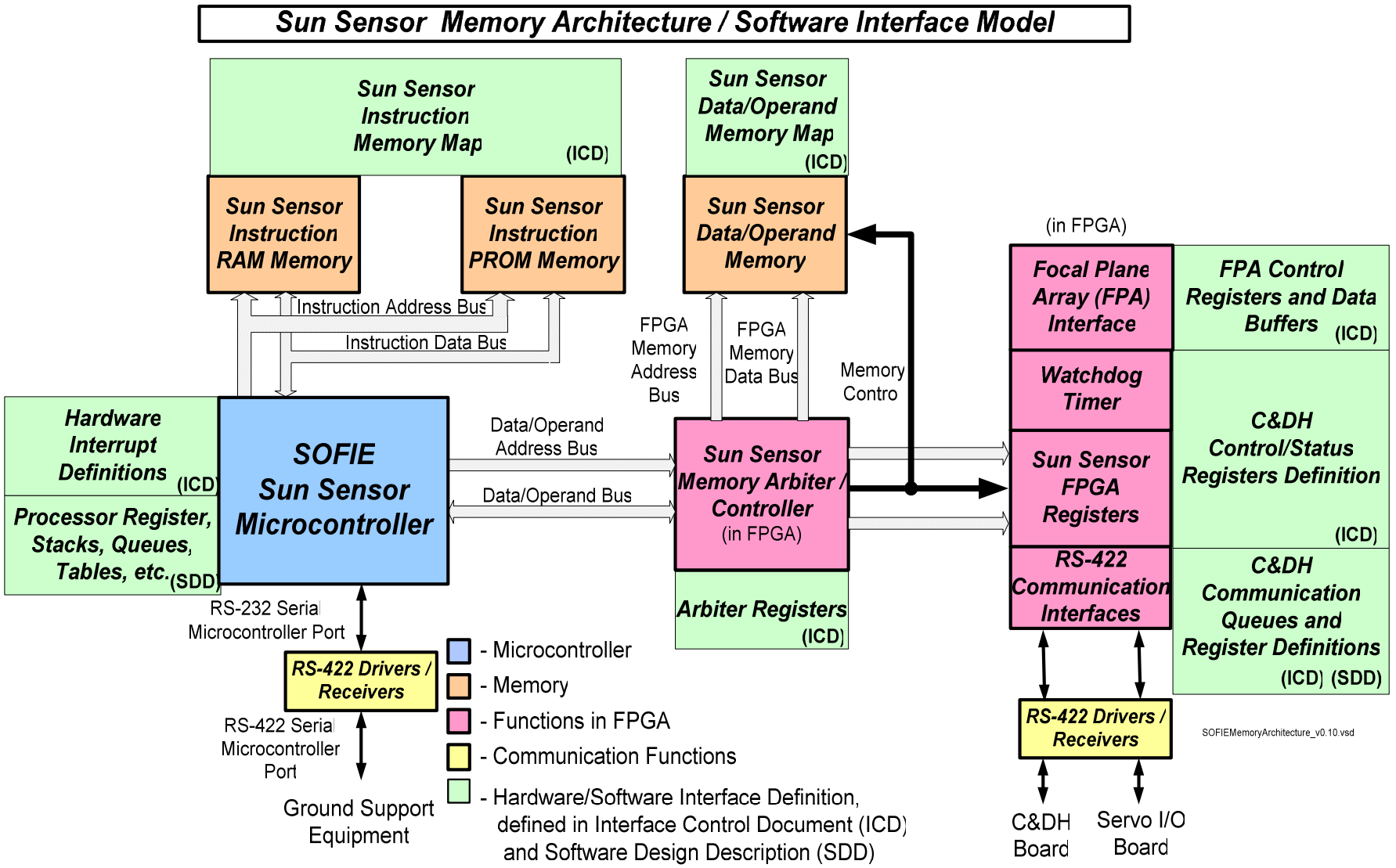


Figure 75 Sun Sensor Memory Architecture / Programmers Model

11.5.1 Sun Sensor Microcontroller Interrupt Definitions

INTERRUPT NUMBER	DESCRIPTION
0 (Highest Priority)	Power-Down Interrupt, Cannot be masked or disabled. **Implemented Not Used**
1	Machine Error. Cannot be disabled. **Spurious Interrupt Handler**
2	INT0. External user interrupt. **20 HZ Interrupt A**
3	Software interrupt (USR3). **Spurious Interrupt Handler**
4	Fixed-point overflow (V bit). **Spurious Interrupt Handler**
5	Software interrupt (USR2). **Implemented Not Used**
6	Software interrupt (USR1). **Spurious Interrupt Handler**
7	Timer A (If implemented). **Used for timing generation**
8	INT1. External user interrupt. **20 HZ Interrupt B**
9	Timer B (If implemented). **Used for timing generation**
10	INT2. External user interrupt. **Spurious Interrupt Handler**
11	INT3. External user interrupt. **Spurious Interrupt Handler**
12	INT5. External user interrupt. **Spurious Interrupt Handler**
13	INT4. External user interrupt. **Spurious Interrupt Handler**
14 (Lowest Priority)	INT6. External user interrupt. **Spurious Interrupt Handler**

Table 1 Sun Sensor Microcontroller Interrupts Definition

11.5.2 Sun Sensor Memory Maps

The memory bank selection is described below and the Sun Sensor Memory Map is shown in Figure 76.

Data Memory Bank Select

Note: operand SRAM (lower 64k) is permanently mapped to the microcontroller's memory address space. For access to other memory regions, the microcontroller needs to use the port I/O instruction and select the region by using the Output Discrete bus (OD(7:0)) as defined in Figure 76.

Data Memory Bank Select

Note: operand SRAM (lower 64k) is permanently mapped to the microcontroller's memory address space. For access to other memory regions, the microcontroller needs to use the M/IO instruction and select the region by using the Output Discrete bus (OD[7:0]) according to the following table.

OD[7:0]	Bank
0x00h	Operand SRAM (upper 64k)
0x04h	FPGA Registers

Figure 76 Sun Sensor Microcontroller Data Memory Bank Select

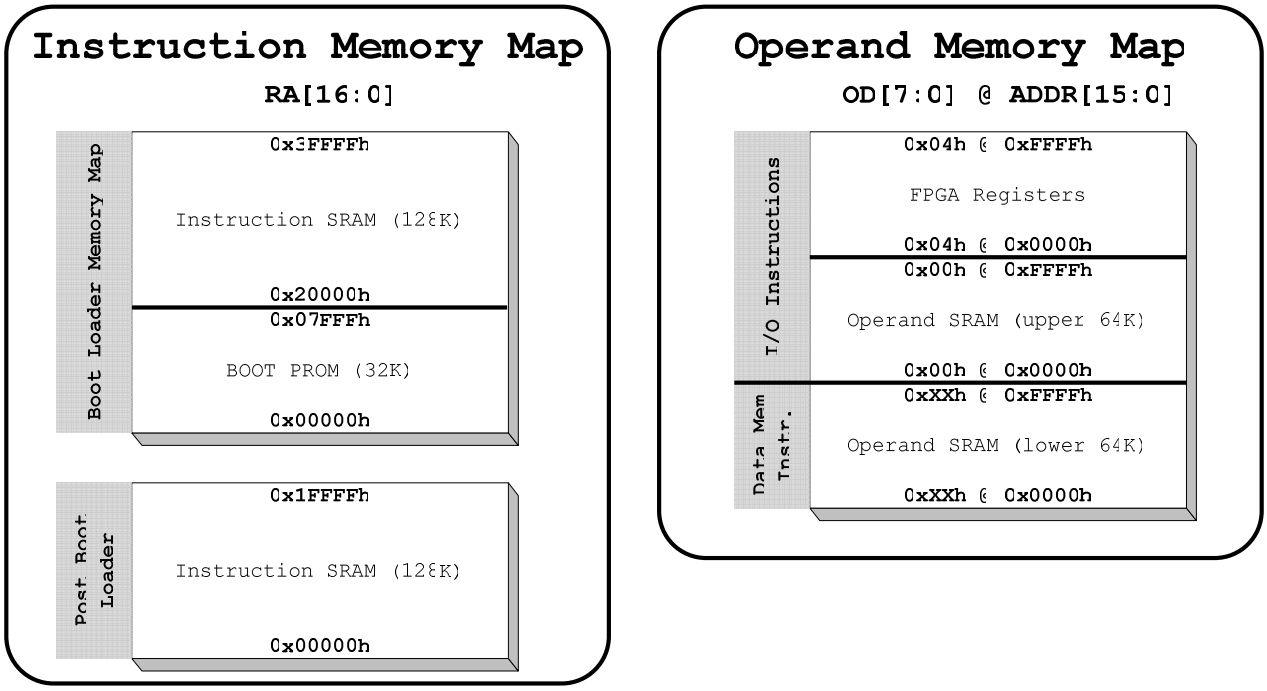


Figure 77 Sun Sensor Processor General Memory Maps

11.6 Sun Sensor FPA Interface

The Sun Sensor microcontroller does not directly interface with the focal plane array (FPA). The microcontroller commands the FPGA to transfer a block of data from the FPA into the upper 64KB of Operand SRAM. The FPGA stores the data sequentially in operand memory beginning at address: 0x10000h + Memory Offset value (normally 0x0000h). The max block size of data that can be transferred is 64K pixels. The block of data is defined by

configuration registers in the FPGA. Rectangular coordinates are configured by a sequence of 4 writes to the FPGA (X1, Y1) to (X2, Y2). The column (x) and row (y) step sizes are also configured in the FPGA. Row Time and Row Reset Time registers are configured in system clock counts and are determined by the number of rows to read and the reset band. Integration Time is configured in multiples of Row Time + Row Reset Time. The command/status register is then configured to command the FPGA to begin the data transfer.

Image Sensor FPGA Registers

Address	15 ... 0
0x0300h	CSR
0x0301h	X1 Register
0x0302h	X2 Register
0x0303h	Y1 Register
0x0304h	Y2 Register
0x0305h	Y step / X step
0x0306h	Memory Offset
0x0307h	Row Time
0x0308h	Integration Time
0x0309h	Current Pixel Addr
0x030Ah	Reset Band
0x030Bh	Row Reset Time

Figure 78 Sun Image Sensor FPGA Registers

11.6.1 Sun Sensor Registers Definition

Sun Sensor FPGA Registers (OD[7:0] = 0x04)						
Register Name	**Size (bits)**	**Description**	**CPU**	**Address**	**FPGA**	**Reset Value**
CDHUARTCSR	7	UART status/control Bit 0: Set bit to reset UART (CTRL) Bit 1: RCV Ch A or B (A=0, B=1)(CTRL) Bit 2: Parity Error (Status) Bit 3: Framing Error (Status) Bit 4: RCV Dead Time (Status) Bit 5: RCV Busy (Status) Bit 6: XMIT Busy (Status)	R/W	0x0100	R/W	0x00
CDHUARTXMITADDR	7	UART XMIT buffer memory location: ADDR[15:9]	R/W	0x0101	R	0x00
CDHUARTRCVADDR	7	UART RCV buffer memory location: ADDR[15:9]	R/W	0x0102	R	0x00
CDHUARTXMITWPTR	9	UART XMIT write buffer pointer address ADDR[8:0]	R/W	0x0103	R	0x00
CDHUARTXMITRPTR	9	UART XMIT read buffer pointer address ADDR[8:0]	R	0x0104	R/W	0x00
CDHUARTRCVWPTR	9	UART RCV write buffer pointer address ADDR[8:0]	R	0x0105	R/W	0x00
SSGUARTCSR	7	UART status/control Bit 0: Set bit to reset UART (CTRL) (CTRL) Bit 1: RCV Ch A or B (A=0, B=1)(CTRL) Bit 2: Parity Error (Status) Bit 3: Framing Error (Status) Bit 4: RCV Dead Time (Status) Bit 5: RCV Busy (Status) Bit 6: XMIT Busy (Status)	R/W	0x0200	R/W	0x00
SSGUARTXMITADDR	7	UART XMIT buffer memory location: ADDR[15:9]	R/W	0x0201	R	0x00
SSGUARTRCVADDR	7	UART RCV buffer memory location: ADDR[15:9]	R/W	0x0202	R	0x00
SSGUARTXMITWPTR	9	UART XMIT write buffer pointer address ADDR[8:0]	R/W	0x0203	R	0x00

SSGUARTXMITRPTR	9	UART XMIT read buffer pointer address ADDR[8:0]	R	0x0204	R/W	0x00
SSGUARTRCVWPTR	9	UART RCV write buffer pointer address ADDR[8:0]	R	0x0205	R/W	0x00
FPACSR	9	Focal Plane Array (FPA) CSR: Bit 0: FPARST_H Set bit to reset FPA controller (CTRL) Bit 1: PIXRST_H Set bit to reset rows Y1 - Y2 (CTRL) Bit 2: START_H Set bit to begin FPA action (CTRL) Bit 3: FPA_G0 (amplifier gain; G[0]) (CTRL) Bit 4: FPA_G1 (amplifier gain; G[1]) (CTRL) Bit 5: FPABITINVERT_L (invert=0, no=1) (CTRL) Bit 6: RDY_L (Ready=0, Busy=1) Bit 7: ERR_BLK_SIZE_H (error=1) Bit 8: ERR_STEP_SIZE_H (error=1)	R/W	0x0300	R/W	0x00
FPAX1	10	Sun sensor X1 block coordinate DAT[9:0]	R/W	0x0301	R	0x00
FPAX2	10	Sun sensor X2 block coordinate DAT[9:0]	R/W	0x0302	R	0x00
FPAY1	10	Sun sensor Y1 block coordinate DAT[9:0]	R/W	0x0303	R	0x00
FPAY2	10	Sun sensor Y2 block coordinate DAT[9:0]	R/W	0x0304	R	0x00
FPASTEPSIZE	16	Sun sensor pixel return step size: LSB: X address increment size: [7:0] MSB: Y address increment size: [15:8]	R/W	0x0305	R	0x0101
FPAMEMOFFSET	16	Memory offset for location to return image sensor data.	R/W	0x0306	R	0x0000
FPARSTBAND	10	Anti-blooming. Number of pixel rows to reset on each side of the row to be returned.	R/W	0x030A	R	0x0000
FPARSTTIME	16	Count represents the time required to reset rows given FPARSTBAND. Requirement: ensure count is at least 5 more than actual time required. (LSB = 83.3 ns; max count = 5.46 ms)	R/W	0x030B	R	0x0000
FPAROWTIME	16	Count represents the time required to read one complete row (includes row select and row read times) given the current block and step sizes. Requirement: ensure count is at least 5 more than actual time required. (LSB = 83.3 ns; max count = 5.46 ms)	R/W	0x0307	R	0x0000
FPAINTTIME	16	Pixel integration time; integer multiple of	R/W	0x0308	R	0x0000

		FPAROWTIME				
FPAPIXELADDR	16	Current address of pixels written to memory. Used for a status count; offset by FPAMEMOFFSET.	R	0x0309	R/W	0x0000
FRTCSR	2	Free Running Timer control Bit 0: Set bit to reset FRT (CTRL) Bit 1: Select 20 Hz Clock A or B (A=0, B=1) (CTRL)	R/W	0x0400	R/W	0x00
FRT	16	Free Running Timer Count (16 bit) LSb resolution = 100 us.	R	0X0401	R/W	0x00
FRT_SYNC_REG	16	Free Running Timer Count (16 bit) LSb resolution = 100 us. Registered on the falling edge of the 20Hz clock.	R	0X0402	R/W	0x00
WDCSR	1	Watchdog Timer control Timeout at 1.5 seconds, then resets uController. Bit 0: Set bit to reset within 1.5 sec When reading from the CSR, if bit 0 is set, then there was a watchdog reset. Note: a read resets bit 0.	R/W	0x0700	R/W	0x00
MODE_FLIP	1	Switches instruction address 0h from PROM to SRAM. Write 0x3333h to switch to SRAM mode (uC RESET follows). Write 0xCCCCh to switch to PROM mode (uC RESET follows). Read to get current mode (0=PROM, 1=SRAM). A watchdog timeout resets to PROM mode.	R/W	0x1000	R/W	0x00
FPGAVER	16	FPGA Version. Specifies the vhdl code revision Bit [15:12] : MONTH Bit [11:7] : DAY Bit [6:3] : YEAR Bit [2:0] : BURN NUMBER	R	0x8000	R	0x00
TESTBUS	2	Software Test Register. Outputs brought out to board.	R/W	0x8010	R	0x00

Table 2 Sun Sensor Register Definition

11.6.2 Sun Sensor FPA Integration Timing

FPA Registers Description

The FPACSR is a 9-bit control and status register with the following definitions:

- Bit 0 – FPARST_H : This bit takes precedence over all other bits. It resets the FPA Controller to a known state. This bit acts like an asynchronous reset. Write a '1' to this bit to set the reset, and a '0' to remove.

- Bit 1 – PIXRST_H : This bit is used in conjunction with the start transfer bit, START_H. When a transfer is initiated using START_H, if PIXRST_H is set, '1', then FPA rows Y1 through Y2 are reset. No other action is performed. For normal operation, set to '0'.

- Bit 2 – START_H : Set this bit to initiate the FPA transfer only after all the other configuration registers are setup. The busy bit, RDY_H, will be set throughout the duration of the transfer.

- Bits 4,3 – FPA_G[1:0] : Bits 3 and 4 are the amplifier gain for the onboard ADC. Bit 4 is the most significant bit and Bit 3 is the least significant. When the 2-bit value is '00' the gain is 1x, '01' is 2x, '10' is 4x, and '11' is 8x.

- Bit 5 – FPABITINVERT_L : Bit 5 is used to invert the output bits from the onboard ADC. Set to '0' to invert the bits and '1' for normal operation.

- Bit 6 – RDY_L : The RDY_L bit indicates a FPA transfer is currently in progress. When '0', the FPA is ready, when '1', the FPA is busy.

- Bit 7 – ERR_BLK_SIZE_H : This is an error condition bit that represents an error in the configuration registers, but will not prevent an attempted data transfer from the FPA. When Bit 7 is set, this means that either FPAX1 > FPAX2 or FPAY1 > FPAY2 or both.

- Bit 8 – ERR_STEP_SIZE_H : This is an error condition bit that represents an error in the FPASTEPSIZE configuration register, but will not prevent an attempted data transfer from the FPA. The Y (row) step size is the most significant byte (MSB) and the X (column) step size is the least significant byte (LSB). If the MSB or LSB is equal to '0', this bit is set, and the FPASTEPSIZE register is reset with the value 0x0101, then the transfer is completed.

FPA configuration registers FPAX1, FPAX2, FPAY1, and FPAY2 are 10-bit registers that define the rectangular coordinates for a block (or window) of pixels. The FPASTEPSIZE register is a 16-bit register that defines the increment step size for the column and row addressing. The MSB defines the row (or Y) step size and the LSB defines the column (or X) step size. The

FPAMEMOFFSET register is also 16-bits and defines a memory offset where to place the pixel data in operand memory. The FPA interface DMAs its pixel data beginning at FPAMEMOFFSET in the upper 64K of operand SRAM.

FPARSTBAND is a 10-bit register to define the number of rows outside the defined rectangular block of pixels that should be reset during the FPA pixel data transfer. This option helps reduce the effects of blooming. Blooming is defined as the bleed over of electrons to adjacent rows, causing pixels to appear falsely illuminated.

Related to FPARSTBAND is the FPARSTTIME register. This is a 16-bit register that represents the time (in system clock cycles) to reset the rows given the number in FPARSTBAND. This register needs to be configured with an additional 5 clock cycles for a safeguard to account for calculation timing in the FPGA.

FPAROWTIME is a 16-bit register that contains the time (in system clock cycles) required to return the data in one row within the defined rectangular block (FPAX1 – FPAX2) and dependent on the configured column step size (LSB of FPASTEPSIZE). This register needs to be configured with an additional 5 clock cycles for a safeguard to account for calculation timing in the FPGA.

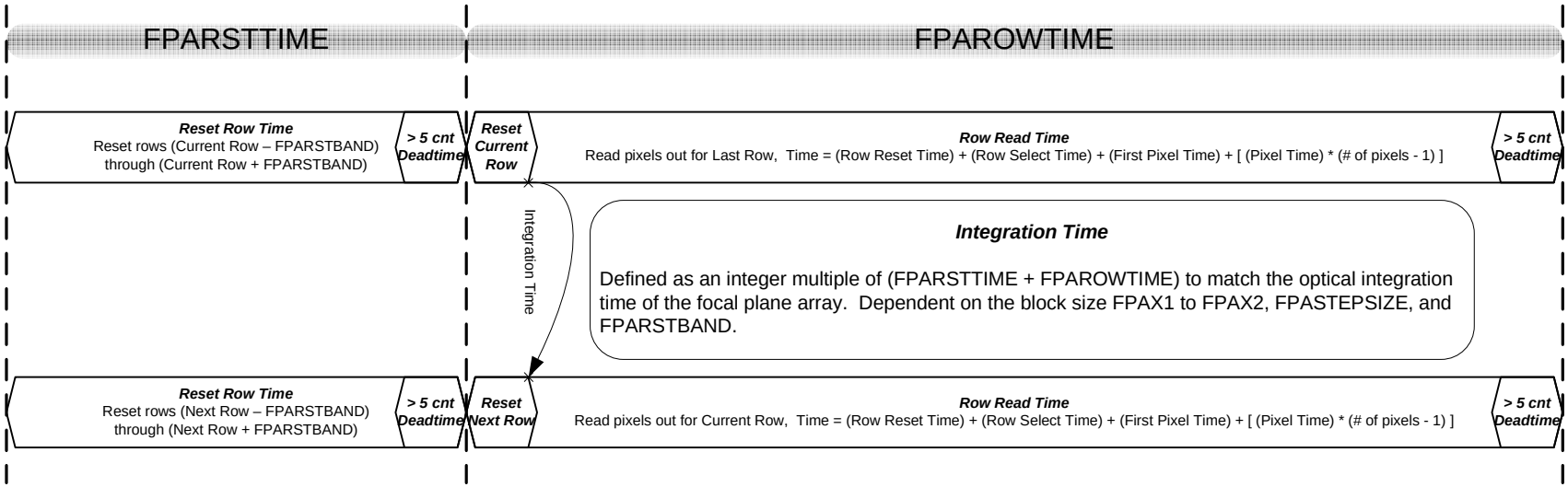
FPAINTTIME controls the integration time for the pixels. Simply defined, the value is an integer multiple of the sum of FPARSTTIME and FPAROWTIME (see Figure 79).

FPA Registers Calculation (all numbers in decimal)			
FPAX1	1	Block Transfer Time (µs)	
FPAX2	1023		
FPAY1	0	**5646.83**	
FPAY2	1023		
stepsize_x	8		
stepsize_y	8	Integration Time (µs)	
FPASTEPSIZE	2056		
FPAINTTIME	7	**296.83**	
FPARSTBAND	8		
# row pixels (X1 - X2)	128		
# of rows (Y1 - Y2)	128	FPARSTTIME	FPAROWTIME
# total pixels (64k max)	16384		
(# of clock cycles)			
row reset	8	142	358
row select	77		
first pixel	11		
pixel	2		
deadband	6		
row select offset	44		
row reset offset	4		
state machine offsets	2		

Table 3 FPA Registers Calculation Aid

Table 3 is a spreadsheet to aid the software team configure the FPA registers. The optical team for the SOFIE instrument designed their system such that 300 µs of sunlight should fill 80% of the well capacity for the STAR-1000 (135,000 electrons). Thus each unique block size of pixels needs to use the spreadsheet to adjust settings to match an integration time of 300 µs ± 10 µs. Shaded areas in the table are fixed or calculated values, the other cells must be configured (block size, integration time, and reset band). In addition, the spreadsheet calculates how long the transfer will take (from the FPA to SRAM). This is labeled 'Block Transfer Time (µs)' in the table.

FPAPIXELADDR is a register the user can read during the FPA data transfer to determine the status/progress. After properly configuring all the FPA registers for a block data transfer, the START_H bit is set to begin the transfer. The first pixel data to be returned is written to upper SRAM plus the FPAMEMOFFSET value. FPAPIXELADDR contains the current address of the pixels and is incremented after each memory write. The user can calculate the status/progress of the transfer by using this value.



FPA Timing		Timing Details
Row Reset	667 ns	From row_reset_go_h to row_reset_done_h.
Row Select	6,417 ns	From start of row select to start of row read.
First Pixel	917 ns	Due to pipeline….from row_read_go_h to FPADAT loaded.
Pixel	167 ns	Two clock cycles per pixel.

Figure 79 Sun Sensor FPA Integration Timing

STAR-1000

The FPA is a radiation-hardened CMOS image sensor. Because the STAR-1000 is built on CMOS technology (an active pixel image sensor), there a couple of advantages over charge-coupled device (CCD) image sensors. First, each pixel on the STAR-1000 can be addressed individually, just like a memory device. Because of this, the STAR-1000 allows the user to output 'windows' or sections of the entire focal plane array based on need. Second, because the device is built on CMOS technology, integrated peripherals are available. The STAR-1000 has a 10-bit analog-to-digital converter (ADC), a programmable gain amplifier, and fixed pattern noise correction onboard.

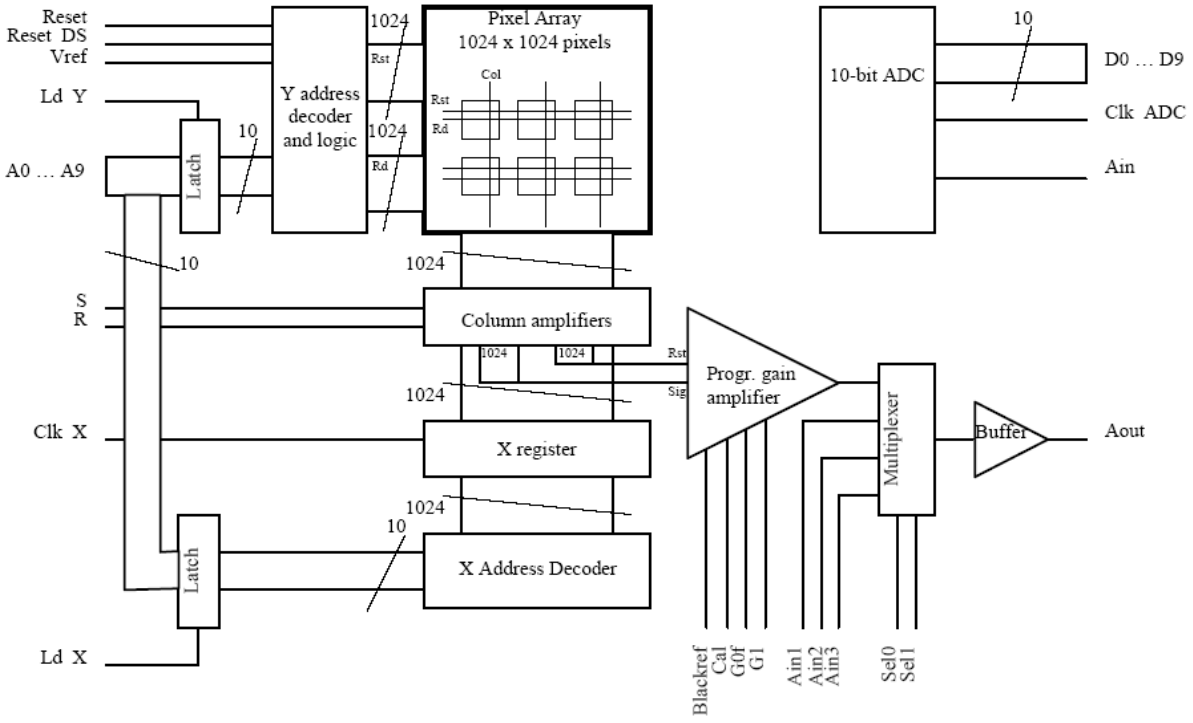


Figure 80 Block diagram of the FillFactory STAR-1000 CMOS Image Sensor

The pixels are arranged as 1,024 rows by 1,024 columns with a 10-bit address bus. To address an individual pixel, first the row address (Y) is latched. After latching the row address, the pixel outputs are connected to the column amplifiers. Next, a sequence of pulses with specific timing is required to sample the pixels (S pulse), reset the pixels (Reset pulse) in that row, and sample the reset signal (R pulse). This process requires 6 – 7 µs, depending on clock rate, and is the most time consuming part of accessing the FPA. The pixel integration time is defined as the time from when the row is reset until the row is sampled again.

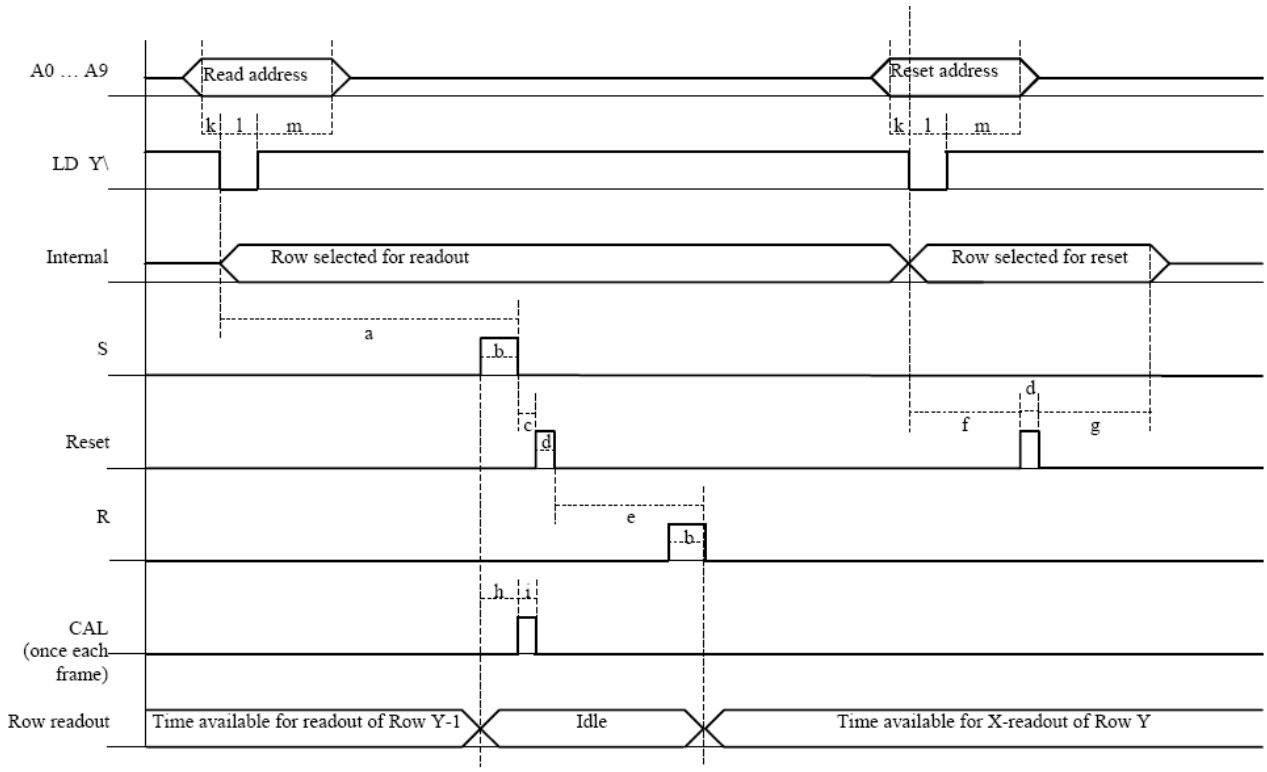


Figure 81 STAR-1000 row selection and reset timing

Symbol	Min.	Typ.	Description
a	3.6 µs		Delay between selection of a new row and falling edge on S. Minimal value: For maximum speed a new row can already be selected during X-readout of the previous row.
b	0.4 µs		Duration of S and R pulse.
c	0	100 ns	Delay between falling edge of S and rising edge of Reset.
d	200 ns		Minimum duration of Reset pulse.
e	1.6 µs		Delay between falling edge of Reset and falling edge of R.
f	0	100 ns	Minimum delay between falling edge on LD_Y and rising edge of Reset.
g		100 ns	Minimum required extension of Y-address after falling edge of reset pulse.
h	100 ns	200 ns	Position of Cal pulse after rising edge of S. The cal pulse must only be given once per frame.
i	100 ns	1 µs	Duration of Cal pulse.
k	10 ns		Address set-up time.
l	20 ns		Load register value.
m	10 ns		Address stable after load.

Table 4 STAR-1000 row selection and reset timing constraints

Next the column address (X) is latched. Following the decoding of the column address, another pulse (CLK-X) is used to load the column selection address into a register and also to subtract the pixel output level from the reset level (double sampling correction). This causes a pipeline delay before the signal level is present at the device output and ready for conversion. The ADC pulse (CLK-ADC) is used to tell the onboard ADC when to convert. The resultant value is returned on a 10-bit data bus. Pixels can be read out along a row at up to 12 MHz.

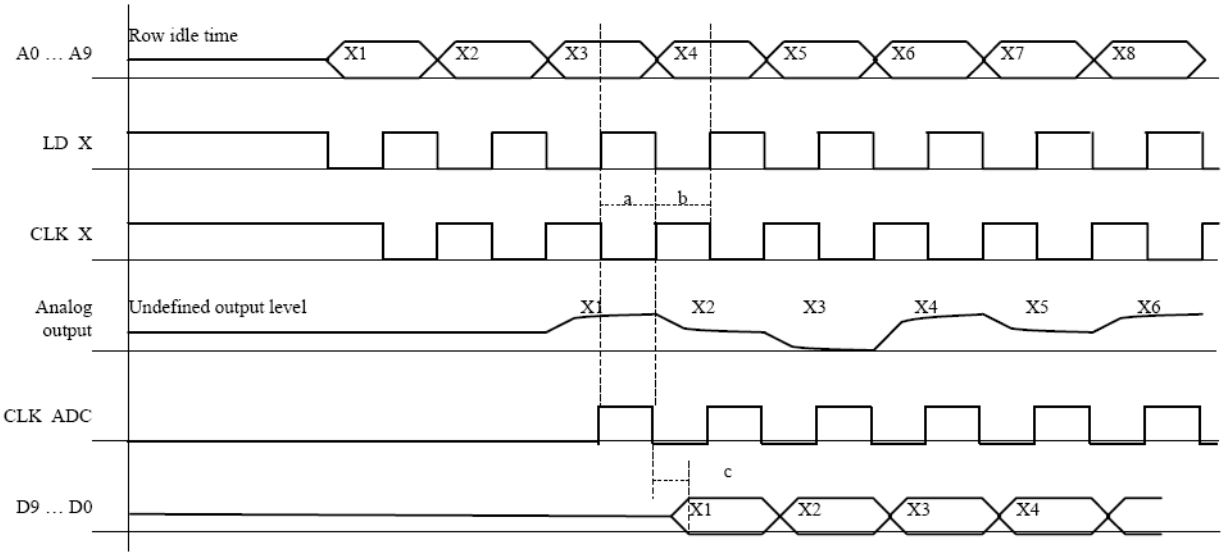


Figure 82 STAR-1000 column selection and row readout

Symbol	Min	Typ	Description
a	40 ns		Address setup time
b	40 ns		Address valid time
c	0	20 ns	ADC output valid after falling edge of CLK_ADC

Table 5 STAR-1000 column selection and row readout timing constraints

The STAR-1000 requires a black reference voltage level. The data sheet recommends a level of 2.0V. To fulfill this requirement the Analog Devices AD584TH/883B Precision Voltage Reference is used.

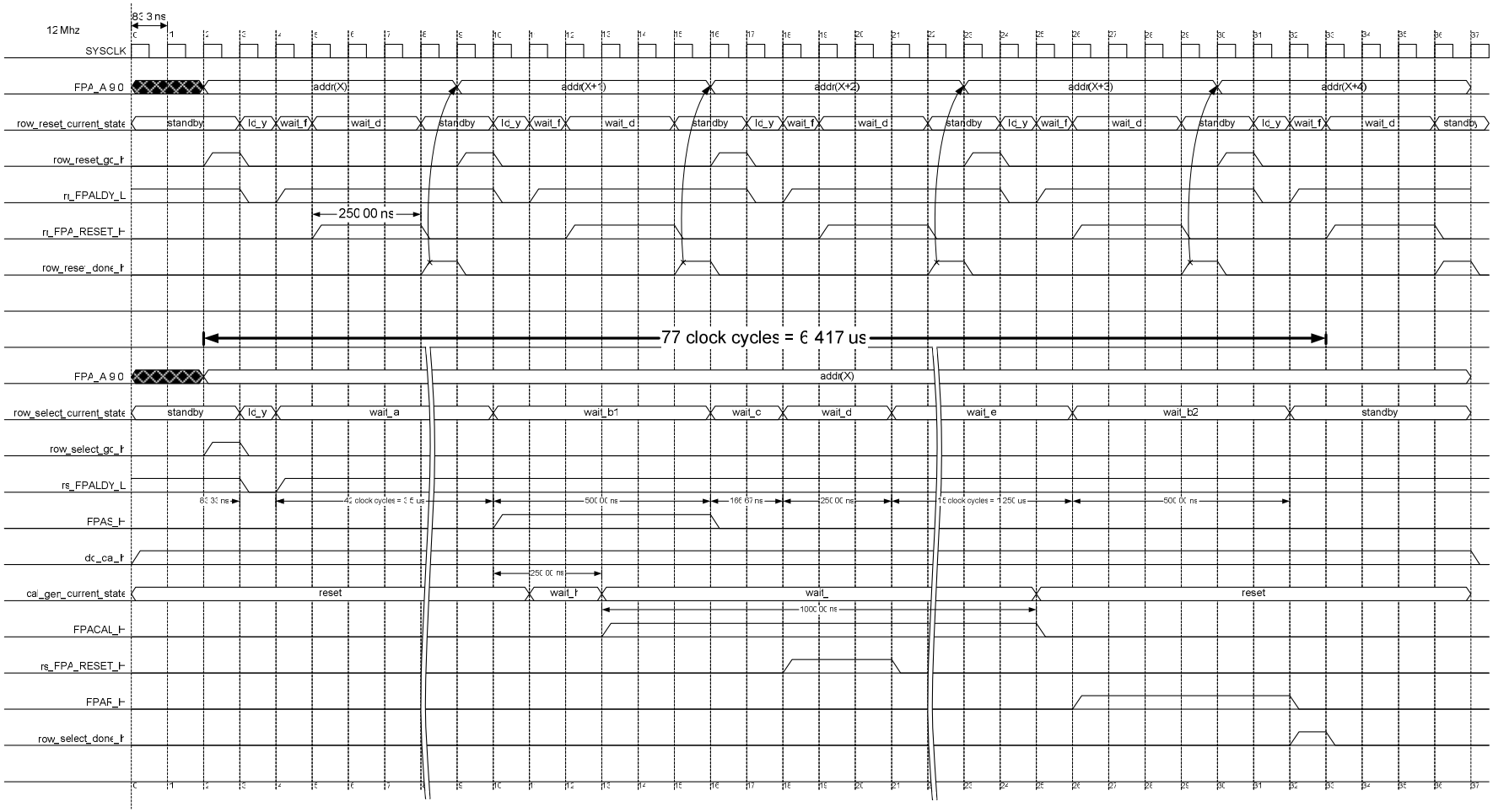


Figure 83 Row Timing for the STAR-1000 CMOS Image Sensor

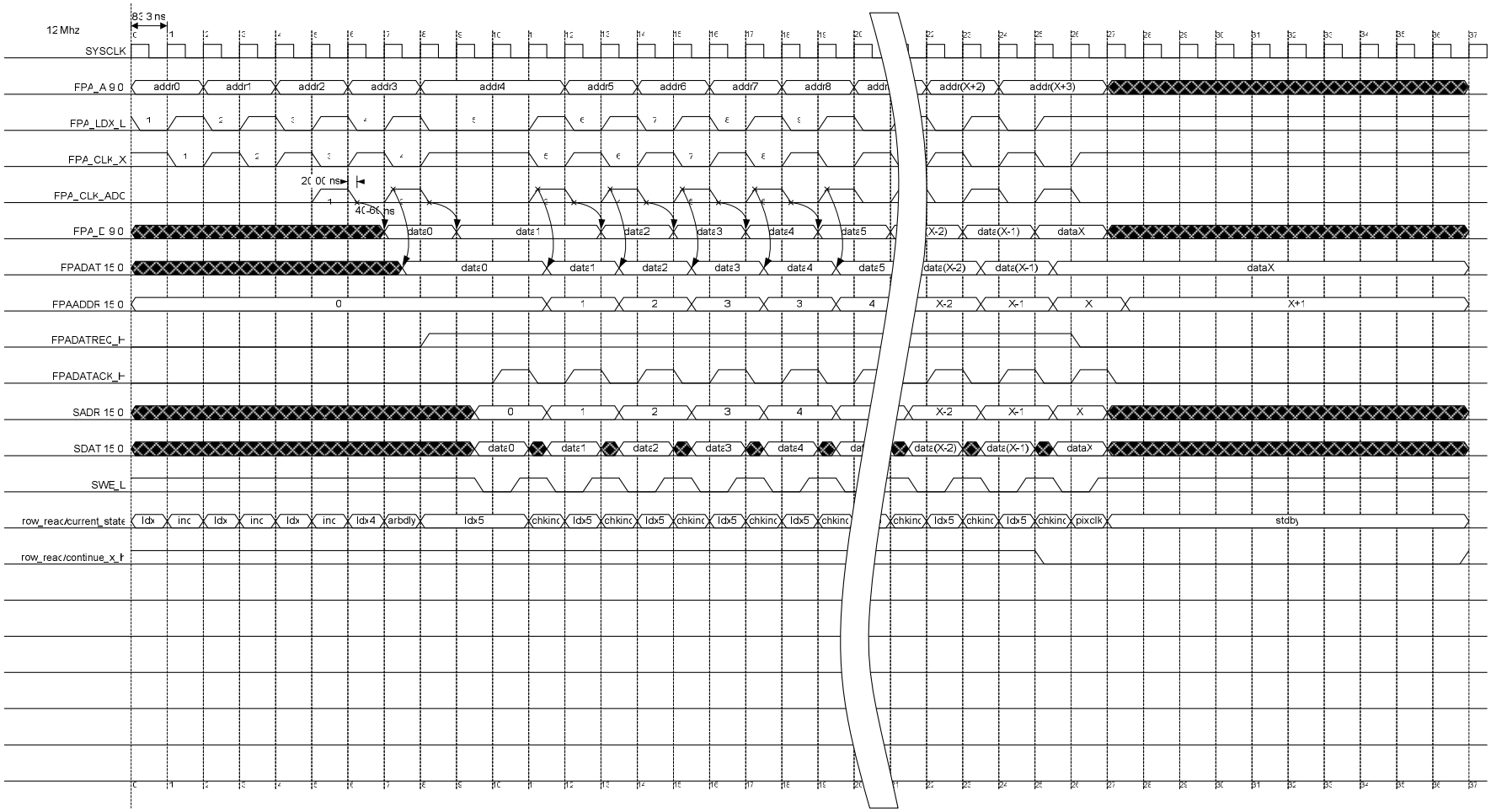


Figure 84 Column (pixel) Timing for the STAR-1000 CMOS Image Sensor

11.7 C&DH Processor Hardware/Software Interface

The Command and Data Handling microcontroller interfaces with multiple components within the SOFIE system. The C&DH Memory Architecture / Programmers Model is shown in Figure 85. This diagram shows the processing and storage elements comprising the C&DH Process System. The C&DH System is composed of:

- 16-bit radiation-hardened microcontroller, the Aeroflex/UTMC UT69R000
- Instruction Memory
- Data/Operand Memory
- Processor Bus Arbiter
- external registers implemented in an FPGA
- Watch Dog Timer
- RS-422 Communication Interfaces
- RS-422 Microcontroller Serial Monitor Port.
- 1553 Communication Interface.

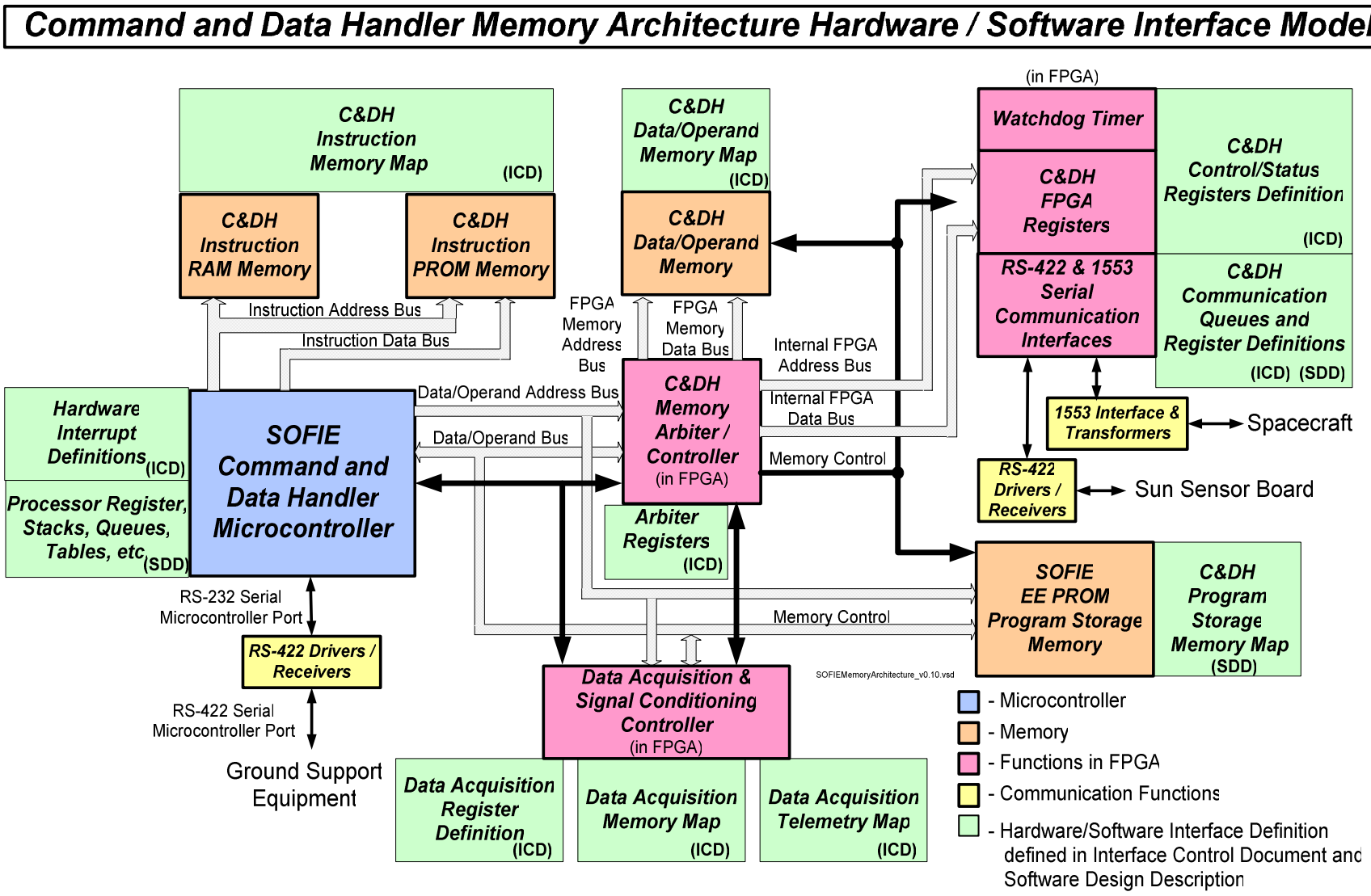


Figure 85 C&DH Processor Programmer Model

11.7.1 C&DH Processor Memory Maps

The memory bank selection is described below and the C&DH Memory Map is shown in Figure 86.

Data Memory Bank Select

Note: operand SRAM (lower 64k) is permanently mapped to the microcontroller's memory address space. For access to other memory regions, the microcontroller needs to use the port I/O instruction and select the region by using the Output Discrete bus (OD(7:0)) as defined in Figure 87.

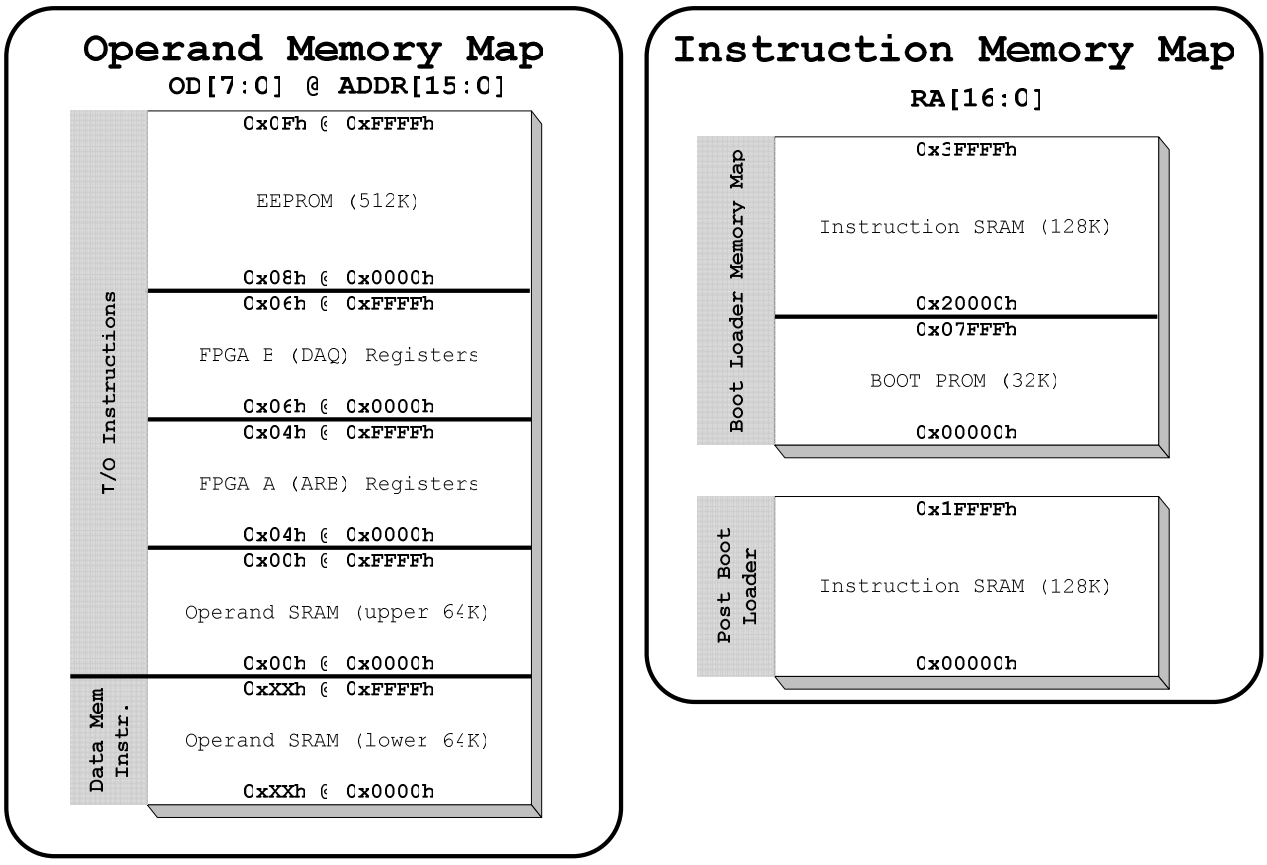


Figure 86 C&DH Memory Map

Data Memory Bank Select

Note: Operand SRAM (lower 64k) is permanently mapped to the microcontroller's memory address space. For access to other memory regions, the microcontroller needs to use the M/IO instruction and select the region by using the Output Discrete bus (OD[7:0]) according to the following table.

OD[7:0]	Bank
0x00h	Upper 64K of Operand SRAM
0x04h	ARB FGPA Reg
0x06h	DAQ FPGA Reg
0x08h	EEPROM 1
0x09h	EEPROM 2
0x0Ah	EEPROM 3
0x0Bh	EEPROM 4
0x0Ch	EEPROM 5
0x0Dh	EEPROM 6
0x0Eh	EEPROM 7
0x0Fh	EEPROM 8

Figure 87 C&DH Processor Memory Bank Map

INTERRUPT NUMBER	DESCRIPTION	
0 (Highest Priority)	Power-Down Interrupt, Cannot be masked or disabled.	**Implemented Not Used**
1	Machine Error. Cannot be disabled.	**Spurious Interrupt Handler**
2	INT0. External user interrupt.	**20 HZ Interrupt A**
3	Software interrupt (USR3).	**Spurious Interrupt Handler**
4	Fixed-point overflow (V bit).	**Spurious Interrupt Handler**
5	Software interrupt (USR2).	**Implemented Not Used**
6	Software interrupt (USR1).	**Spurious Interrupt Handler**
7	Timer A (If implemented).	**Used for timing generation**
8	INT1. External user interrupt.	**20 HZ Interrupt B**
9	Timer B (If implemented).	**Used for timing generation**
10	INT2. External user interrupt.	**Spurious Interrupt Handler**
11	INT3. External user interrupt.	**Spurious Interrupt Handler**
12	INT5. External user interrupt.	**Spurious Interrupt Handler**
13	INT4. External user interrupt.	**Spurious Interrupt Handler**
14 (Lowest Priority)	INT6. External user interrupt.	**Spurious Interrupt Handler**

Table 6 C&DH Microcontroller Interrupt Definition

11.7.2 C&DH Processor Register definitions

ARB FPGA Registers (OD[7:0] = 0x04)						
Register Name	**Size (bits)**	**Description**	**CPU**	**Address**	**FPGA**	**Reset Value**
PIN_PULL	4	Pin puller release mechanism return side enables: Bit 0-2: Pin Puller "000" Nothing Asserted "001" APTRLS_PWR1A Asserted "010" APTRLS_PWR1B Asserted "011" APTRLS_PWR2A Asserted "100" APTRLS_PWR2B Asserted Bit 3 - Aperature_Open_H monitor (Read Only) Bit 4-15: Reserved	R/W	0x0001	R	0x0
SEC_HI_CNT	16	Hi 16 bits of 32 bit wide "Seconds" counter. The output of the "Seconds" counter is latched into this register on the falling edge of the 20Hz clock. The "Seconds" counter is corrected to space craft time at each 1 second TIC update. The "Seconds" counter increments with a carry input from the "Sub-Second" counter.	R	0x1303	R/W	0x00
SEC_LO_CNT	16	Low 16 bits of the 32 bit wide "Seconds" counter.	R	0x1302	R/W	0x00
SUBSEC_HI_CNT	16	Hi 16 bits of 32 bit wide "Sub-Second" counter. The output of the "Seconds" counter is latched into this register on the falling edge of the 20Hz clock. The "Seconds" counter is corrected to spacecraft time at each 1 second TIC update. The "Sub-Second" counter adds 100 usec to "Sub-Second" time every 100 usec.	R	0x1301	R/W	0x00
SUBSEC_LO_CNT	16	Low 16 bits of the 32 bit wide "Sub-Second" counter.	R	0x1300	R/W	0x00
FRTCSR	2	Free Running Timer control Bit 0: Set bit to reset FRT (CTRL) on the next neg. edge 20Hz signal Bit1: Reserved for the C&DH board.	R/W	0x0400	R/W	0x00
FRT	16	A free running timer used to synchronize the different SOFIE components. LSB = 100 usec	R	0x0401	R/W	0x00

ARB FPGA Registers (OD[7:0] = 0x04)						
Register Name	**Size (bits)**	**Description**	**CPU**	**Address**	**FPGA**	**Reset Value**
FRT_SYNC_REG	16	FRT is latched into this location every neg. edge on the 20Hz signal. This value is reset on a FRT reset via the FRTCSR.	R	0x0402	R/W	0x00
SYNC_NEXT_REG	4	Signal the SSG Board to reset its Free Running Timers on the next neg. 20Hz clock edge. Write all ones to this register.	R/W	0x0403	R	0x00
WDCSR	1	Watchdog Timer control Bit 0: Set bit to reset WDT (CTRL)	W	0x0700	R/W	0x00
WD_TIME	16	Shows current 100us time of the WatchDog The WatchDog timer counts down from 0x3E80 to zero (1.6 seconds), emits a 2.67 usec reset signal to the microcontroller, then starts counting down again from 0x3E80.	R	0x0701	R	0x3EF0
MODE_FLIP	1	Switches instruction PROM at address 0h to instruction SRAM at address 0h (tristates PROM). Write 0x3333h to register to switch mode (RESET follows). Read register to get current mode (0=PROM, 1=SRAM).	R/W	0x1000	R	0x00
FFTHCSR	4	1553 Configuration and Status Register Bit 3: if 1 then a 1553 TX has occurred, read to clear Bit2: if 1 then a 1553 RX has occurred, read to clear Bit1: if 1 then the 1553 memory interface has failed Bit0: Set to a 1 to enable Shutdown transmitter Mode code	R/W	0x1500	R/W	0x00
SRAM_BLK_REG	4	Sets the 4 MSBs of SRAM address block used for 1553 Bus information. The 1553 buffer size is a potentially 4k words.	R/W	0x1501	R	0x00
TEL_POL	16	Telemetry Poll Register. Counts down one per 1553 message transmitted on 1553 Sub Address 0x04.	R/W	0x1502	R/W	0x00
CRIT_TEL_POL	16	Critical Telemetry Poll Register. Counts down one per 1553 message transmitted on 1553 Sub Address 0x06.	R/W	0x1503	R/W	0x00
TEL_MSG_CNT	16	Telemetry Up Counter that increments by one for every 1553 message that is transmitted from the Telemetry buffer.	R/W	0x1504	R/W	0x00
CRIT_TEL_MSG_CNT	16	Critical Telemetry Up Counter that increments by one for every 1553 message that is transmitted from the Critical Telemetry buffer.	R/W	0x1505	R/W	0x00

ARB FPGA Registers (OD[7:0] = 0x04)						
Register Name	**Size (bits)**	**Description**	**CPU**	**Address**	**FPGA**	**Reset Value**
TEL_BUF_CNT	16	Telemetry down counter that is settable by the Microcontroller. The counter is decremented by transmitting a 1553 message from the Telemetry buffer.	R/W	0x1506	R/W	0x00
CRIT_TEL_BUF_CNT	16	Critical Telemetry down counter that is settable by the Microcontroller. The counter is decremented by transmitting a 1553 message from the Critical Telemetry buffer.	R/W	0x1507	R/W	0x00
CMD_1_COUNTER	16	Running count of successful Command 1 MESSAGE transfers received from spacecraft.	R	0x1508	R/W	0x00
CMD_2_COUNTER	16	Running count of successful Command 2 MESSAGE transfers received from spacecraft.	R	0x1509	R/W	0x00
TAT_COUNTER	16	Running count of successful Time at Tick MESSAGE transfers received from spacecraft.	R	0x150A	R/W	0x00
ACS_COUNTER	16	Running count of successful ACS MESSAGE transfers received from spacecraft.	R	0x150B	R/W	0x00
FFTHADR	16	Memory Address of the Last 1553 Transaction	R	0x150C	R/W	0x00
FFTHRXDAT	16	Data from the Last 1553 Receive Transaction	R	0x150D	R/W	0x00
FFTHTXDAT	16	Data from the Last 1553 Transmit Transaction	R	0x150E	R/W	0x00
FPGAVER	16	FPGA Version. Specifies the vhdl code revision BITS 15 - 12 = MONTH BITS 11 - 7 = DAY BITS 6 - 3 = YEAR BITS 2 - 0 = BURN NUMBER	R	0x8000	R	0x00
TESTBUS	4	Software Test Register. Outputs brought out to board.	R/W	0x8010	R	0x00

ARB FPGA Registers (OD[7:0] = 0x04)						
Register Name	**Size (bits)**	**Description**	**CPU**	**Address**	**FPGA**	**Reset Value**
UARTCSR	7	UART status/control Bit 0: Set bit to reset UART (CTRL) Bit 1: RCV Ch A or B (A=0, B=1)(CTRL) Bit 2: Parity Error (Status) Bit 3: Framing Error (Status) Bit 4: RCV Dead Time (Status) Bit 5: RCV Busy (Status) Bit 6: XMIT Busy (Status)	R/W	0x0100	R/W	0x00
UARTXMITADDR	7	UART XMIT buffer memory location: ADDR[15:9]	R/W	0x0101	R	0x00
UARTRCVADDR	7	UART RCV buffer memory location: ADDR[15:9]	R/W	0x0102	R	0x00
UARTXMITWPTR	9	UART XMIT write buffer pointer address ADDR[8:0]	R/W	0x0103	R	0x00
UARTXMITRPTR	9	UART XMIT read buffer pointer address ADDR[8:0]	R	0x0104	R/W	0x00
UARTRCVWPTR	9	UART RCV write buffer pointer address ADDR[8:0]	R	0x0105	R/W	0x00
EEREG	3	EEPROM status/control Bit 0: Set to allow EEPROM to read or write. Wait 1 sec. Bit 1: Low EEPROM Status. Ready: Set, Busy: Reset Bit 2: High EEPROM Status. Ready: Set, Busy: Reset Bit 3: Feedback Status from EEPROM Supervisory Chip. Ready: Set, Disabled: Reset	R/W	0x0800	R/W	0x00
Total FFs:	246					

SRAM Registers (Lower SRAM Memory, Accessed through Data Memory Instructions) These addresses are offsets from the value specified SRAM_BLK_REG. SRAM_BLK_REG provides the upper 5-bits of the 16-bit memory address.						
Register Name	**Size (bits)**	**Description**	**CPU**	**Address**	**FPGA**	**Reset Value**
CMD1_STAT	16	CMD1 MESSAGE TRANSFER STATUS WORD	R/W	0x0C01	R/W	0x00
CMD2_STAT	16	CMD2 MESSAGE TRANSFER STATUS WORD	R/W	0x0C02	R/W	0x00
TAT_STAT	16	TIME AT TICK MESSAGE TRANSFER STATUS WORD	R/W	0x0C03	R/W	0x00
ACS_STAT	16	ACS MESSAGE TRANSFER STATUS WORD	R/W	0x0C04	R/W	0x00
TEL_POL_STAT	16	TELEMETRY POLL MESSAGE TRANSFER STATUS WORD	R/W	0x0E03	R/W	0x00
TEL_STAT	16	TELEMETRY MESSAGE TRANSFER STATUS WORD	R/W	0x0E24	R/W	0x00
CRIT_TEL_POL_STAT	16	CRITICAL TELEMETRY POLL MESSAGE TRANSFER STATUS WORD	R/W	0x0E05	R/W	0x00
CRIT_TEL_STAT	16	CRITICAL TELEMETRY MESSAGE TRANSFER STATUS WORD	R/W	0x0526	R/W	0x00
TEL_1	512	TELEMETRY CCSDS MESSAGE #1	R/W	0x0000 - 0x001F	R/W	0x00
TEL_2	512	TELEMETRY CCSDS MESSAGE #2	R/W	0x0020 - 0x003F	R/W	0x00
TEL_3	512	TELEMETRY CCSDS MESSAGE #3	R/W	0x0040 - 0x005F	R/W	0x00
TEL_4	512	TELEMETRY CCSDS MESSAGE #4	R/W	0x0060 - 0x007F	R/W	0x00
TEL_5	512	TELEMETRY CCSDS MESSAGE #5	R/W	0x0080 - 0x009F	R/W	0x00
TEL_6	512	TELEMETRY CCSDS MESSAGE #6	R/W	0x00A0 - 0x00BF	R/W	0x00
TEL_7	512	TELEMETRY CCSDS MESSAGE #7	R/W	0x00C0 - 0x00DF	R/W	0x00
TEL_8	512	TELEMETRY CCSDS MESSAGE #8	R/W	0x00E0 - 0x00FF	R/W	0x00
TEL_9	512	TELEMETRY CCSDS MESSAGE #9	R/W	0x0100 - 0x011F	R/W	0x00
TEL_10	512	TELEMETRY CCSDS MESSAGE #10	R/W	0x0120 - 0x013F	R/W	0x00
TEL_11	512	TELEMETRY CCSDS MESSAGE #11	R/W	0x0140 - 0x015F	R/W	0x00

SRAM Registers (Lower SRAM Memory, Accessed through Data Memory Instructions) These addresses are offsets from the value specified SRAM_BLK_REG. SRAM_BLK_REG provides the upper 5-bits of the 16-bit memory address.						
Register Name	**Size (bits)**	**Description**	**CPU**	**Address**	**FPGA**	**Reset Value**
TEL_12	512	TELEMETRY CCSDS MESSAGE #12	R/W	0x0160 - 0x017F	R/W	0x00
TEL_13	512	TELEMETRY CCSDS MESSAGE #13	R/W	0x0180 - 0x019F	R/W	0x00
TEL_14	512	TELEMETRY CCSDS MESSAGE #14	R/W	0x01A0 - 0x01BF	R/W	0x00
TEL_15	512	TELEMETRY CCSDS MESSAGE #15	R/W	0x01C0 - 0x01DF	R/W	0x00
CRIT_TEL_1	512	CRITICAL TELEMETRY CCSDS MESSAGE #1	R/W	0x0200 - 0x021F	R/W	0x00
CRIT_TEL_2	512	CRITICAL TELEMETRY CCSDS MESSAGE #2	R/W	0x0220 - 0x023F	R/W	0x00
CRIT_TEL_3	512	CRITICAL TELEMETRY CCSDS MESSAGE #3	R/W	0x0240 - 0x025F	R/W	0x00
CRIT_TEL_4	512	CRITICAL TELEMETRY CCSDS MESSAGE #4	R/W	0x0260 - 0x027F	R/W	0x00
CRIT_TEL_5	512	CRITICAL TELEMETRY CCSDS MESSAGE #5	R/W	0x0280 - 0x029F	R/W	0x00
CRIT_TEL_6	512	CRITICAL TELEMETRY CCSDS MESSAGE #6	R/W	0x02A0 - 0x02BF	R/W	0x00
CRIT_TEL_7	512	CRITICAL TELEMETRY CCSDS MESSAGE #7	R/W	0x02C0 - 0x02DF	R/W	0x00
CRIT_TEL_8	512	CRITICAL TELEMETRY CCSDS MESSAGE #8	R/W	0x02E0 - 0x02FF	R/W	0x00
CRIT_TEL_9	512	CRITICAL TELEMETRY CCSDS MESSAGE #9	R/W	0x0300 - 0x031F	R/W	0x00
CRIT_TEL_10	512	CRITICAL TELEMETRY CCSDS MESSAGE #10	R/W	0x0320 - 0x033F	R/W	0x00
CRIT_TEL_11	512	CRITICAL TELEMETRY CCSDS MESSAGE #11	R/W	0x0340 - 0x035F	R/W	0x00
CRIT_TEL_12	512	CRITICAL TELEMETRY CCSDS MESSAGE #12	R/W	0x0360 - 0x037F	R/W	0x00
CRIT_TEL_13	512	CRITICAL TELEMETRY CCSDS MESSAGE #13	R/W	0x0380 - 0x039F	R/W	0x00
CRIT_TEL_14	512	CRITICAL TELEMETRY CCSDS MESSAGE #14	R/W	0x03A0 - 0x03BF	R/W	0x00
CRIT_TEL_15	512	CRITICAL TELEMETRY CCSDS MESSAGE #15	R/W	0x03C0 - 0x03DF	R/W	0x00
CMD1_1	512	COMMAND 1 CCSDS MESSAGE #1	R/W	0x0400 - 0x041F	R/W	0x00
CMD1_2	512	COMMAND 1 CCSDS MESSAGE #2	R/W	0x0420 - 0x043F	R/W	0x00

SRAM Registers (Lower SRAM Memory, Accessed through Data Memory Instructions) These addresses are offsets from the value specified SRAM_BLK_REG. SRAM_BLK_REG provides the upper 5-bits of the 16-bit memory address.						
Register Name	**Size (bits)**	**Description**	**CPU**	**Address**	**FPGA**	**Reset Value**
CMD1_3	512	COMMAND 1 CCSDS MESSAGE #3	R/W	0x0440 - 0x045F	R/W	0x00
CMD1_4	512	COMMAND 1 CCSDS MESSAGE #4	R/W	0x0460 - 0x047F	R/W	0x00
CMD2_1	512	COMMAND 2 CCSDS MESSAGE #1	R/W	0x0600 - 0x061F	R/W	0x00
CMD2_2	512	COMMAND 2 CCSDS MESSAGE #2	R/W	0x0620 - 0x063F	R/W	0x00
CMD2_3	512	COMMAND 2 CCSDS MESSAGE #3	R/W	0x0640 - 0x065F	R/W	0x00
CMD2_4	512	COMMAND 2 CCSDS MESSAGE #4	R/W	0x0660 - 0x067F	R/W	0x00
TIME_AT_TICK	512	TIME AT TICK MESSAGE	R/W	0x0800 - 0x08E9	R/W	0x00
ACS	512	ACS MESSAGE	R/W	0x0A00 - 0x0A1F	R/W	0x00

DAQ FPGA Registers (OD[7:0] = 0x06)						
Register Name	**Size (bits)**	**Description**	**CPU**	**Address**	**FPGA**	**Reset Value**
MAINCSR	16	Main control and status register: Bit 0: RSTSYNC_H, Resets Sync. Rectification Controller Bit 1: RSTDAS_H, Resets Data Acquisition Subsystem Bit 2: RSTBAL_H, Resets Balance Controller Bit 3: DAQTESTMODE_H, Fills DAQ memory with Address values Bit 7:4: TEST_PORTA, Test Port for Software Bit 15:8: Version Control Identification, (Read Only) Initial Release = 01 Next Release = 02 (etc.)	R/W	0x0000	R/W	0x0000
PINPULL_RTN	3	Pin puller release mechanism return side enables: Bit 0-2: Pin Puller "000" Nothing Asserted "001" APTRLS_RTN1A Asserted "010" APTRLS_RTN1B Asserted "011" APTRLS_RTN2A Asserted "100" APTRLS_RTN2B Asserted Bit 3-15: Reserved	R/W	0x0001	R	0x00

DAQ FPGA Registers (OD[7:0] = 0x06)						
Register Name	**Size (bits)**	**Description**	**CPU**	**Address**	**FPGA**	**Reset Value**
BALANCE	16	Channel #1-16 Balance Attenuation Setting BALDAT[15:12], Balance Attenuation Channel Address BALDAT[11:0], Balance Attenuation Data Balance Attenuation Channel Address Definition: "0000" = Detector #1 "0001" = Detector #2 "0010" = Detector #5 "0011" = Detector #6 "0100" = Detector #3 "0101" = Detector #4 "0110" = Detector #7 "0111" = Detector #8 "1000" = Detector #9 "1001" = Detector #10 "1010" = Detector #13 "1011" = Detector #14 "1100" = Detector #11 "1101" = Detector #12 "1110" = Detector #15 "1111" = Detector #16	R/W	0x0002	R	0x00
TECCHON	8	TEC channel ON/OFF control, High = On Bit 0: TECCH1ON_H Bit 1: TECCH2ON_H Bit 2: TECCH3ON_H Bit 3: TECCH4ON_H Bit 4: TECCH5ON_H Bit 5: TECCH6ON_H Bit 6: TECCH7ON_H Bit 7: TECCH8ON_H Bit 8-15: Reserved	R/W	0x0003	R	0x00
DASADR	16	DAS data memory buffer location: DASADR[15:9], Micro Controller Controlled (R/W) DASADR[8:0], FPGA Controlled (Read Only)	R/W	0x0004	R/W	0x0000

DAQ FPGA Registers (OD[7:0] = 0x06)						
Register Name	**Size (bits)**	**Description**	**CPU**	**Address**	**FPGA**	**Reset Value**
DASDATA	16	DAS data (Valid until written to memory)	R	0x0005	W	0x0000
SYNCCTRL	7	Sync Control Register Bit 0: SELINRISOUTFALL_H, Selects input edge for Output Falling edge Bit 1: SELINRISOUTRIS_H, Selects input edge for Output Rising edge Bit 2: CHOPRIGHT_H, Selects Right Side Chopper Electronics Bit 3: CHOPEN_H, Enables Chopper Electronics Bit 4: CHOPOFF_H, Disables Chopper Electronics Bit 5: CHOPONL_H, (Read Only) Bit 6: CHOPONR_H, (Read Only) Bit 7-15: Reserved	R/W	0X0006	R/W	0x0000
SYNCPULSEWIDTH	15	Synchronous Rectifier Pulse Width: SYNCPULSE[3:0], # of sub 1usec Counts, 1 Count = 83.33 ns SYNCPULSE[14:4], # of 1usec Counts Bit 15: Reserved	R	0X0007	W	0x0000
SYNCRDELAY1	11	Synchronous Rectifier #1 Rising Edge Phase Shift SYNCR1DAT[10:00], Delay of Rising Edge, # of 1usec Counts Bit 11-15: Reserved	R/W	0x0008	R	0
SYNCRDELAY2	11	Synchronous Rectifier #2 Rising Edge Phase Shift SYNCR2DAT[10:00], Delay of Rising Edge, # of 1usec Counts Bit 11-15: Reserved	R/W	0x0009	R	0
SYNCRDELAY3	11	Synchronous Rectifier #3 Rising Edge Phase Shift SYNCR3DAT[10:00], Delay of Rising Edge, # of 1usec Counts Bit 11-15: Reserved	R/W	0x000a	R	0
SYNCRDELAY4	11	Synchronous Rectifier #4 Rising Edge Phase Shift SYNCR4DAT[10:00], Delay of Rising Edge, # of 1usec Counts Bit 11-15: Reserved	R/W	0x000b	R	0
SYNCRDELAY5	11	Synchronous Rectifier #5 Rising Edge Phase Shift SYNCR5DAT[10:00], Delay of Rising Edge, # of 1usec Counts Bit 11-15: Reserved	R/W	0x000c	R	0

DAQ FPGA Registers (OD[7:0] = 0x06)						
Register Name	**Size (bits)**	**Description**	**CPU**	**Address**	**FPGA**	**Reset Value**
SYNCRDELAY6	11	Synchronous Rectifier #6 Rising Edge Phase Shift SYNCR6DAT[10:00], Delay of Rising Edge, # of 1usec Counts Bit 11-15: Reserved	R/W	0x000d	R	0
SYNCRDELAY7	11	Synchronous Rectifier #7 Rising Edge Phase Shift SYNCR7DAT[10:00], Delay of Rising Edge, # of 1usec Counts Bit 11-15: Reserved	R/W	0x000e	R	0
SYNCRDELAY8	11	Synchronous Rectifier #8 Rising Edge Phase Shift SYNCR8DAT[10:00], Delay of Rising Edge, # of 1usec Counts Bit 11-15: Reserved	R/W	0x000f	R	0
SYNCRDELAY9	11	Synchronous Rectifier #9 Rising Edge Phase Shift SYNCR9DAT[10:00], Delay of Rising Edge, # of 1usec Counts Bit 11-15: Reserved	R/W	0x0010	R	0
SYNCRDELAY10	11	Synchronous Rectifier #10 Rising Edge Phase Shift SYNCR10DAT[10:00], Delay of Rising Edge, # of 1usec Counts Bit 11-15: Reserved	R/W	0x0011	R	0
SYNCRDELAY11	11	Synchronous Rectifier #11 Rising Edge Phase Shift SYNCR11DAT[10:00], Delay of Rising Edge, # of 1usec Counts Bit 11-15: Reserved	R/W	0x0012	R	0
SYNCRDELAY12	11	Synchronous Rectifier #12 Rising Edge Phase Shift SYNCR12DAT[10:00], Delay of Rising Edge, # of 1usec Counts Bit 11-15: Reserved	R/W	0x0013	R	0
SYNCRDELAY13	11	Synchronous Rectifier #13 Rising Edge Phase Shift SYNCR13DAT[10:00], Delay of Rising Edge, # of 1usec Counts Bit 11-15: Reserved	R/W	0x0014	R	0
SYNCRDELAY14	11	Synchronous Rectifier #14 Rising Edge Phase Shift SYNCR14DAT[10:00], Delay of Rising Edge, # of 1usec Counts Bit 11-15: Reserved	R/W	0x0015	R	0
SYNCRDELAY15	11	Synchronous Rectifier #15 Rising Edge Phase Shift SYNCR15DAT[10:00], Delay of Rising Edge, # of 1usec Counts Bit 11-15: Reserved	R/W	0x0016	R	0
SYNCRDELAY16	11	Synchronous Rectifier #16 Rising Edge Phase Shift SYNCR16DAT[10:00], Delay of Rising Edge, # of 1usec Counts Bit 11-15: Reserved	R/W	0x0017	R	0

DAQ FPGA Registers (OD[7:0] = 0x06)						
Register Name	**Size (bits)**	**Description**	**CPU**	**Address**	**FPGA**	**Reset Value**
SYNCFDELAY1	11	Synchronous Rectifier #1 Falling Edge Phase Shift SYNCF1DAT[10:00], Delay of Falling Edge, # of 1usec Counts Bit 11-15: Reserved	R/W	0x0018	R	500
SYNCFDELAY2	11	Synchronous Rectifier #2 Falling Edge Phase Shift SYNCF2DAT[10:00], Delay of Falling Edge, # of 1usec Counts Bit 11-15: Reserved	R/W	0x0019	R	500
SYNCFDELAY3	11	Synchronous Rectifier #3 Falling Edge Phase Shift SYNCF3DAT[10:00], Delay of Falling Edge, # of 1usec Counts Bit 11-15: Reserved	R/W	0x001a	R	500
SYNCFDELAY4	11	Synchronous Rectifier #4 Falling Edge Phase Shift SYNCF4DAT[10:00], Delay of Falling Edge, # of 1usec Counts Bit 11-15: Reserved	R/W	0x001b	R	500
SYNCFDELAY5	11	Synchronous Rectifier #5 Falling Edge Phase Shift SYNCF5DAT[10:00], Delay of Falling Edge, # of 1usec Counts Bit 11-15: Reserved	R/W	0x001c	R	500
SYNCFDELAY6	11	Synchronous Rectifier #6 Falling Edge Phase Shift SYNCF6DAT[10:00], Delay of Falling Edge, # of 1usec Counts Bit 11-15: Reserved	R/W	0x001d	R	500
SYNCFDELAY7	11	Synchronous Rectifier #7 Falling Edge Phase Shift SYNCF7DAT[10:00], Delay of Falling Edge, # of 1usec Counts Bit 11-15: Reserved	R/W	0x001e	R	500
SYNCFDELAY8	11	Synchronous Rectifier #8 Falling Edge Phase Shift SYNCF8DAT[10:00], Delay of Falling Edge, # of 1usec Counts Bit 11-15: Reserved	R/W	0x001f	R	500
SYNCFDELAY9	11	Synchronous Rectifier #9 Falling Edge Phase Shift SYNCF9DAT[10:00], Delay of Falling Edge, # of 1usec Counts Bit 11-15: Reserved	R/W	0x0020	R	500
SYNCFDELAY10	11	Synchronous Rectifier #10 Falling Edge Phase Shift SYNCF10DAT[10:00], Delay of Falling Edge, # of 1usec Counts Bit 11-15: Reserved	R/W	0x0021	R	500
SYNCFDELAY11	11	Synchronous Rectifier #11 Falling Edge Phase Shift SYNCF11DAT[10:00], Delay of Falling Edge, # of 1usec Counts Bit 11-15: Reserved	R/W	0x0022	R	500

DAQ FPGA Registers (OD[7:0] = 0x06)						
Register Name	**Size (bits)**	**Description**	**CPU**	**Address**	**FPGA**	**Reset Value**
SYNCFDELAY12	11	Synchronous Rectifier #12 Falling Edge Phase Shift SYNCF12DAT[10:00], Delay of Falling Edge, # of 1usec Counts Bit 11-15: Reserved	R/W	0x0023	R	500
SYNCFDELAY13	11	Synchronous Rectifier #13 Falling Edge Phase Shift SYNCF13DAT[10:00], Delay of Falling Edge, # of 1usec Counts Bit 11-15: Reserved	R/W	0x0024	R	500
SYNCFDELAY14	11	Synchronous Rectifier #14 Falling Edge Phase Shift SYNCF14DAT[10:00], Delay of Falling Edge, # of 1usec Counts Bit 11-15: Reserved	R/W	0x0025	R	500
SYNCFDELAY15	11	Synchronous Rectifier #15 Falling Edge Phase Shift SYNCF15DAT[10:00], Delay of Falling Edge, # of 1usec Counts Bit 11-15: Reserved	R/W	0x0026	R	500
SYNCFDELAY16	11	Synchronous Rectifier #16 Falling Edge Phase Shift SYNCF16DAT[10:00], Delay of Falling Edge, # of 1usec Counts Bit 11-15: Reserved	R/W	0x0027	R	500
Total FFs:	445					

Table 7 C&DH Register Definition

11.7.3 Data Acquisition Memory Map

The A/D channel assignments for the house keeping PRTs, detector temperatures, voltage and current monitors, and Memory Map for the Acquisition Data are shown in Table 8 through Table 11.

House Keeping PRT Temperature Sensor Definition

Data Acquisition PCB #1

A/D Channel #1

TS1	(INT) Reference Resistor, 200 Ohms = 77 Kelvin
TS2	(INT) Reference Resistor, 1.38 KOhms = 373 Kelvin
TS3	(EXT) Steering Mirror Motor Coil
TS4	(EXT) Pin Puller
TS5	(EXT) Radiator Top
TS6	(EXT) Fore Optics Bench #1
TS7	(EXT) Optics Housing Bands 1&3
TS8	(EXT) Optics Housing Bands 6&8
TS9	(EXT) CSM Near Optics Module
TS10	(EXT) CSM Beam Splitter Assembly
TS11	(INT) Electronics Box Baseplate #1
TS12	(INT) C&DH PCB
TS13	(INT) Data Acquisition PCB #1
TS14	TEC Voltage Reference Channel 1
TS15	TEC Voltage Reference Channel 2
TS16	PRT Voltage Reference Channel 1

A/D Channel #2

TS17	(INT) Reference Resistor, 200 Ohms = 77 Kelvin
TS18	(INT) Reference Resistor, 1.38 KOhms = 373 Kelvin
TS19	(EXT) Steering Mirror Base
TS20	(EXT) Upper Cable Bulkhead
TS21	(EXT) Sun Sensor PCB
TS22	(EXT) Aft Optics Bench #1
TS23	(EXT) Optics Housing Bands 9&11
TS24	(EXT) Optics Housing Bands 14&16
TS25	(EXT) CSM Far Optics Module
TS26	(INT) SSG Mirror Amplifier PCB
TS27	(INT) Signal Conditioning / TEC PCB #1
TS28	(INT) Signal Conditioning / TEC PCB #2
TS29	Chopper Health Right Channel
TS30	TEC Voltage Reference Channel 3
TS31	TEC Voltage Reference Channel 4
TS32	PRT Voltage Reference Channel 2

Data Acquisition PCB #2

A/D Channel #3

TS33	(INT) Reference Resistor, 200 Ohms = 77 Kelvin
TS34	(INT) Reference Resistor, 1.38 KOhms = 373 Kelvin
TS35	(EXT) Blue Line Electronics Box
TS36	(EXT) Mid Optics Housing
TS37	(EXT) Radiator Center
TS38	(EXT) Spare
TS39	(EXT) Optics Housing Bands 10&12
TS40	(EXT) Optics Housing Bands 13&15
TS41	(EXT) Aft Optics Bench #2
TS42	(EXT) Base Deck Plate
TS43	(INT) Electronics Box Baseplate #2
TS44	(INT) Chopper PCB
TS45	(INT) Data Acquisition PCB #2

A/D Channel #4

TS49	(INT) Reference Resistor, 200 Ohms = 77 Kelvin
TS50	(INT) Reference Resistor, 1.38 KOhms = 373 Kelvin
TS51	(EXT) Aperture Cover Hinge Base Frame
TS52	(EXT) Fore Optics Bench #2
TS53	(EXT) Sun Sensor Module
TS54	(EXT) Steering Mirror Housing Top
TS55	(EXT) Optics Housing Bands 5&7
TS56	(EXT) Optics Housing Bands 2&4
TS57	(EXT) Aft Optics Bench #3
TS58	(INT) SSG Servo I/O PCB
TS59	(INT) Signal Conditioning / TEC PCB #3
TS60	(INT) Signal Conditioning / TEC PCB #4
TS61	Chopper Health Left Channel

TS46 TEC Voltage Reference Channel 5
TS47 TEC Voltage Reference Channel 6
TS48 PRT Voltage Reference Channel 3
TS62 TEC Voltage Reference Channel 7
TS63 TEC Voltage Reference Channel 8
TS64 PRT Voltage Reference Channel 4

Conversion Equations for Temperature Sensors

General Equation to get A/D counts into volts
Y = C0 + C1*DN (Where DN = A/D Counts)
Volts = (X Signed Integer) A/D Counts * (3.0 / 32768.0)
C0 = 0.000000E+00
C1 = 9.155273E-05

TS1-TS13, TS17- TS28, TS33-TS45, TS49-TS60
Y = C0 + C1*DN (Where DN = A/D Counts)
Temp Deg C = (A/D Volts * 128.0683) - 255.87
C0 = -2.560333E+02
C1 = 1.171824E-02

TS29, TS61
Y = C0 + C1*DN (Where DN = A/D Counts)
Volts = A/D Volts / 2.0
C0 = 0.000000E+00
C1 = 4.577637E-05

TS14-TS16, TS30-TS32, TS46-TS48, TS62-TS64
Y = C0 + C1*DN (Where DN = A/D Counts)
Volts = A/D Volts * 1.25
C0 = 0.000000E+00
C1 = 1.144409E-04

Table 8 House Keeping PRT A/D Channel Assignments

House Keeping Detector Temperature Definition

Data Acquisition PCB #1

A/D Channel #1

DT1	Detector 1 Temperature
DT2	Detector 2 Temperature
DT3	Detector 3 Temperature
DT4	Detector 4 Temperature

A/D Channel #2

DT5	Detector 5 Temperature
DT6	Detector 6 Temperature
DT7	Detector 7 Temperature
DT8	Detector 8 Temperature

Data Acquisition PCB #2

A/D Channel #3

DT9	Detector 9 Temperature
DT10	Detector 10 Temperature
DT11	Detector 11 Temperature
DT12	Detector 12 Temperature

A/D Channel #4

DT13	Detector 13 Temperature
DT14	Detector 14 Temperature
DT15	Detector 15 Temperature
DT16	Detector 16 Temperature

Conversion Equations for Detector Temperatures

General Equation to get A/D counts into volts

Y = C0 + C1*DN (Where DN = A/D Counts)

Volts = (X Signed Integer) A/D Counts * (3.0 / 32768.0)

C0 =	0.000000E+00
C1 =	9.155273E-05

DT1-DT12

Y = C0 + C1*DN + C2*DN^2 + … + C7*DN^7
(Where DN = A/D Counts)

C0 =	3.085764E+01
C1 =	-6.278928E-03
C2=	2.130150E-07
C3 =	-3.795255E-12
C4 =	3.653734E-17
C5 =	-1.919175E-22
C6 =	5.170105E-28
C7 =	-5.583942E-34

DT13-DT16

Y = C0 + C1*DN + C2*DN^2 + … + C7*DN^7 (Where DN = A/D Counts)	C0 =	3.085764E+01
	C1 =	-2.178788E-02
	C2=	2.564892E-06
	C3 =	-1.585731E-10
	C4 =	5.297303E-15
	C5 =	-9.655215E-20
	C6 =	9.025602E-25
	C7 =	-3.382573E-30

Table 9 House Keeping Detector Temperature A/D Channel Assignments

House Keeping Power Supply Definition

Data Acquisition PCB #1

A/D Channel #1

PS1	PS Voltage Monitor +12V_I
PS2	PS Voltage Monitor -12V_I
PS3	PS Current Monitor +12V_I
PS4	PS Current Monitor -12V_I

A/D Channel #2

PS5	PS Voltage Monitor +5V
PS6	PS Voltage Monitor +3.3V TEC
PS7	PS Current Monitor +5V
PS8	PS Current Monitor +3.3V TEC

Data Acquisition PCB #2

A/D Channel #3

PS9	PS Voltage Monitor +12V_SM
PS10	PS Voltage Monitor -12V_SM
PS11	PS Current Monitor +12V_SM
PS12	PS Current Monitor - 12V_SM

A/D Channel #4

PS13	PS Voltage Monitor +2.5V TEC
PS14	PS Voltage Monitor +2.5V FPGA
PS15	PS Current Monitor +2.5V TEC
PS16	PS Current Monitor +2.5V FPGA

Conversion Equations for Power Supplies Voltages and Currents

General Equation to get A/D counts into volts

Y = C0 + C1*DN (Where DN = A/D Counts)

Volts = (X Signed Integer) A/D Counts * (3.0 / 32768.0)

C0 = 0.000000E+00

C1 = 9.155273E-05

PS1-PS2,PS9-PS10

Y = C0 + C1*DN (Where DN = A/D Counts)

Volts = A/D Volts / (10k / 50.2k ohms)

C0 = 0.000000E+00

C1 = 4.595947E-04

PS5-PS6, PS13-PS14

Y = C0 + C1*DN (Where DN = A/D Counts)

Volts = A/D Volts / (10k / 20k ohms)

C0 = 0.000000E+00

C1 = 1.831055E-04

PS3

Y = C0 + C1*DN (Where DN = A/D Counts)

Amps = (A/D Volts + 57.17mV)/(0.04974 ohms * 21 gain)

C0 = 0.054732227

C1 = 8.76489E-05

PS4		Amps = (A/D Volts - 21.12mV)/(0.04979 ohms * 21 gain)
	Y = C0 + C1*DN (Where DN = A/D Counts)	C0 = -0.020199122
		C1 = 8.75608E-05
PS7		Amps = (A/D Volts + 23.54mV)/(0.01013 ohms * 41 gain)
	Y = C0 + C1*DN (Where DN = A/D Counts)	C0 = 0.056677822
		C1 = 2.20434E-04
PS8		Amps = (A/D Volts - 8.41mV)/(0.01016 ohms * 41 gain)
	Y = C0 + C1*DN (Where DN = A/D Counts)	C0 = -0.020189168
		C1 = 2.19783E-04
PS11		Amps = (A/D Volts - 36.78mV)/(0.05 ohms * 21 gain)
	Y = C0 + C1*DN (Where DN = A/D Counts)	C0 = -0.035028571
		C1 = 8.71931E-05
PS12		Amps = (A/D Volts - 20.73mV)/(0.05 ohms * 21 gain)
	Y = C0 + C1*DN (Where DN = A/D Counts)	C0 = -0.019742857
		C1 = 8.71931E-05
PS15		Amps = (A/D Volts + 51.54mV)/(0.01013 ohms * 41 gain)
	Y = C0 + C1*DN (Where DN = A/D Counts)	C0 = 0.124094094
		C1 = 2.20434E-04
PS16		Amps = (A/D Volts - 23.54mV)/(0.2 ohms * 41 gain)
	Y = C0 + C1*DN (Where DN = A/D Counts)	C0 = -0.002870732
		C1 = 1.11650E-05

Table 10 House Keeping Power Supply A/D Channel Assignments

Address Memory Map for the A/D measurements 16-bit values, 512 Locations

June 1, 2005

S# = Sample #, HK = HouseKeeping, DT = Detector Temp, TS = Temp Sensor, PS = Power Supply Voltage / Current

	A/D Conv #1	A/D Conv #2	A/D Conv #3	A/D Conv #4	A/D Conv #1	A/D Conv #2	A/D Conv #3	A/D Conv #4
Address	0x0	0x1	0x2	0x3	0x4	0x5	0x6	0x7
0x0	Chan. 1 Detector 1 S#1	Chan. 3 Detector 5 S#1	Chan. 5 Detector 9 S#1	Chan. 7 Detector 13 S#1	Chan. 1 Diff Signal S#1	Chan. 3 Diff Signal S#1	Chan. 5 Diff Signal S#1	Chan. 7 Diff Signal S#1
0x8	Chan. 1 Detector 2 S#1	Chan. 3 Detector 6 S#1	Chan. 5 Detector 10 S#1	Chan. 7 Detector 14 S#1	HK DT1 S#1	HK DT5 S#1	HK DT9 S#1	HK DT13 S#1
0x10	Chan. 2 Detector 3 S#1	Chan. 4 Detector 7 S#1	Chan. 6 Detector 11 S#1	Chan. 8 Detector 15 S#1	Chan. 2 Diff Signal S#1	Chan. 4 Diff Signal S#1	Chan. 6 Diff Signal S#1	Difference Sig. Chan. 8 S#1
0x18	Chan. 2 Detector 4 S#1	Chan. 4 Detector 8 S#1	Chan. 6 Detector 12 S#1	Chan. 8 Detector 16 S#1	HK TS1 S#1	HK TS17 S#1	HK TS33 S#1	HK TS49 S#1
0x20	Chan. 1 Detector 1 S#2	Chan. 3 Detector 5 S#2	Chan. 5 Detector 9 S#2	Chan. 7 Detector 13 S#2	Chan. 1 Diff Signal S#2	Chan. 3 Diff Signal S#2	Chan. 5 Diff Signal S#2	Chan. 7 Diff Signal S#2
0x28	Chan. 1 Detector 2 S#2	Chan. 3 Detector 6 S#2	Chan. 5 Detector 10 S#2	Chan. 7 Detector 14 S#2	HK DT2 S#1	HK DT6 S#1	HK DT10 S#1	HK DT14 S#1
0x30	Chan. 2 Detector 3 S#2	Chan. 4 Detector 7 S#2	Chan. 6 Detector 11 S#2	Chan. 8 Detector 15 S#2	Chan. 2 Diff Signal S#2	Chan. 4 Diff Signal S#2	Chan. 6 Diff Signal S#2	Chan. 8 Diff Signal S#2
0x38	Chan. 2 Detector 4 S#2	Chan. 4 Detector 8 S#2	Chan. 6 Detector 12 S#2	Chan. 8 Detector 16 S#2	HK TS2 S#1	HK TS18 S#1	HK TS34 S#1	HK TS50 S#1
0x40	Chan. 1 Detector 1 S#3	Chan. 3 Detector 5 S#3	Chan. 5 Detector 9 S#3	Chan. 7 Detector 13 S#3	Chan. 1 Diff Signal S#3	Chan. 3 Diff Signal S#3	Chan. 5 Diff Signal S#3	Chan. 7 Diff Signal S#3
0x48	Chan. 1 Detector 2 S#3	Chan. 3 Detector 6 S#3	Chan. 5 Detector 10 S#3	Chan. 7 Detector 14 S#3	HK DT3 S#1	HK DT7 S#1	HK DT11 S#1	HK DT15 S#1

0x50	Chan. 2 Detector 3 S#3	Chan. 4 Detector 7 S#3	Chan. 6 Detector 11 S#3	Chan. 8 Detector 15 S#3	Chan. 2 Diff Signal S#3	Chan. 4 Diff Signal S#3	Chan. 6 Diff Signal S#3	Chan. 8 Diff Signal S#3
0x58	Chan. 2 Detector 4 S#3	Chan. 4 Detector 8 S#3	Chan. 6 Detector 12 S#3	Chan. 8 Detector 16 S#3	HK TS3 S#1	HK TS19 S#1	HK TS35 S#1	HK TS51 S#1
0x60	Chan. 1 Detector 1 S#4	Chan. 3 Detector 5 S#4	Chan. 5 Detector 9 S#4	Chan. 7 Detector 13 S#4	Chan. 1 Diff Signal S#4	Chan. 3 Diff Signal S#4	Chan. 5 Diff Signal S#4	Chan. 7 Diff Signal S#4
0x68	Chan. 1 Detector 2 S#4	Chan. 3 Detector 6 S#4	Chan. 5 Detector 10 S#4	Chan. 7 Detector 14 S#4	HK DT4 S#1	HK DT8 S#1	HK DT12 S#1	HK DT16 S#1
0x70	Chan. 2 Detector 3 S#4	Chan. 4 Detector 7 S#4	Chan. 6 Detector 11 S#4	Chan. 8 Detector 15 S#4	Chan. 2 Diff Signal S#4	Chan. 4 Diff Signal S#4	Chan. 6 Diff Signal S#4	Chan. 8 Diff Signal S#4
0x78	Chan. 2 Detector 4 S#4	Chan. 4 Detector 8 S#4	Chan. 6 Detector 12 S#4	Chan. 8 Detector 16 S#4	HK TS4 S#1	HK TS20 S#1	HK TS36 S#1	HK TS52 S#1
0x80	Chan. 1 Detector 1 S#5	Chan. 3 Detector 5 S#5	Chan. 5 Detector 9 S#5	Chan. 7 Detector 13 S#5	Chan. 1 Diff Signal S#5	Chan. 3 Diff Signal S#5	Chan. 5 Diff Signal S#5	Chan. 7 Diff Signal S#5
0x88	Chan. 1 Detector 2 S#5	Chan. 3 Detector 6 S#5	Chan. 5 Detector 10 S#5	Chan. 7 Detector 14 S#5	HK PS1 S#1	HK PS5 S#1	HK PS9 S#1	HK PS13 S#1
0x90	Chan. 2 Detector 3 S#5	Chan. 4 Detector 7 S#5	Chan. 6 Detector 11 S#5	Chan. 8 Detector 15 S#5	Chan. 2 Diff Signal S#5	Chan. 4 Diff Signal S#5	Chan. 6 Diff Signal S#5	Chan. 8 Diff Signal S#5
0x98	Chan. 2 Detector 4 S#5	Chan. 4 Detector 8 S#5	Chan. 6 Detector 12 S#5	Chan. 8 Detector 16 S#5	HK TS5 S#1	HK TS21 S#1	HK TS37 S#1	HK TS53 S#1
0xa0	Chan. 1 Detector 1 S#6	Chan. 3 Detector 5 S#6	Chan. 5 Detector 9 S#6	Chan. 7 Detector 13 S#6	Chan. 1 Diff Signal S#6	Chan. 3 Diff Signal S#6	Chan. 5 Diff Signal S#6	Chan. 7 Diff Signal S#6
0xa8	Chan. 1 Detector 2 S#6	Chan. 3 Detector 6 S#6	Chan. 5 Detector 10 S#6	Chan. 7 Detector 14 S#6	HK PS2 S#1	HK PS6 S#1	HK PS10 S#1	HK PS14 S#1
0xb0	Chan. 2 Detector 3 S#6	Chan. 4 Detector 7 S#6	Chan. 6 Detector 11 S#6	Chan. 8 Detector 15 S#6	Chan. 2 Diff Signal S#6	Chan. 4 Diff Signal S#6	Chan. 6 Diff Signal S#6	Chan. 8 Diff Signal S#6

0xb8	Chan. 2 Detector 4 S#6	Chan. 4 Detector 8 S#6	Chan. 6 Detector 12 S#6	Chan. 8 Detector 16 S#6	HK TS6 S#1	HK TS22 S#1	HK TS38 S#1	HK TS54 S#1
0xc0	Chan. 1 Detector 1 S#7	Chan. 3 Detector 5 S#7	Chan. 5 Detector 9 S#7	Chan. 7 Detector 13 S#7	Chan. 1 Diff Signal S#7	Chan. 3 Diff Signal S#7	Chan. 5 Diff Signal S#7	Chan. 7 Diff Signal S#7
0xc8	Chan. 1 Detector 2 S#7	Chan. 3 Detector 6 S#7	Chan. 5 Detector 10 S#7	Chan. 7 Detector 14 S#7	HK PS3 S#1	HK PS7 S#1	HK PS11 S#1	HK PS15 S#1
0xd0	Chan. 2 Detector 3 S#7	Chan. 4 Detector 7 S#7	Chan. 6 Detector 11 S#7	Chan. 8 Detector 15 S#7	Chan. 2 Diff Signal S#7	Chan. 4 Diff Signal S#7	Chan. 6 Diff Signal S#7	Chan. 8 Diff Signal S#7
0xd8	Chan. 2 Detector 4 S#7	Chan. 4 Detector 8 S#7	Chan. 6 Detector 12 S#7	Chan. 8 Detector 16 S#7	HK TS7 S#1	HK TS23 S#1	HK TS39 S#1	HK TS55 S#1
0xe0	Chan. 1 Detector 1 S#8	Chan. 3 Detector 5 S#8	Chan. 5 Detector 9 S#8	Chan. 7 Detector 13 S#8	Chan. 1 Diff Signal S#8	Chan. 3 Diff Signal S#8	Chan. 5 Diff Signal S#8	Chan. 7 Diff Signal S#8
0xe8	Chan. 1 Detector 2 S#8	Chan. 3 Detector 6 S#8	Chan. 5 Detector 10 S#8	Chan. 7 Detector 14 S#8	HK PS4 S#1	HK PS8 S#1	HK PS12 S#1	HK PS16 S#1
0xf0	Chan. 2 Detector 3 S#8	Chan. 4 Detector 7 S#8	Chan. 6 Detector 11 S#8	Chan. 8 Detector 15 S#8	Chan. 2 Diff Signal S#8	Chan. 4 Diff Signal S#8	Chan. 6 Diff Signal S#8	Chan. 8 Diff Signal S#8
0xf8	Chan. 2 Detector 4 S#8	Chan. 4 Detector 8 S#8	Chan. 6 Detector 12 S#8	Chan. 8 Detector 16 S#8	HK TS8 S#1	HK TS24 S#1	HK TS40 S#1	HK TS56 S#1
0x100	Chan. 1 Detector 1 S#9	Chan. 3 Detector 5 S#9	Chan. 5 Detector 9 S#9	Chan. 7 Detector 13 S#9	Chan. 1 Diff Signal S#9	Chan. 3 Diff Signal S#9	Chan. 5 Diff Signal S#9	Chan. 7 Diff Signal S#9
0x108	Chan. 1 Detector 2 S#9	Chan. 3 Detector 6 S#9	Chan. 5 Detector 10 S#9	Chan. 7 Detector 14 S#9	HK DT1 S#2	HK DT5 S#2	HK DT9 S#2	HK DT13 S#2
0x110	Chan. 2 Detector 3 S#9	Chan. 4 Detector 7 S#9	Chan. 6 Detector 11 S#9	Chan. 8 Detector 15 S#9	Chan. 2 Diff Signal S#9	Chan. 4 Diff Signal S#9	Chan. 6 Diff Signal S#9	Chan. 8 Diff Signal S#9
0x118	Chan. 2 Detector 4 S#9	Chan. 4 Detector 8 S#9	Chan. 6 Detector 12 S#9	Chan. 8 Detector 16 S#9	HK TS9 S#1	HK TS25 S#1	HK TS41 S#1	HK TS57 S#1

0x120	Chan. 1 Detector 1 S#10	Chan. 3 Detector 5 S#10	Chan. 5 Detector 9 S#10	Chan. 7 Detector 13 S#10	Chan. 1 Diff Signal S#10	Chan. 3 Diff Signal S#10	Chan. 5 Diff Signal S#10	Chan. 7 Diff Signal S#10
0x128	Chan. 1 Detector 2 S#10	Chan. 3 Detector 6 S#10	Chan. 5 Detector 10 S#10	Chan. 7 Detector 14 S#10	HK TD2 S#2	HK DT6 S#2	HK DT10 S#2	HK DT14 S#2
0x130	Chan. 2 Detector 3 S#10	Chan. 4 Detector 7 S#10	Chan. 6 Detector 11 S#10	Chan. 8 Detector 15 S#10	Chan. 2 Diff Signal S#10	Chan. 4 Diff Signal S#10	Chan. 6 Diff Signal S#10	Chan. 8 Diff Signal S#10
0x138	Chan. 2 Detector 4 S#10	Chan. 4 Detector 8 S#10	Chan. 6 Detector 12 S#10	Chan. 8 Detector 16 S#10	HK TS10 S#1	HK TS26 S#1	HK TS42 S#1	HK TS58 S#1
0x140	Chan. 1 Detector 1 S#11	Chan. 3 Detector 5 S#11	Chan. 5 Detector 9 S#11	Chan. 7 Detector 13 S#11	Chan. 1 Diff Signal S#11	Chan. 3 Diff Signal S#11	Chan. 5 Diff Signal S#11	Chan. 7 Diff Signal S#11
0x148	Chan. 1 Detector 2 S#11	Chan. 3 Detector 6 S#11	Chan. 5 Detector 10 S#11	Chan. 7 Detector 14 S#11	HK DT3 S#2	HK DT7 S#2	HK DT11 S#2	HK DT15 S#2
0x150	Chan. 2 Detector 3 S#11	Chan. 4 Detector 7 S#11	Chan. 6 Detector 11 S#11	Chan. 8 Detector 15 S#11	Chan. 2 Diff Signal S#11	Chan. 4 Diff Signal S#11	Chan. 6 Diff Signal S#11	Chan. 8 Diff Signal S#11
0x158	Chan. 2 Detector 4 S#11	Chan. 4 Detector 8 S#11	Chan. 6 Detector 12 S#11	Chan. 8 Detector 16 S#11	HK TS11 S#1	HK TS27 S#1	HK TS43 S#1	HK TS59 S#1
0x160	Chan. 1 Detector 1 S#12	Chan. 3 Detector 5 S#12	Chan. 5 Detector 9 S#12	Chan. 7 Detector 13 S#12	Chan. 1 Diff Signal S#12	Chan. 3 Diff Signal S#12	Chan. 5 Diff Signal S#12	Chan. 7 Diff Signal S#12
0x168	Chan. 1 Detector 2 S#12	Chan. 3 Detector 6 S#12	Chan. 5 Detector 10 S#12	Chan. 7 Detector 14 S#12	HK DT4 S#2	HK DT8 S#2	HK DT12 S#2	HK DT16 S#2
0x170	Chan. 2 Detector 3 S#12	Chan. 4 Detector 7 S#12	Chan. 6 Detector 11 S#12	Chan. 8 Detector 15 S#12	Chan. 2 Diff Signal S#12	Chan. 4 Diff Signal S#12	Chan. 6 Diff Signal S#12	Chan. 8 Diff Signal S#12
0x178	Chan. 2 Detector 4 S#12	Chan. 4 Detector 8 S#12	Chan. 6 Detector 12 S#12	Chan. 8 Detector 16 S#12	HK TS12 S#1	HK TS28 S#1	HK TS44 S#1	HK TS60 S#1

0x180	Chan. 1 Detector 1 S#13	Chan. 3 Detector 5 S#13	Chan. 5 Detector 9 S#13	Chan. 7 Detector 13 S#13	Chan. 1 Diff Signal S#13	Chan. 3 Diff Signal S#13	Chan. 5 Diff Signal S#13	Chan. 7 Diff Signal S#13
0x188	Chan. 1 Detector 2 S#13	Chan. 3 Detector 6 S#13	Chan. 5 Detector 10 S#13	Chan. 7 Detector 14 S#13	HK PS1 S#2	HK PS5 S#2	HK PS9 S#2	HK PS13 S#2
0x190	Chan. 2 Detector 3 S#13	Chan. 4 Detector 7 S#13	Chan. 6 Detector 11 S#13	Chan. 8 Detector 15 S#13	Chan. 2 Diff Signal S#13	Chan. 4 Diff Signal S#13	Chan. 6 Diff Signal S#13	Chan. 8 Diff Signal S#13
0x198	Chan. 2 Detector 4 S#13	Chan. 4 Detector 8 S#13	Chan. 6 Detector 12 S#13	Chan. 8 Detector 16 S#13	HK TS13 S#1	HK TS29 S#1	HK TS45 S#1	HK TS61 S#1
0x1a0	Chan. 1 Detector 1 S#14	Chan. 3 Detector 5 S#14	Chan. 5 Detector 9 S#14	Chan. 7 Detector 13 S#14	Chan. 1 Diff Signal S#14	Chan. 3 Diff Signal S#14	Chan. 5 Diff Signal S#14	Chan. 7 Diff Signal S#14
0x1a8	Chan. 1 Detector 2 S#14	Chan. 3 Detector 6 S#14	Chan. 5 Detector 10 S#14	Chan. 7 Detector 14 S#14	HK PS2 S#2	HK PS6 S#2	HK PS10 S#2	HK PS14 S#2
0x1b0	Chan. 2 Detector 3 S#14	Chan. 4 Detector 7 S#14	Chan. 6 Detector 11 S#14	Chan. 8 Detector 15 S#14	Chan. 2 Diff Signal S#14	Chan. 4 Diff Signal S#14	Chan. 6 Diff Signal S#14	Chan. 8 Diff Signal S#14
0x1b8	Chan. 2 Detector 4 S#14	Chan. 4 Detector 8 S#14	Chan. 6 Detector 12 S#14	Chan. 8 Detector 16 S#14	HK TS14 S#1	HK TS30 S#1	HK TS46 S#1	HK TS62 S#1
0x1c0	Chan. 1 Detector 1 S#15	Chan. 3 Detector 5 S#15	Chan. 5 Detector 9 S#15	Chan. 7 Detector 13 S#15	Chan. 1 Diff Signal S#15	Chan. 3 Diff Signal S#15	Chan. 5 Diff Signal S#15	Chan. 7 Diff Signal S#15
0x1c8	Chan. 1 Detector 2 S#15	Chan. 3 Detector 6 S#15	Chan. 5 Detector 10 S#15	Chan. 7 Detector 14 S#15	HK PS3 S#2	HK PS7 S#2	HK PS11 S#2	HK PS15 S#2
0x1d0	Chan. 2 Detector 3 S#15	Chan. 4 Detector 7 S#15	Chan. 6 Detector 11 S#15	Chan. 8 Detector 15 S#15	Chan. 2 Diff Signal S#15	Chan. 4 Diff Signal S#15	Chan. 6 Diff Signal S#15	Chan. 8 Diff Signal S#15
0x1d8	Chan. 2 Detector 4 S#15	Chan. 4 Detector 8 S#15	Chan. 6 Detector 12 S#15	Chan. 8 Detector 16 S#15	HK TS15 S#1	HK TS31 S#1	HK TS47 S#1	HK TS63 S#1

0x1e0	Chan. 1 Detector 1 S#16	Chan. 3 Detector 5 S#16	Chan. 5 Detector 9 S#16	Chan. 7 Detector 13 S#16	Chan. 1 Diff Signal S#16	Chan. 3 Diff Signal S#16	Chan. 5 Diff Signal S#16	Chan. 7 Diff Signal S#16
0x1e8	Chan. 1 Detector 2 S#16	Chan. 3 Detector 6 S#16	Chan. 5 Detector 10 S#16	Chan. 7 Detector 14 S#16	HK PS4 S#2	HK PS8 S#2	HK PS12 S#2	HK PS16 S#2
0x1f0	Chan. 2 Detector 3 S#16	Chan. 4 Detector 7 S#16	Chan. 6 Detector 11 S#16	Chan. 8 Detector 15 S#16	Chan. 2 Diff Signal S#16	Chan. 4 Diff Signal S#16	Chan. 6 Diff Signal S#16	Chan. 8 Diff Signal S#16
0x1f8	Chan. 2 Detector 4 S#16	Chan. 4 Detector 8 S#16	Chan. 6 Detector 12 S#16	Chan. 8 Detector 16 S#16	HK TS16 S#1	HK TS32 S#1	HK TS48 S#1	HK TS64 S#1

Table 11 Data Acquisition Memory Map

12. SOFIE CABLING/CONNECTOR INTERFACE CONTROL

This section defines the interfaces between the sub-components and modules within the SOFIE system. Pictures are used to show the locations for the connections along with a table outlining the connection and the associated assembly number for the build. Additional information related to pin assignments for the cables can by found in Appendix B.

12.1 General Overview

The SOFIE cables fall into two primary groups. The first group contains cables which run from the SOFIE Electronics Box to the SOFIE Instrument. The second group contains cables internal to the SOFIE Instrument. Reference designators for each cable end are used to group the cables in terms of general locations. The letters J and P are also used to designate the two sides of a mating pair, with J representing a jack or fixed location (examples include connectors mounted on circuit boards or fastened to the wall of a container) and P representing the plug or flexible end of a cable.

The basic reference designators are listed in Table 12.

Designator	
Jxxx	Typically a Jack or rigid mounted connector (Exception when both ends of a cable of flexible)
Pxxx	Plug or flexible end
J1xx or P1xx	Connectors on or near the electronics box which interface with the spacecraft power system
J3xx or P3xx	Connectors on the electronics box which interface with the instrument or the spacecraft communications system
J4xx or P4xx	Connectors on the instrument which interface with the electronics box and the instrument electronics
J5xx or P5xx	Connectors internal to the instrument which are tied to the detector assemblies
J6xx or P6xx	Connectors internal to the instrument which are tied to electronics internal to the instrument
J7xx or P7xx	Temperature sensors

Table 12 Basic cabling reference designators.

12.2 Electronics Box External Connections

The following figures show the exterior connections for the SOFIE electronics box.

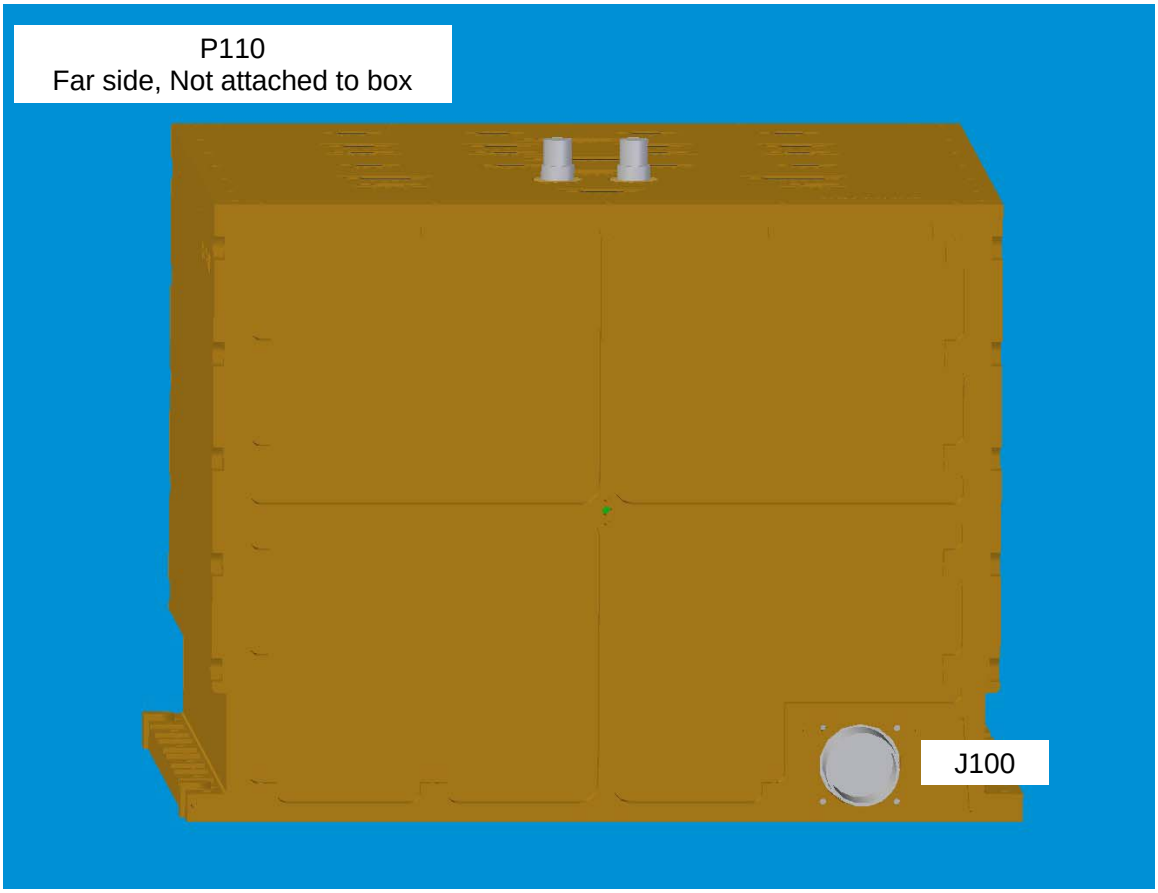


Figure 88 Electronics Box auxilary connections.

J100	48-0428	Electronics Box, Power Assembly
P100		Spacecraft, Power
P110		Spacecraft, Survival Heaters
P100	48-0160	GSE, Power Bench Operation
P100	48-0486	GSE, TVAC Internal
P110	48-0486	GSE, TVAC Internal

Table 13 Electronics Box auxiliary connections.

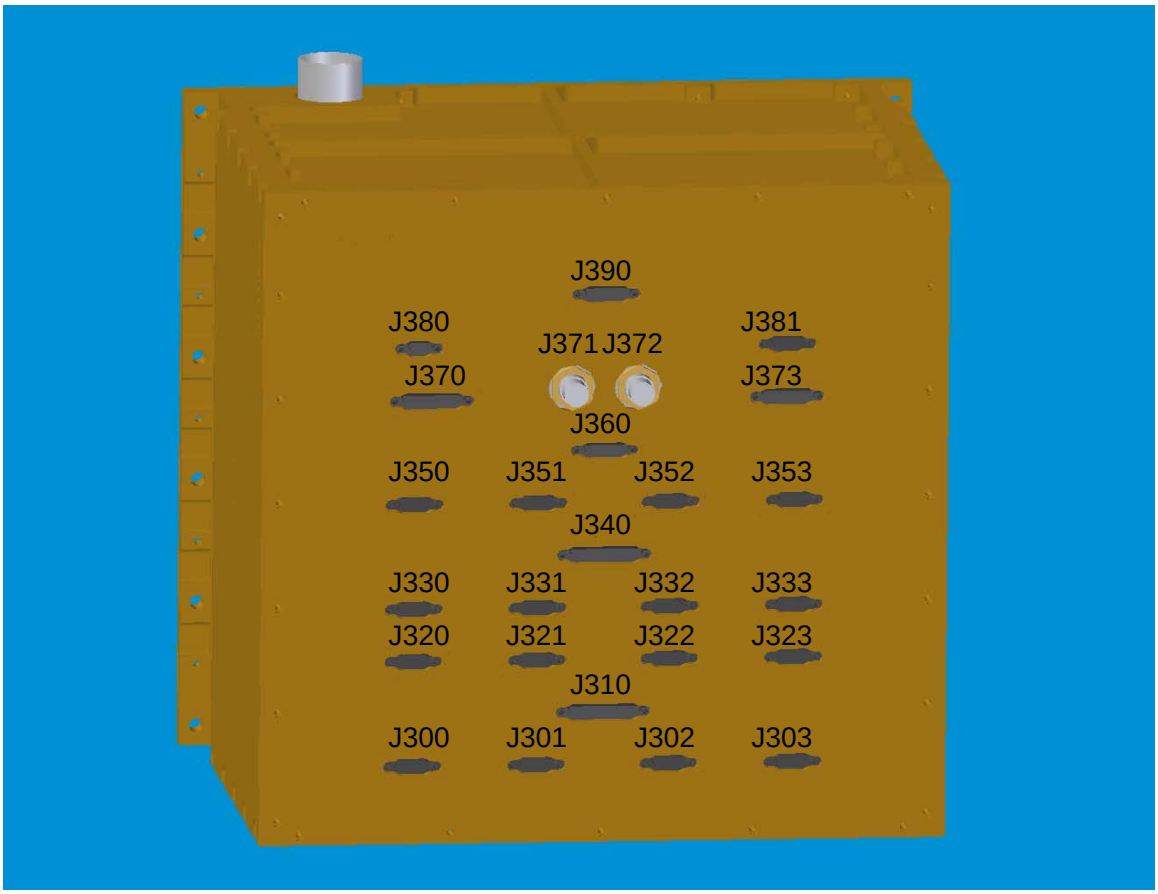


Figure 89 Electronics Box instrument connections.

J390	48-0xxx	SSG Servo Motor, PCB
J380	48-0xxx	SSG Motor Control, PCB
J381	48-0xxx	SSG Motor Control, PCB
J370	48-0xxx	C&DH
J371	48-0xxx	C&DH
J372	48-0xxx	C&DH
J373	48-0xxx	C&DH
J360	48-0xxx	Chopper
J350	48-0xxx	Signal/Tec 4
J351	48-0xxx	Signal/Tec 4
J352	48-0xxx	Signal/Tec 4
J353	48-0xxx	Signal/Tec 4
J340	48-0xxx	Data Acquisition 2
J330	48-0xxx	Signal/Tec 3
J331	48-0xxx	Signal/Tec 3
J332	48-0xxx	Signal/Tec 3
J333	48-0xxx	Signal/Tec 3
J320	48-0xxx	Signal/Tec 2

J321	48-0xxx	Signal/Tec 2
J322	48-0xxx	Signal/Tec 2
J323	48-0xxx	Signal/Tec 2
J310	48-0xxx	Data Acquisition 1
J300	48-0xxx	Signal/Tec 1
J301	48-0xxx	Signal/Tec 1
J302	48-0xxx	Signal/Tec 1
J303	48-0xxx	Signal/Tec 1
P390	48-0359	Motor, External
P380	48-0356	Sun sensor, External
P381	48-0358	Position, External
P370	48-0356	Sun sensor, External
P371		Spacecraft, 1553A
P372		Spacecraft, 1553B
P373	48-0357	Release
P360	48-0355	Chopper
P350	48-0353	Signal/TEC 2, External
P351	48-0353	Signal/TEC 2, External
P352	48-0353	Signal/TEC 2, External
P353	48-0353	Signal/TEC 2, External
P340	48-0354	Data Acquisition, External
P330	48-0353	Signal/TEC 2, External
P331	48-0353	Signal/TEC 2, External
P332	48-0353	Signal/TEC 2, External
P333	48-0353	Signal/TEC 2, External
P320	48-0352	Signal/TEC 1, External
P321	48-0352	Signal/TEC 1, External
P322	48-0352	Signal/TEC 1, External
P323	48-0352	Signal/TEC 1, External
P310	48-0354	Data Acquisition, External
P300	48-0352	Signal/TEC 1, External
P301	48-0352	Signal/TEC 1, External
P302	48-0352	Signal/TEC 1, External
P303	48-0352	Signal/TEC 1, External

Table 14 Electronics Box instrument connections.

12.3 Instrument External Connections

The following figures and tables outline the external connections on the SOFIE instrument.

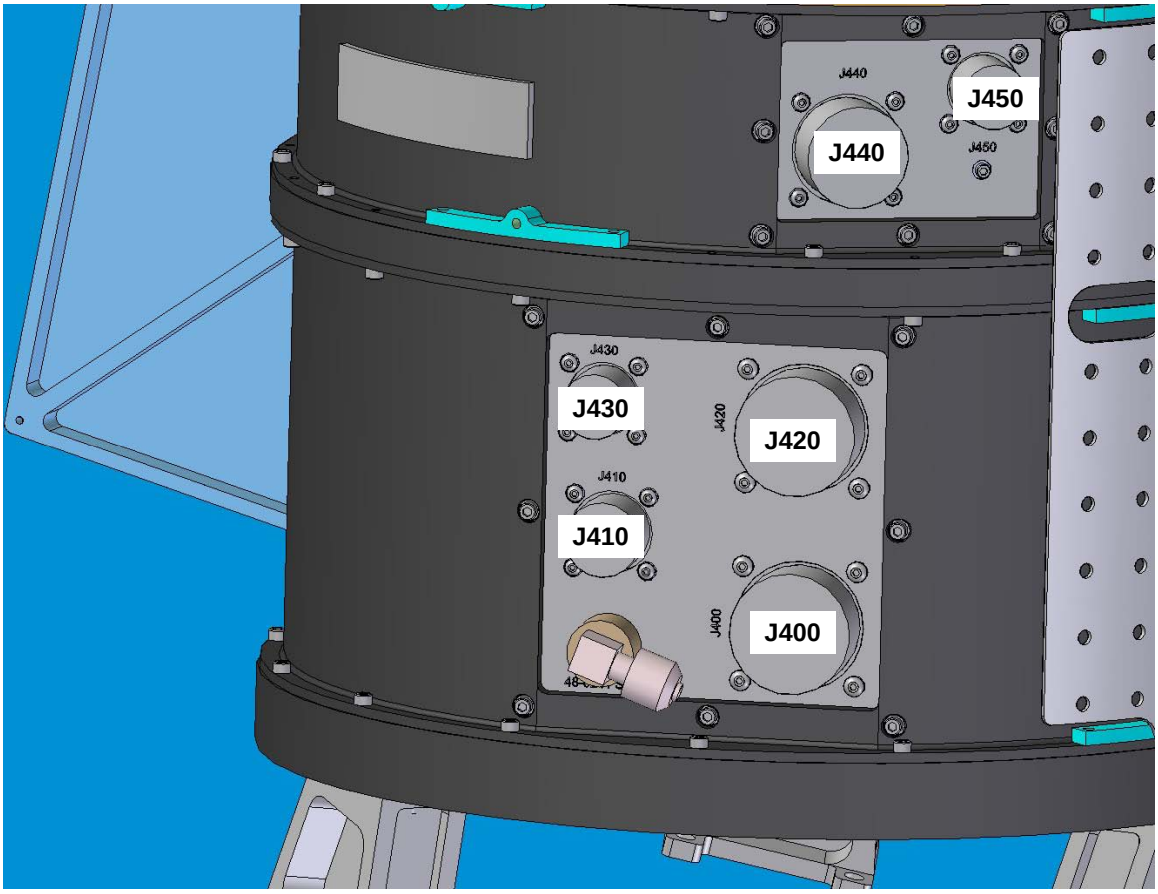


Figure 90 Instrument external connections 1

J450	48-0365	Chopper, Internal
J440	48-0366	Data Acquisition, Internal
J430	48-0368	Survival Heaters, Internal
J420	48-0363	Signal/TEC 2, Internal
J410	48-0366	Sun sensor, Internal
J400	48-0362	Signal/TEC 1, Internal
P450	48-0355	Chopper, External
P440	48-0354	Data Acquisition, External
P430	48-0360	Survival Heaters, External
P420	48-0353	Signal/TEC 2, External
P410	48-0356	Sun sensor, External
P400	48-0352	Signal/TEC 1, External

Table 15 Instrument external connections 1

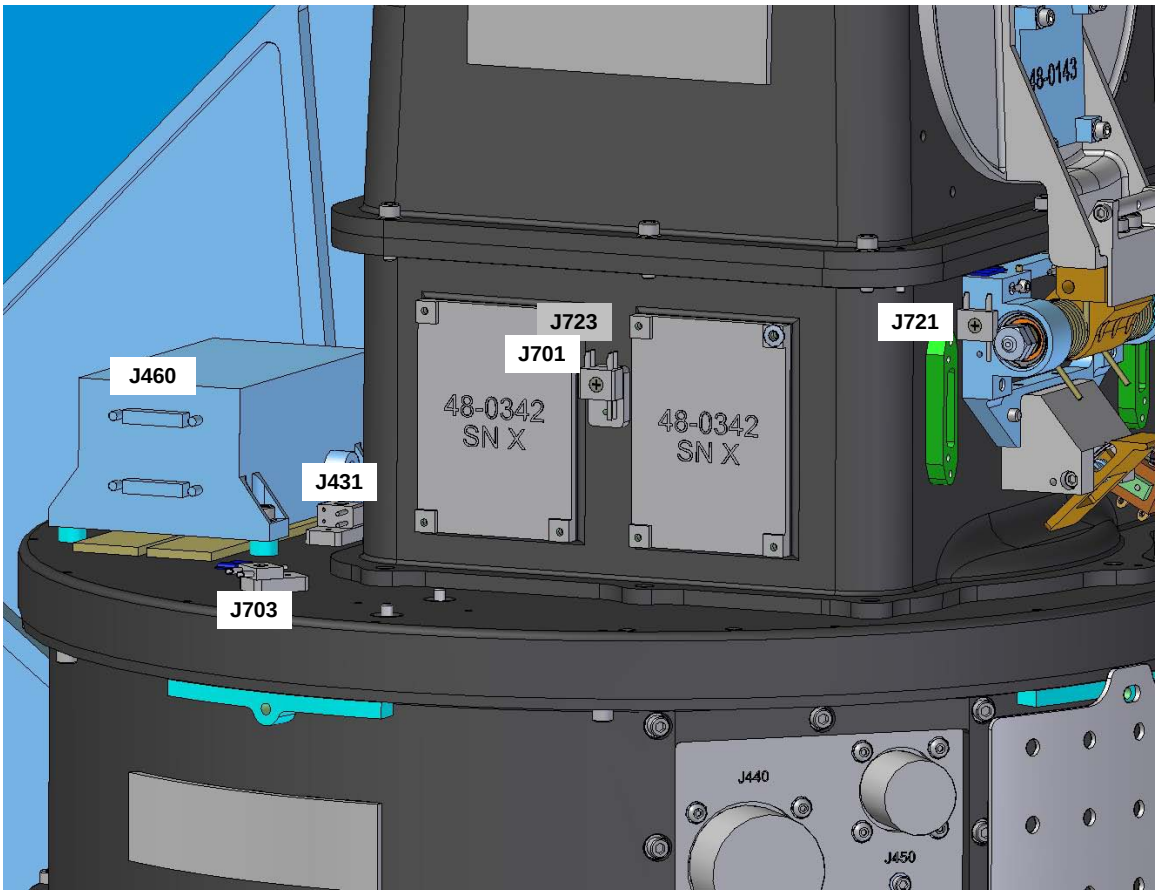


Figure 91 Instrument external connections 2

J460	48-0365	Blue Line Electronics
J723	48-0391	TS[54] (EXT) Steering Mirror Housing Top
J701	48-0392	TS[4] (EXT) Pin Puller
J721	48-0390	TS[51] (EXT) Aperture Cover Hinge Base Frame
J431	48-0413	Heaters, Blue Line Electronics
J703	48-0413	TS[6] (EXT) Fore Optics Bench #1
P460	48-0358	Position, External
P723	48-0354	Data Acquisition, External
P701	48-0354	Data Acquisition, External
P721	48-0354	Data Acquisition, External
P431	48-0360	Survival Heaters, External
P703	48-0354	Data Acquisition, External

Table 16 Instrument external connections 2

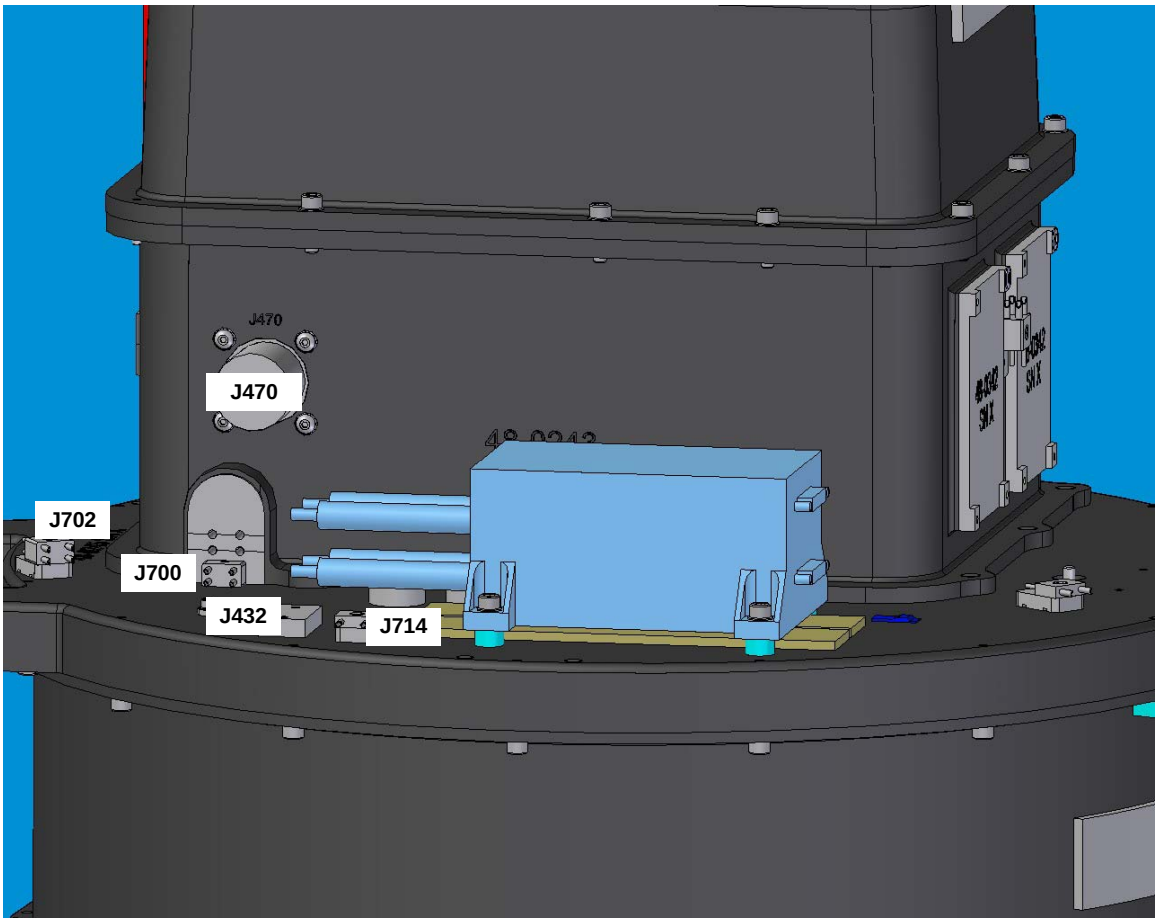


Figure 92 Instrument external connections 3

J470	48-0367	Motor, Internal
J702	48-0389	TS[5] (EXT) Radiator Top TS[37] (EXT) Radiator Center
J700	48-0367	Motor, Internal
J432		Temperature sensor, Spacecraft
J714	48-0404	TS[35] (EXT) Blue Line Electronics Box
P470	48-0359	Motor, External
P702	48-0354	Data Acquisition, External
P700	48-0354	Data Acquisition, External
P432	48-0360	Survival Heater, External
P714	48-0354	Data Acquisition, External

Table 17 Instrument external connections 3

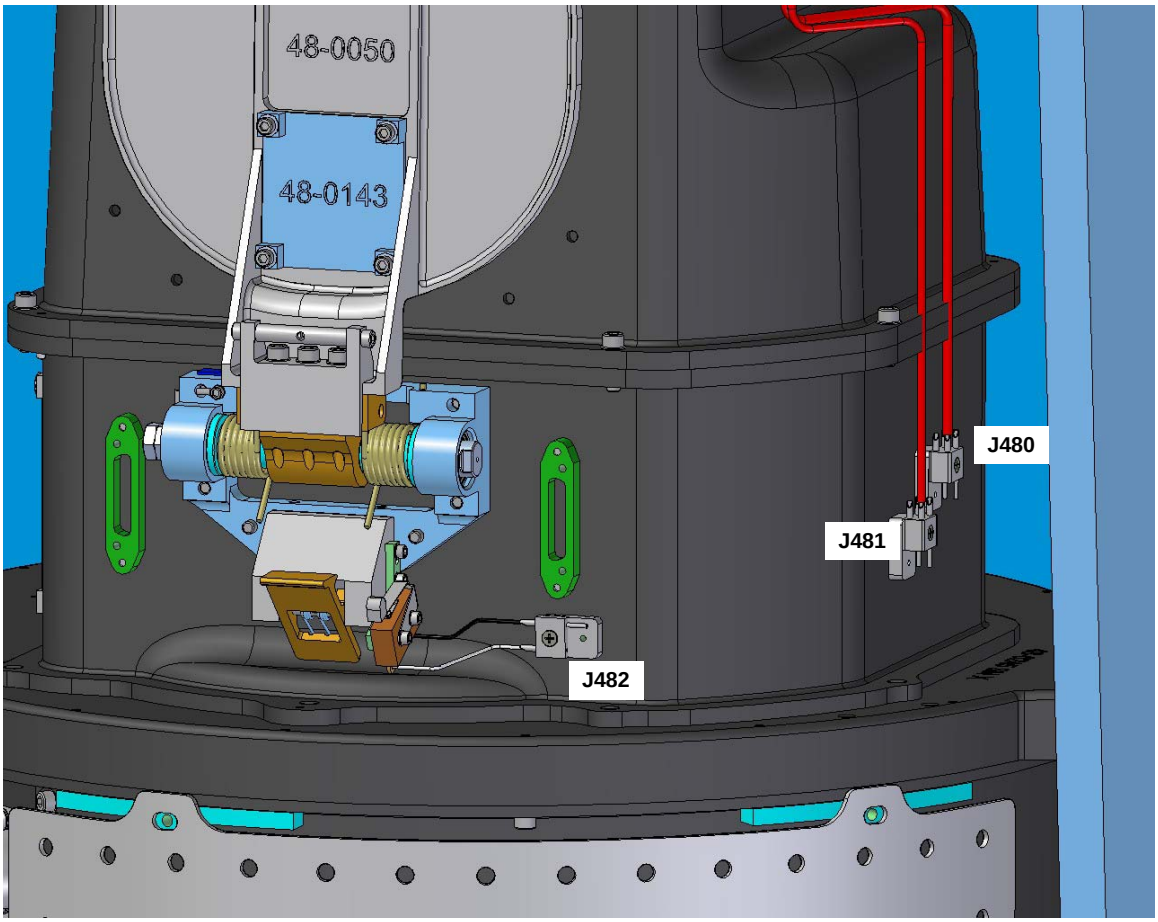


Figure 93 Instrument external connections 4

J480	48-0xxx	Pin Puller Assembly
J481	48-0xxx	Pin Puller Assembly
J482	48-0xxx	Cover Release Sensor
P480	48-0357	Release
P481	48-0357	Release
P482	48-0357	Release

Table 18 Instrument external connections 4

12.4 Instrument Internal Connections

The following figures and tables outline the internal connections on the SOFIE instrument.

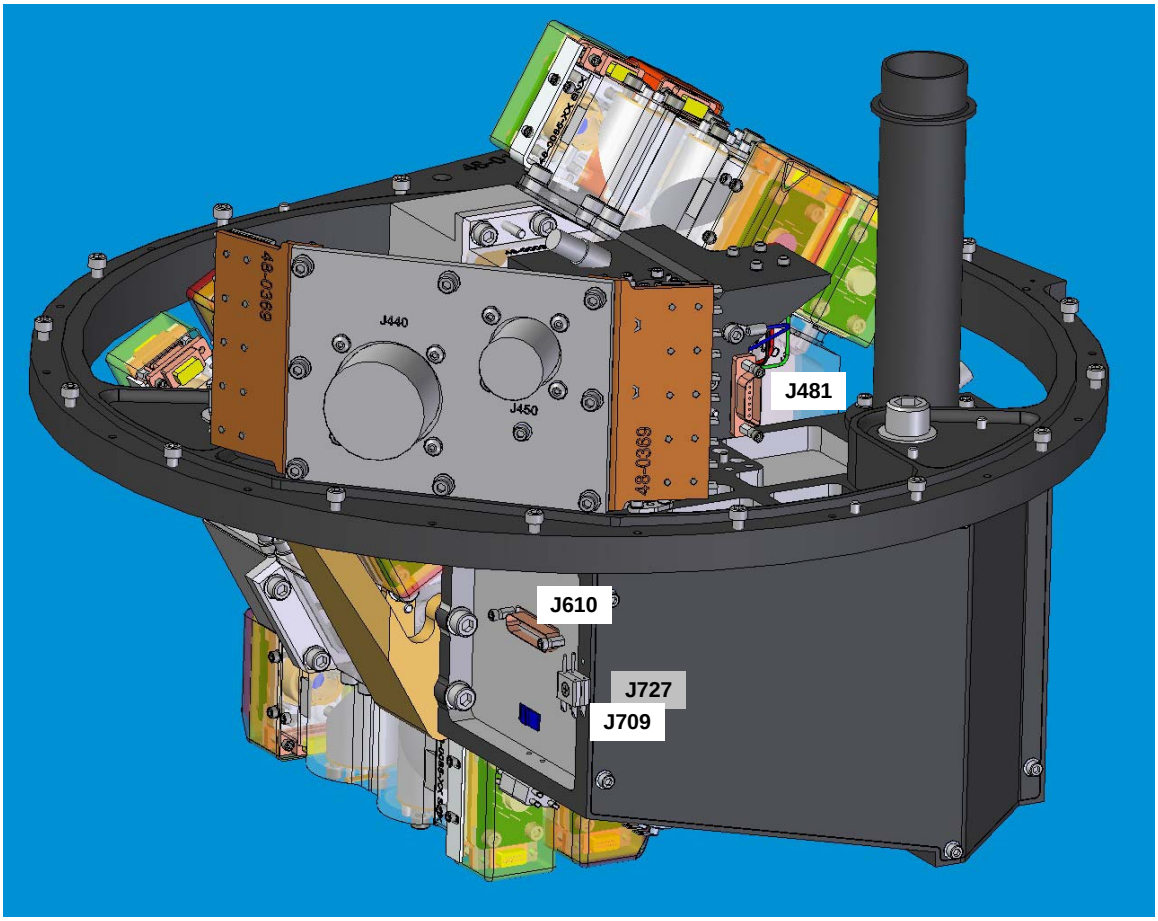


Figure 94 Instrument internal connections 1

J481	48-0xxx	Chopper, Internal
J610	48-0xxx	Sun sensor, Internal
J727	48-0535	TS[53] (EXT) Sun Sensor Module
J709	48-0366	TS[21] (EXT) Sun Sensor PCB
P481	48-0365	Chopper, Internal
P610	48-0366	Sun sensor, Internal
P727	48-0xxx	TS[53] (EXT) Sun Sensor Module
P709	48-0xxx	TS[21] (EXT) Sun Sensor PCB

Table 19 Instrument internal connections 1

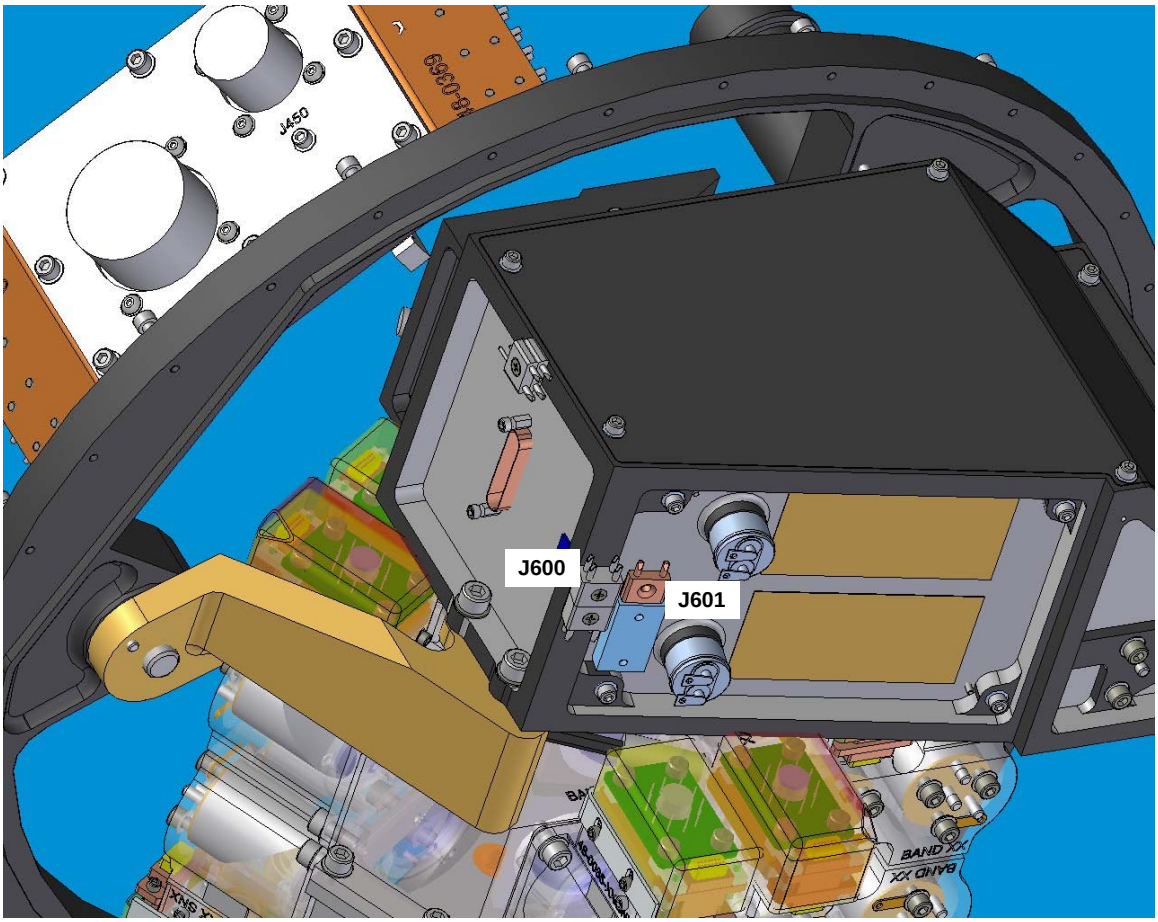


Figure 95 Instrument internal connections 2

J600	48-0535	Survival Heaters, Internal
J601	48-0535	Temperature sensor (Monitored by Spacecraft)
P600	48-0368	Survival Heaters, Internal
P601	48-0368	Temperature sensor (Monitored by Spacecraft)

Table 20 Instrument internal connections 2

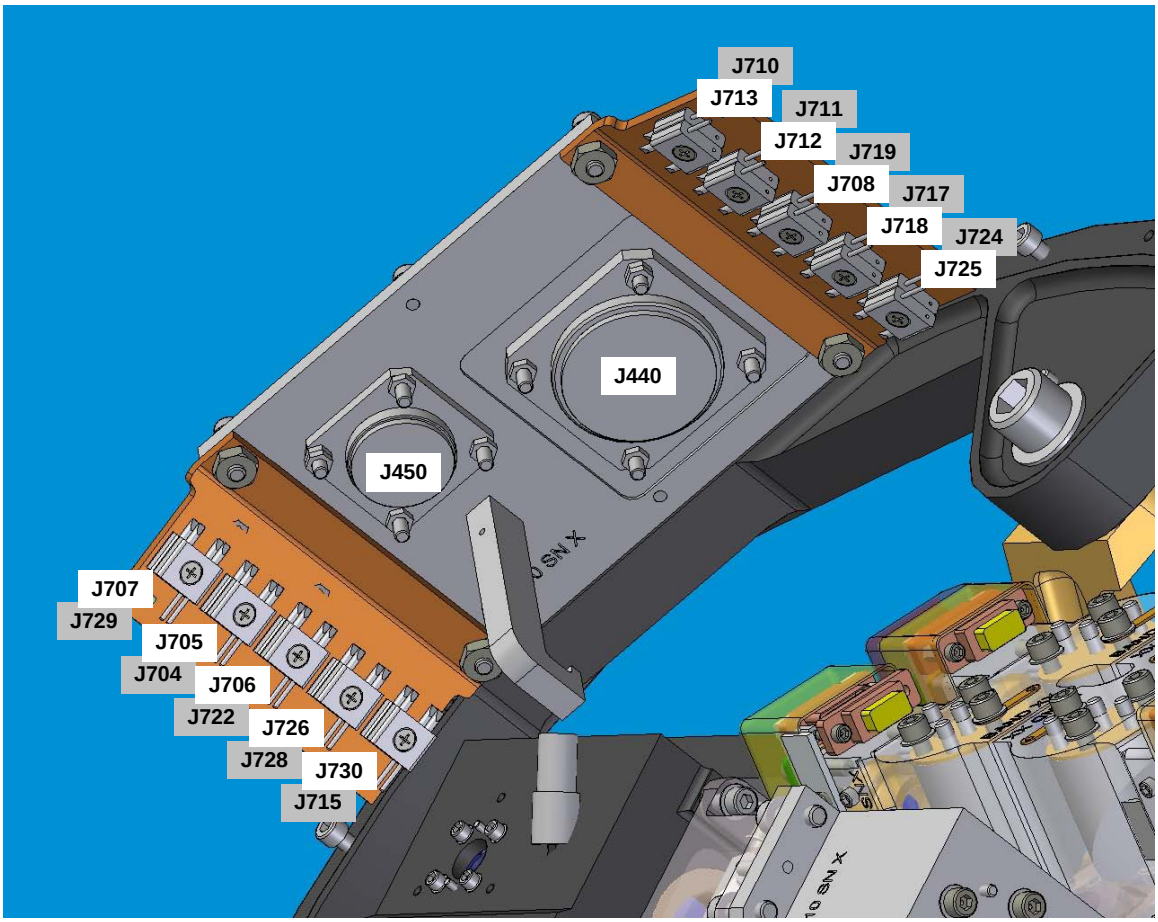


Figure 96 Instrument internal connections 3

J450	48-0365	Chopper, Internal
J440	48-0364	Data Acquistion, Internal
J710	48-0364	TS[22] (EXT) Aft Optics Bench #1
J713	48-0364	TS[25] (EXT) CSM Far Optics Module
J711	48-0364	TS[23] (EXT) Optics Housing Bands 9&11
J712	48-0364	TS[24] (EXT) Optics Housing Bands 14&16
J719	48-0364	TS[41] (EXT) Aft Optics Bench #2
J708	48-0364	TS[20] (EXT) Upper Cable Bulkhead
J717	48-0364	TS[39] (EXT) Optics Housing Bands 10&12
J718	48-0364	TS[40] (EXT) Optics Housing Bands 13&15
J724	48-0364	TS[55] (EXT) Optics Housing Bands 5&7
J725	48-0364	TS[56] (EXT) Optics Housing Bands 2&4
J707	48-0364	TS[10] (EXT) CSM Beam Splitter Assembly
J729	48-0364	TS[21] (EXT) Sun Sensor PCB
J705	48-0364	TS[8] (EXT) Optics Housing Bands 6&8
J704	48-0364	TS[7] (EXT) Optics Housing Bands 1&3
J706	48-0364	TS[9] (EXT) CSM Near Optics Module
J722	48-0364	TS[52] (EXT) Fore Optics Bench #2

J726	48-0364	TS[57] (EXT) Aft Optics Bench #3
J728	48-0364	TS[53] (EXT) Sun Sensor Module
J730	48-0364	TS[42] (EXT) Base Deck Plate
J715	48-0364	TS[36] (EXT) Mid Optics Housing
P710	48-0406	TS[22] (EXT) Aft Optics Bench #1
P713	48-0411	TS[25] (EXT) CSM Far Optics Module
P711	48-0401	TS[23] (EXT) Optics Housing Bands 9&11
P712	48-0397	TS[24] (EXT) Optics Housing Bands 14&16
P719	48-0407	TS[41] (EXT) Aft Optics Bench #2
P708	48-0xxx	TS[20] (EXT) Upper Cable Bulkhead
P717	48-0400	TS[39] (EXT) Optics Housing Bands 10&12
P718	48-0396	TS[40] (EXT) Optics Housing Bands 13&15
P724	48-0399	TS[55] (EXT) Optics Housing Bands 5&7
P725	48-0395	TS[56] (EXT) Optics Housing Bands 2&4
P707	48-0405	TS[10] (EXT) CSM Beam Splitter Assembly
P729	48-0xxx	TS[21] (EXT) Sun Sensor PCB
P705	48-0398	TS[8] (EXT) Optics Housing Bands 6&8
P704	48-0394	TS[7] (EXT) Optics Housing Bands 1&3
P706	48-0402	TS[9] (EXT) CSM Near Optics Module
P722	48-0409	TS[52] (EXT) Fore Optics Bench #2
P726	48-0408	TS[57] (EXT) Aft Optics Bench #3
P728	48-0xxx	TS[53] (EXT) Sun Sensor Module
P730	48-0xxx	TS[42] (EXT) Base Deck Plate
P715	48-0403	TS[36] (EXT) Mid Optics Housing

Table 21 Instrument internal connections 3

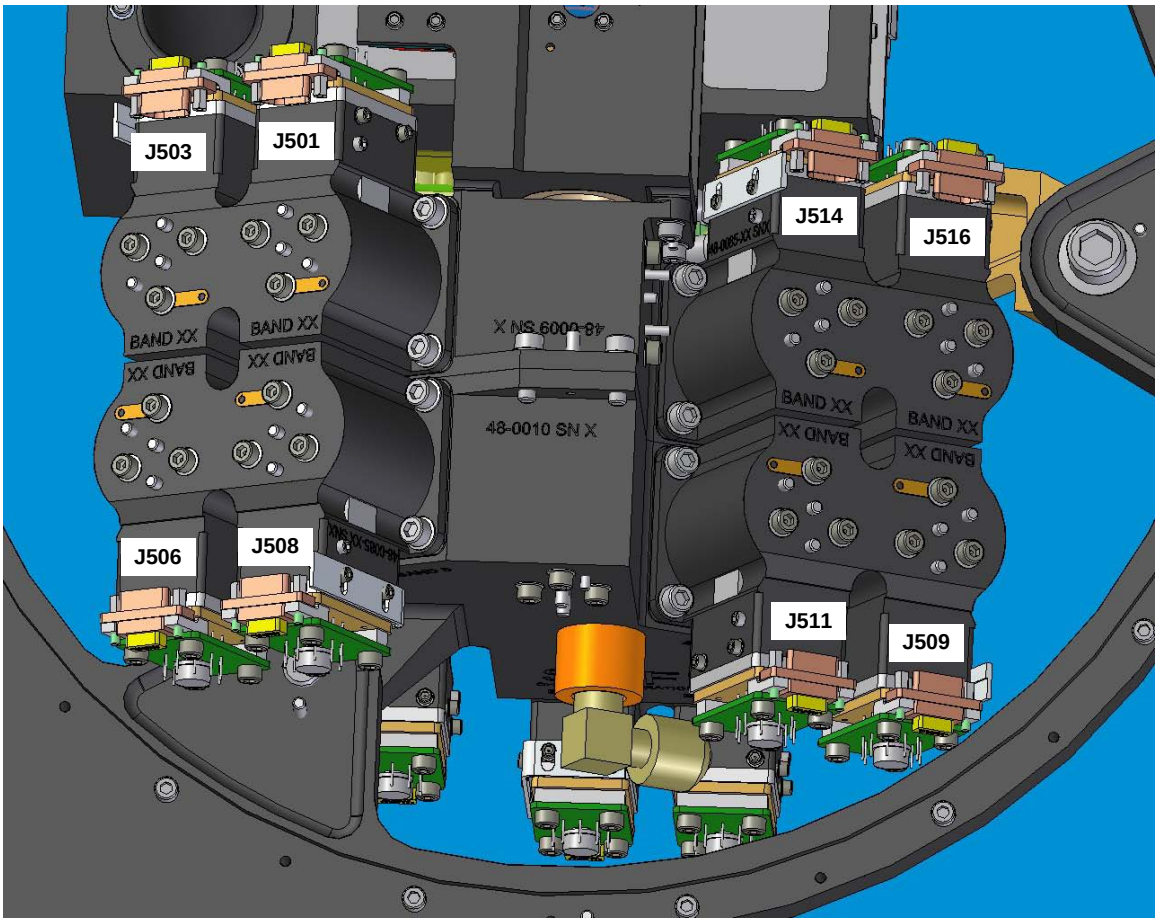


Figure 97 Instrument internal connections 4

J503	48-0xxx	Detector Assembly, Band 3
J501	48-0xxx	Detector Assembly, Band 1
J514	48-0xxx	Detector Assembly, Band 14
J516	48-0xxx	Detector Assembly, Band 16
J506	48-0xxx	Detector Assembly, Band 6
J508	48-0xxx	Detector Assembly, Band 8
J511	48-0xxx	Detector Assembly, Band 11
J509	48-0xxx	Detector Assembly, Band 9
P503	48-0362	Signal/TEC 1, Internal
P501	48-0362	Signal/TEC 1, Internal
P514	48-0363	Signal/TEC 2, Internal
P516	48-0363	Signal/TEC 2, Internal
P506	48-0362	Signal/TEC 1, Internal
P508	48-0362	Signal/TEC 1, Internal
P511	48-0363	Signal/TEC 2, Internal
P509	48-0363	Signal/TEC 2, Internal

Table 22 Instrument internal connections 4

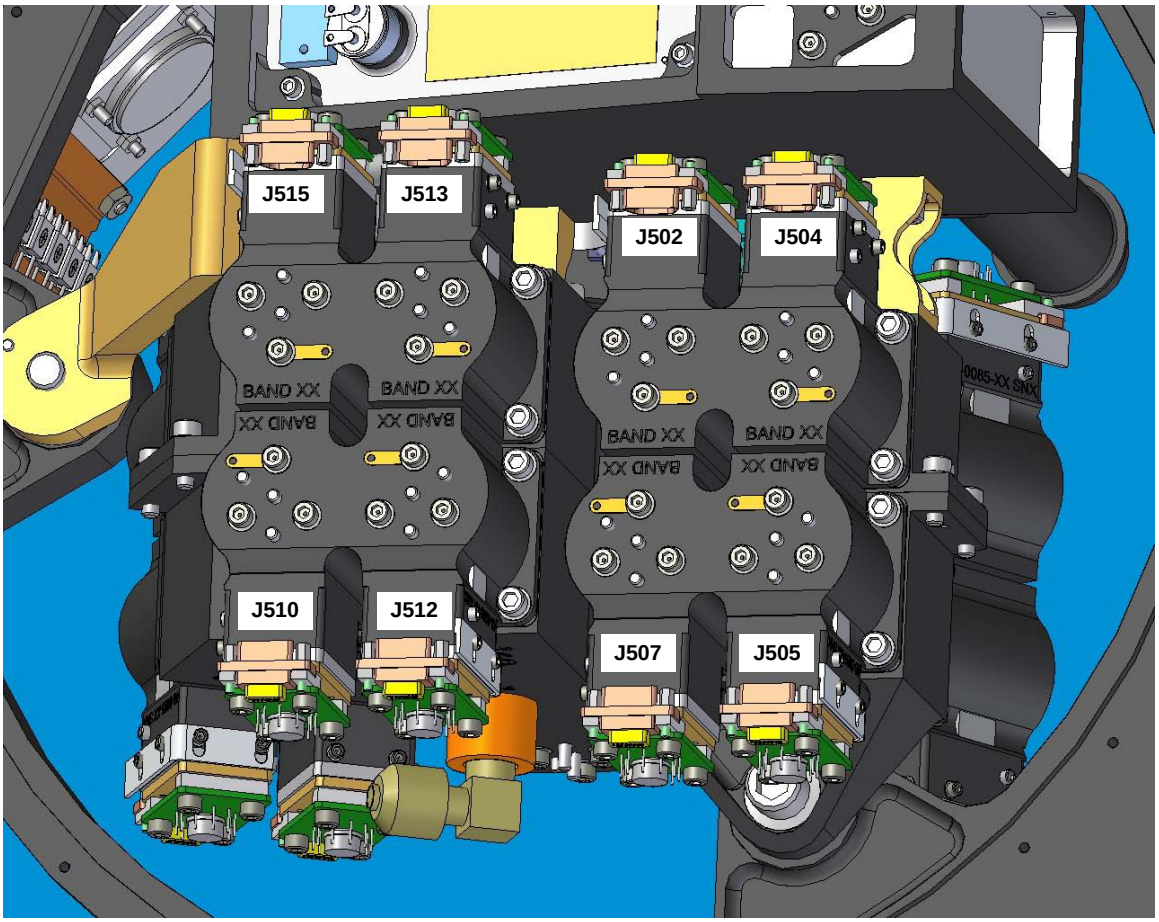


Figure 98 Instrument internal connections 5

J515	48-0xxx	Detector Assembly, Band 15
J513	48-0xxx	Detector Assembly, Band 13
J502	48-0xxx	Detector Assembly, Band 2
J504	48-0xxx	Detector Assembly, Band 4
J510	48-0xxx	Detector Assembly, Band 10
J512	48-0xxx	Detector Assembly, Band 12
J507	48-0xxx	Detector Assembly, Band 7
J505	48-0xxx	Detector Assembly, Band 5
P515	48-0363	Signal/TEC 2, Internal
P513	48-0363	Signal/TEC 2, Internal
P502	48-0362	Signal/TEC 1, Internal
P504	48-0362	Signal/TEC 1, Internal
P510	48-0363	Signal/TEC 2, Internal
P512	48-0363	Signal/TEC 2, Internal
P507	48-0362	Signal/TEC 1, Internal
P505	48-0362	Signal/TEC 1, Internal

Table 23 Instrument internal connections 5

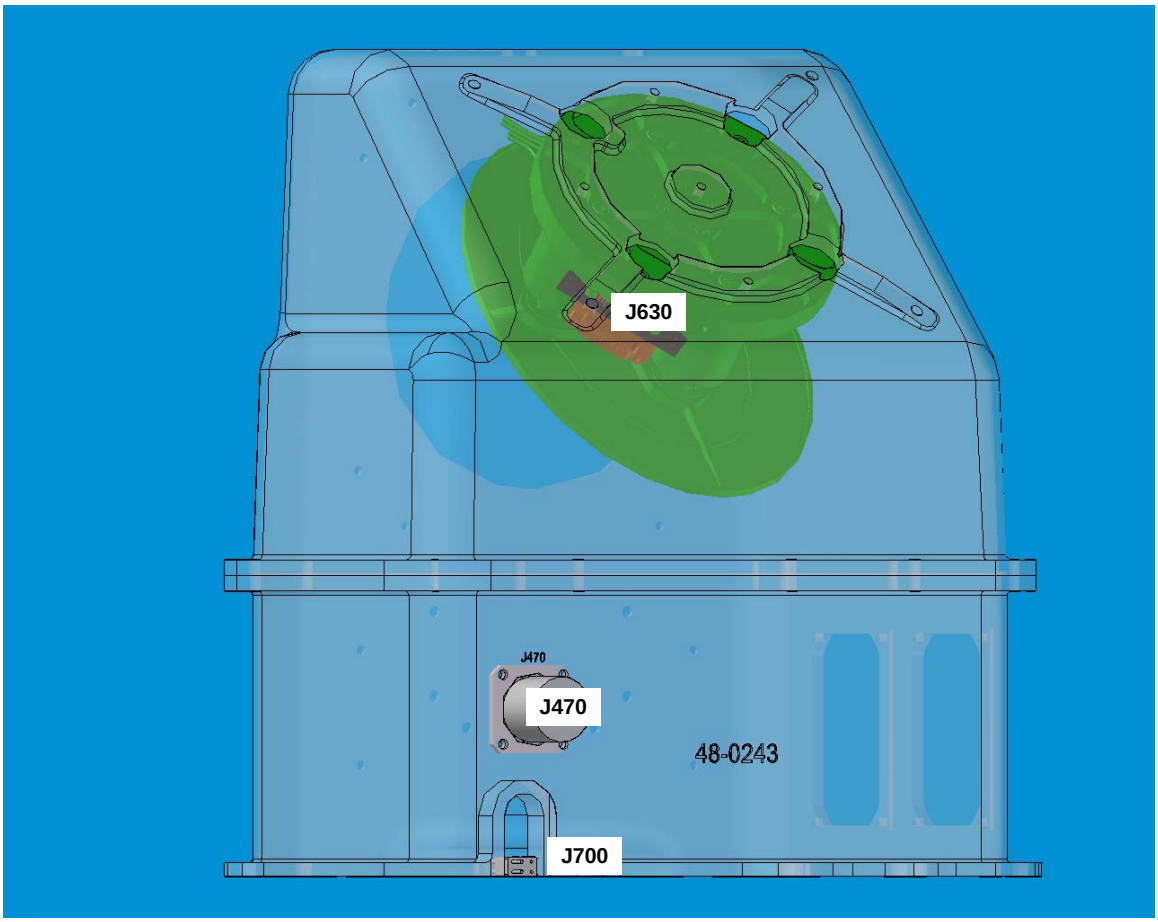


Figure 99 Instrument internal connections 6

J630		SSG Steering Mirror Assy
J470	48-0367	Motor, Internal
J700	48-0367	Motor, Internal
P630	48-0367	Motor, Internal
P470	48-0359	Motor, External
P700	48-0354	Data Acquisition, External

Table 24 Instrument internal connections 6

13. GROUND SUPPORT EQUIPMENT ICD

This section defines the components within the Ground Support Equipment and the interfaces between them. The Ground Support Equipment interface to SOFIE is the same as the Spacecraft's interface. The Ground Support Equipment also has additional monitoring interfaces to the Spacecraft Communication Bus.

13.1 Ground Support Equipment Overview

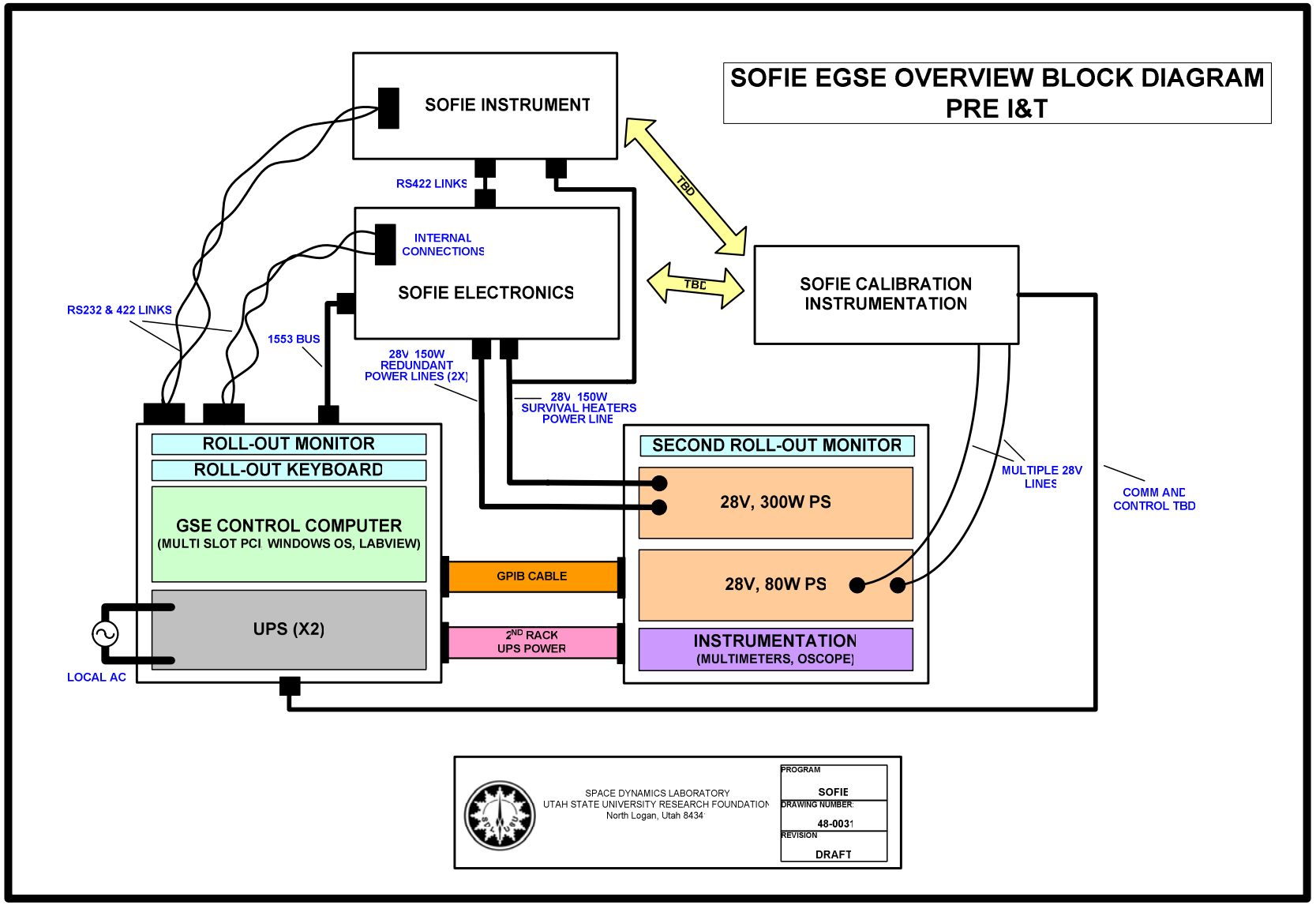


Figure 100 Ground Support Equipment Block Diagram

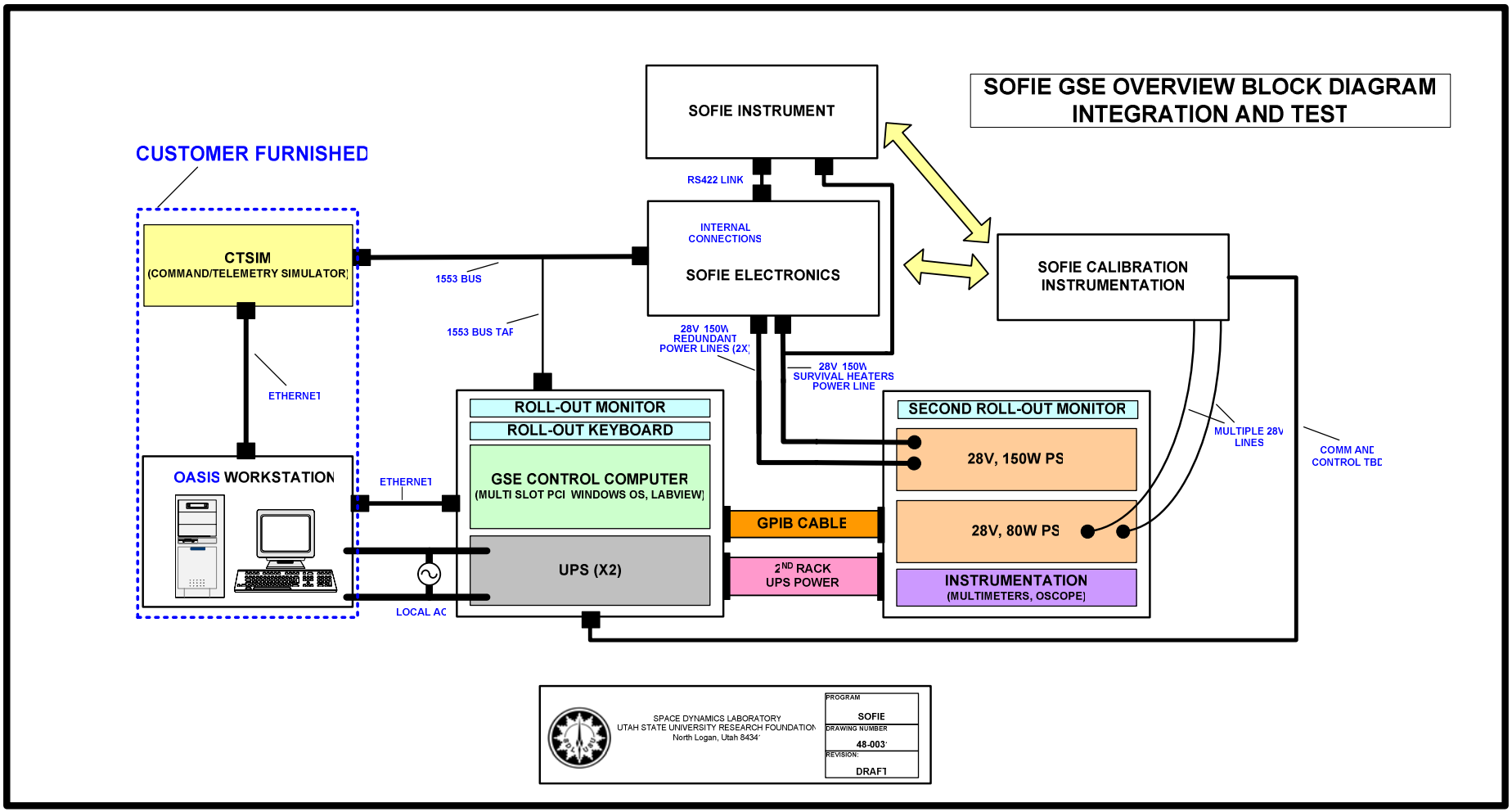


Figure 101 Ground Support Equipment Block Diagram

A depiction of the instruments in the Ground Support Equipment's equipment racks are shown in Figure 102 Ground Support Equipment Enclosure 1 Depiction and Figure 103 Ground Support Equipment Enclosure 2 Depiction.

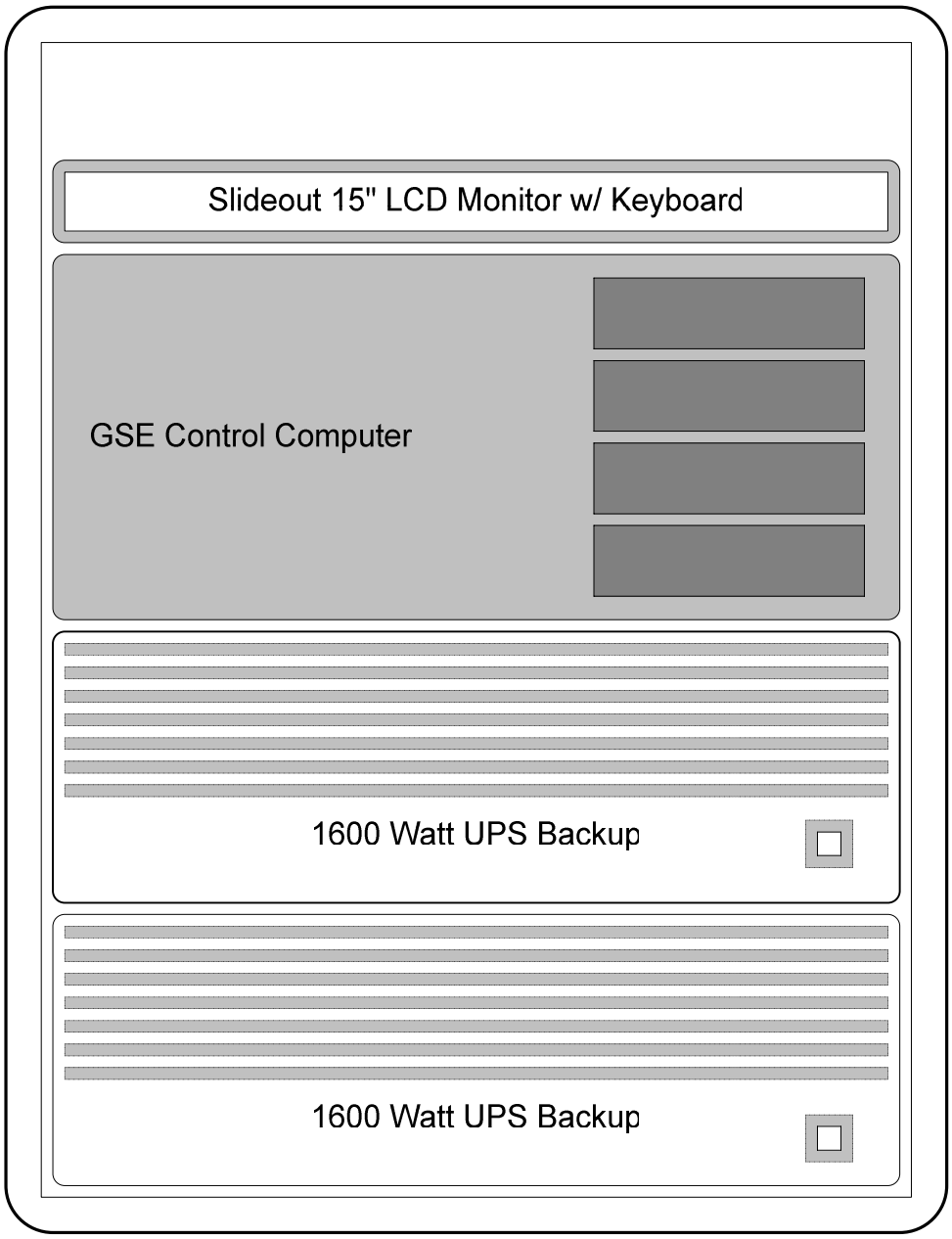


Figure 102 Ground Support Equipment Enclosure 1 Depiction

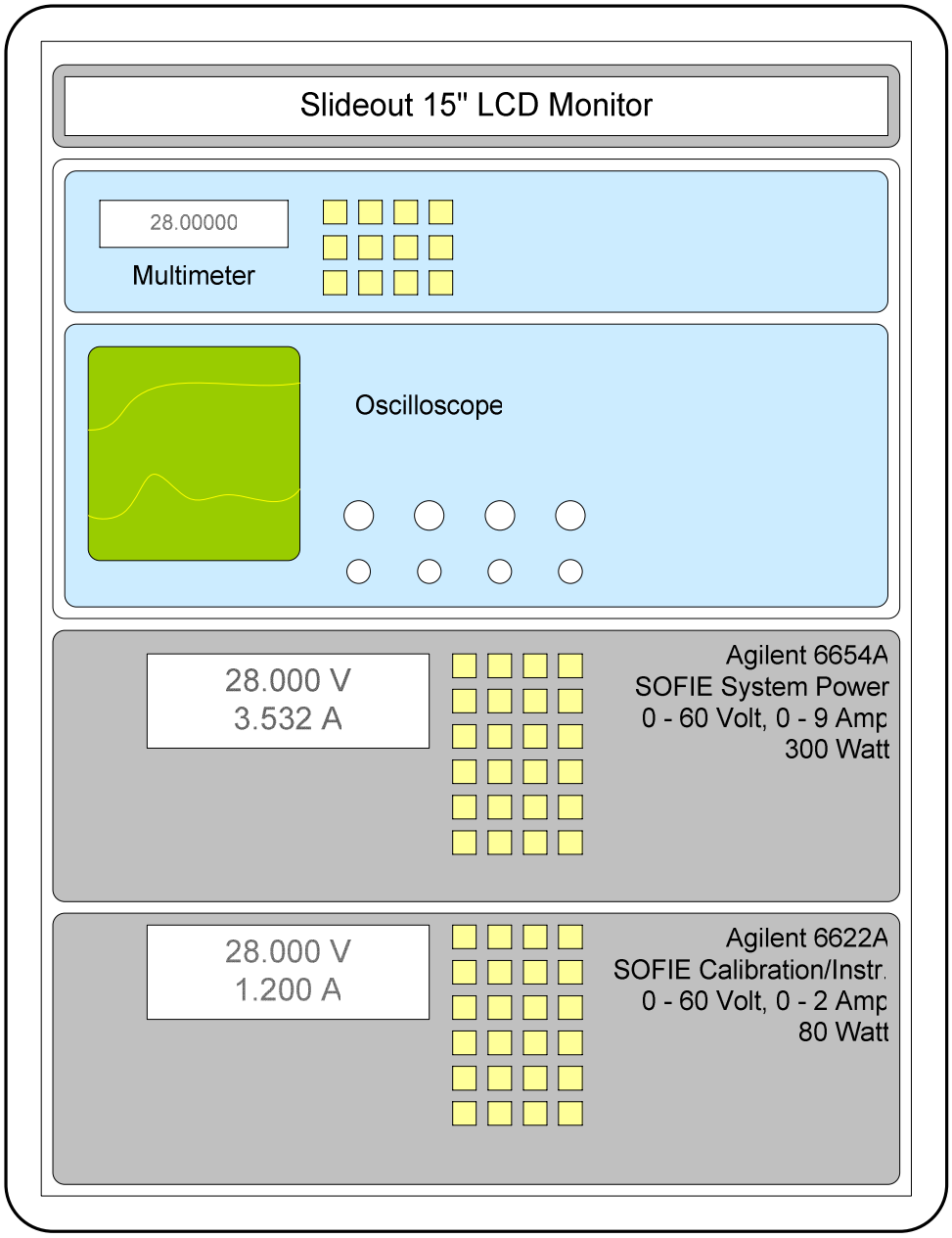


Figure 103 Ground Support Equipment Enclosure 2 Depiction

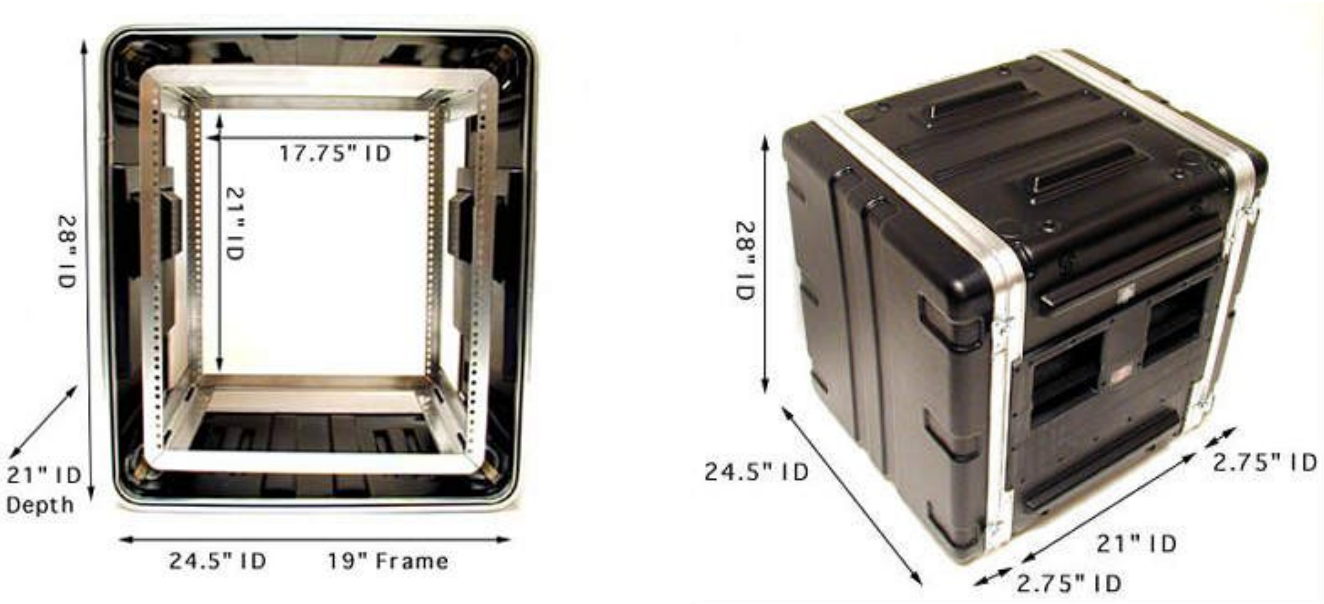


Figure 104 Support Equipment Enclosure

APPENDIX A – INSTRUMENT UNIT TEMPERATURE SENSORS

The following figures identify the name and location of the SOFIE Instrument Unit temperature sensors

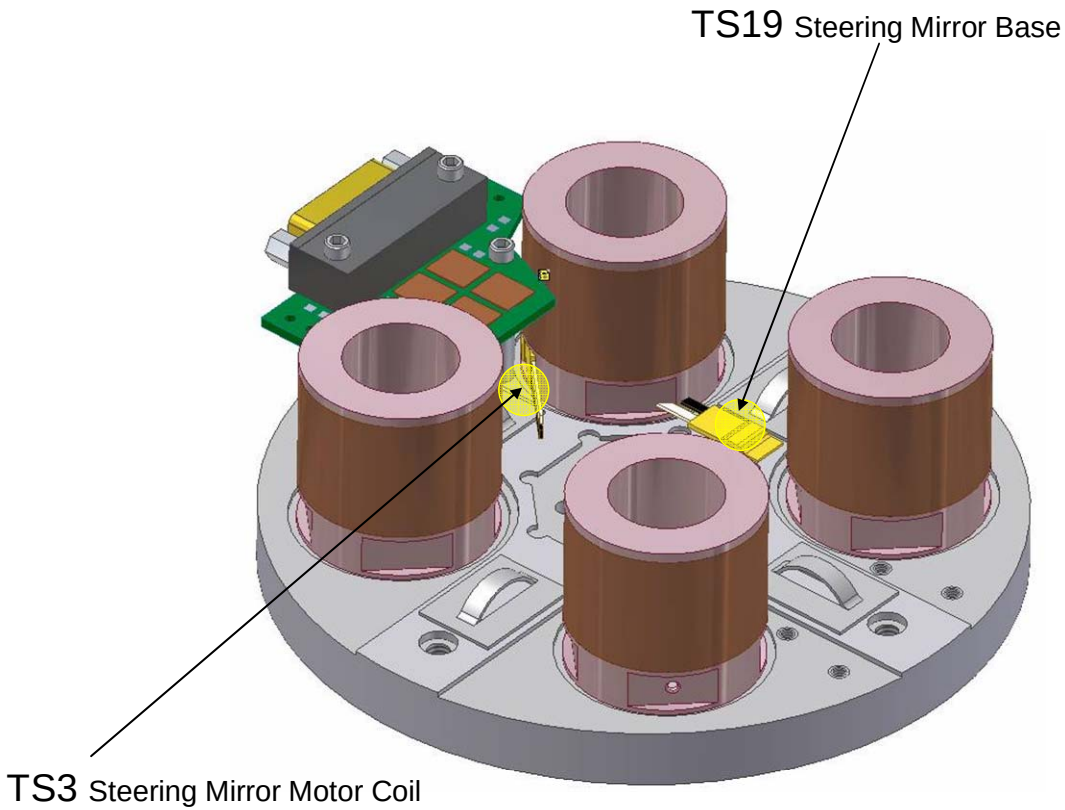


Figure 105 SOFIE PRT locations: steering mirror base

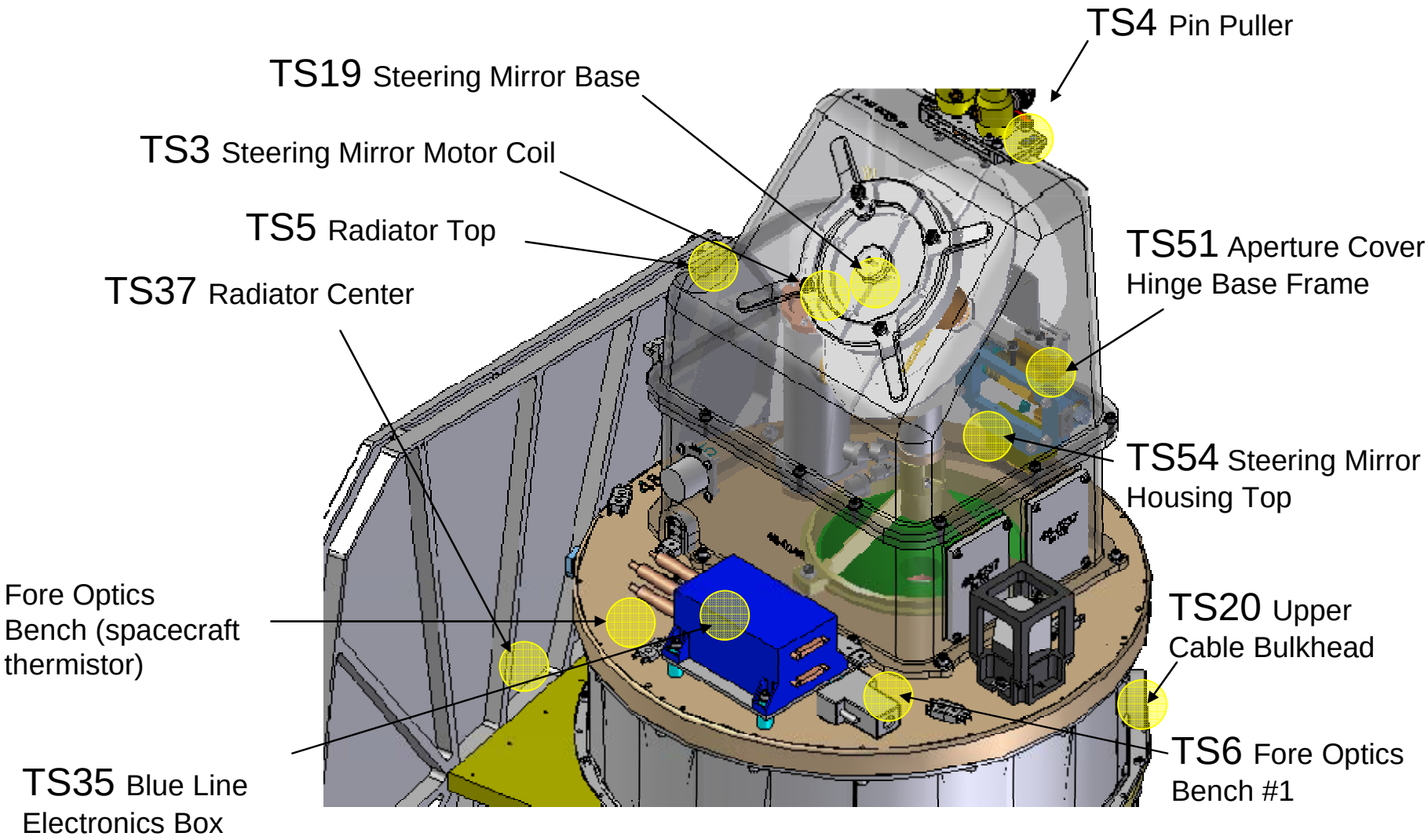


Figure 106 SOFIE PRT locations: instrument top

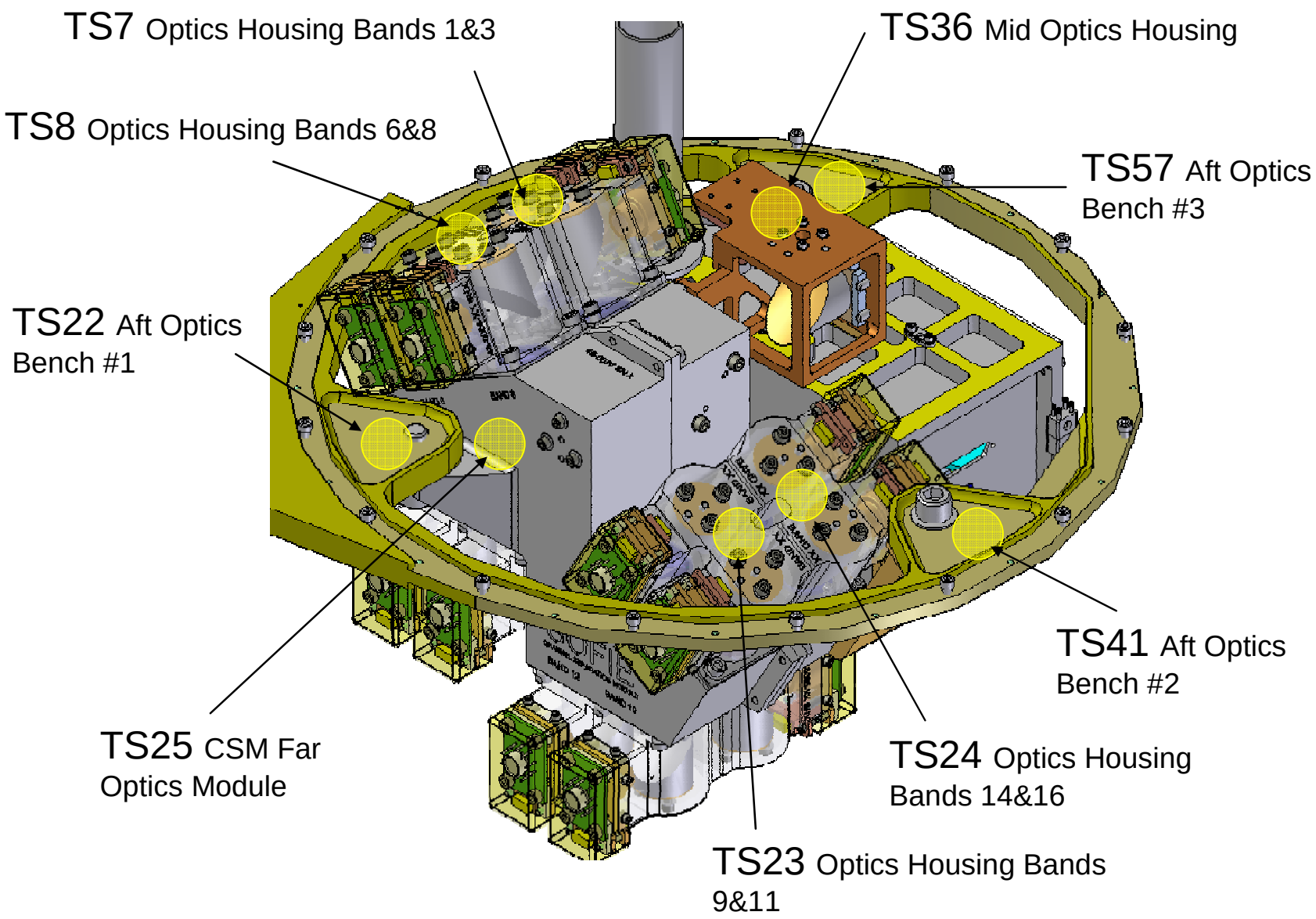


Figure 107 SOFIE PRT locations: instrument optics housing top

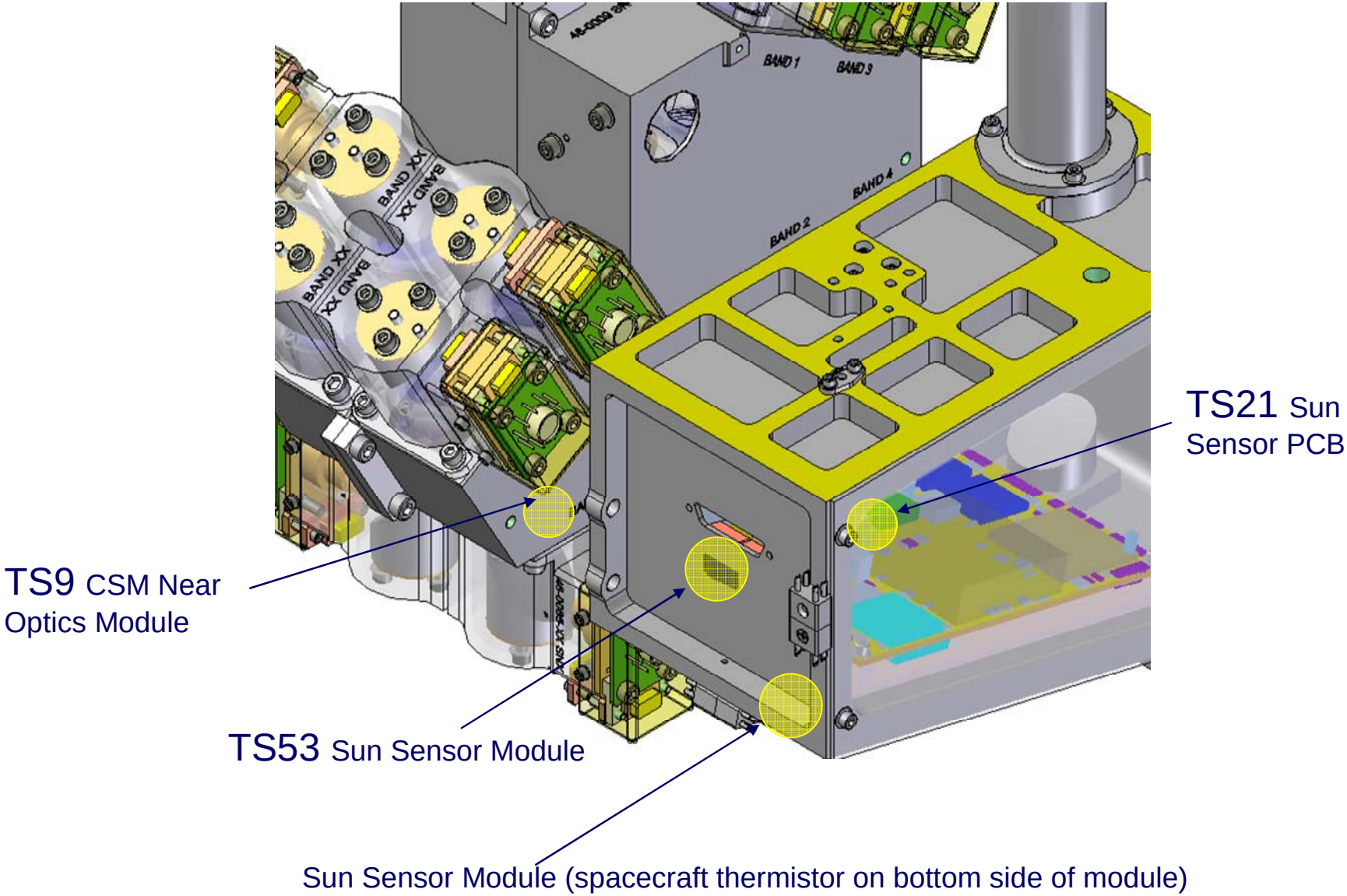


Figure 108 SOFIE PRT locations: sun sensor module

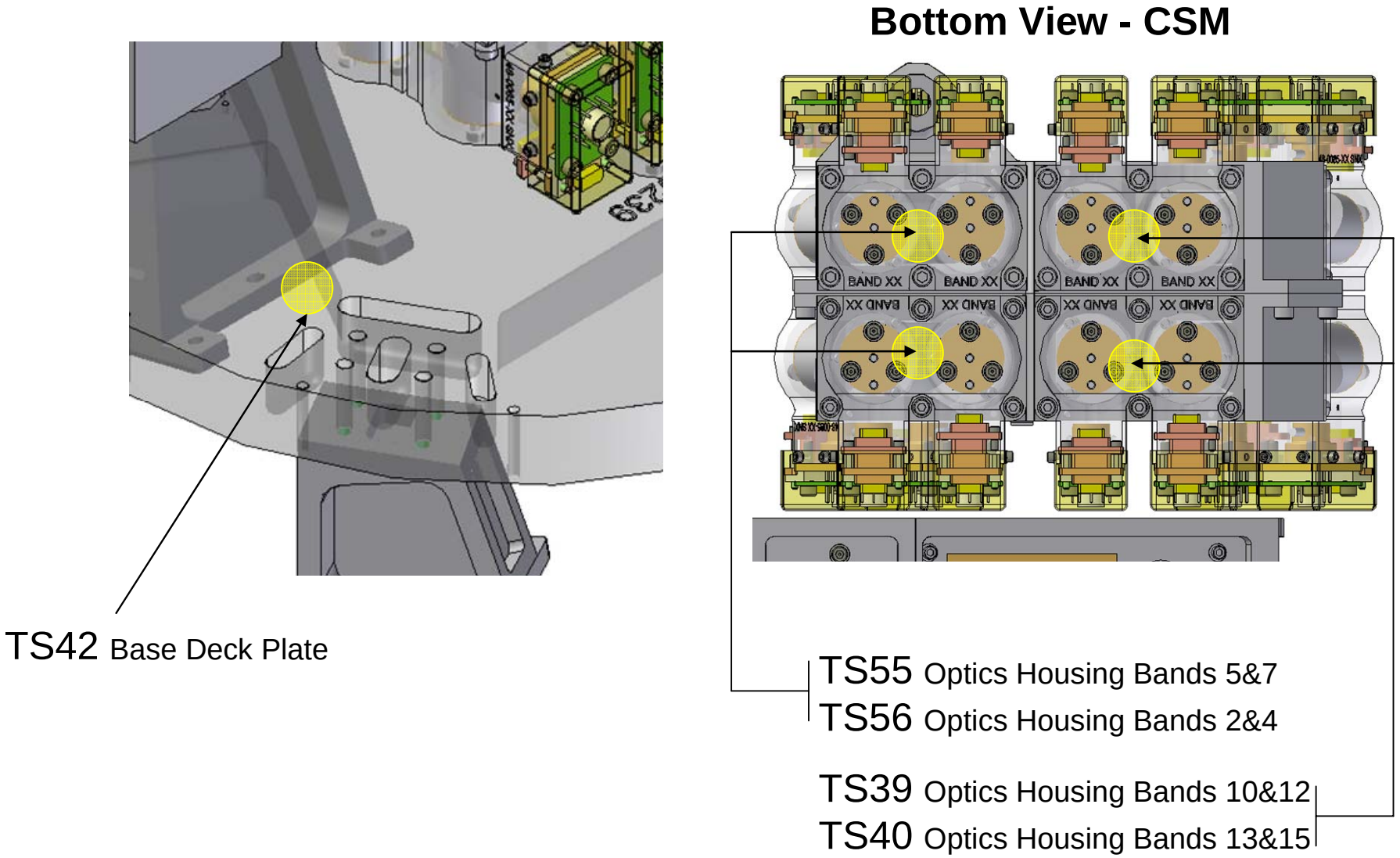


Figure 109 SOFIE PRT locations: instrument optics housing bottom / deck plate

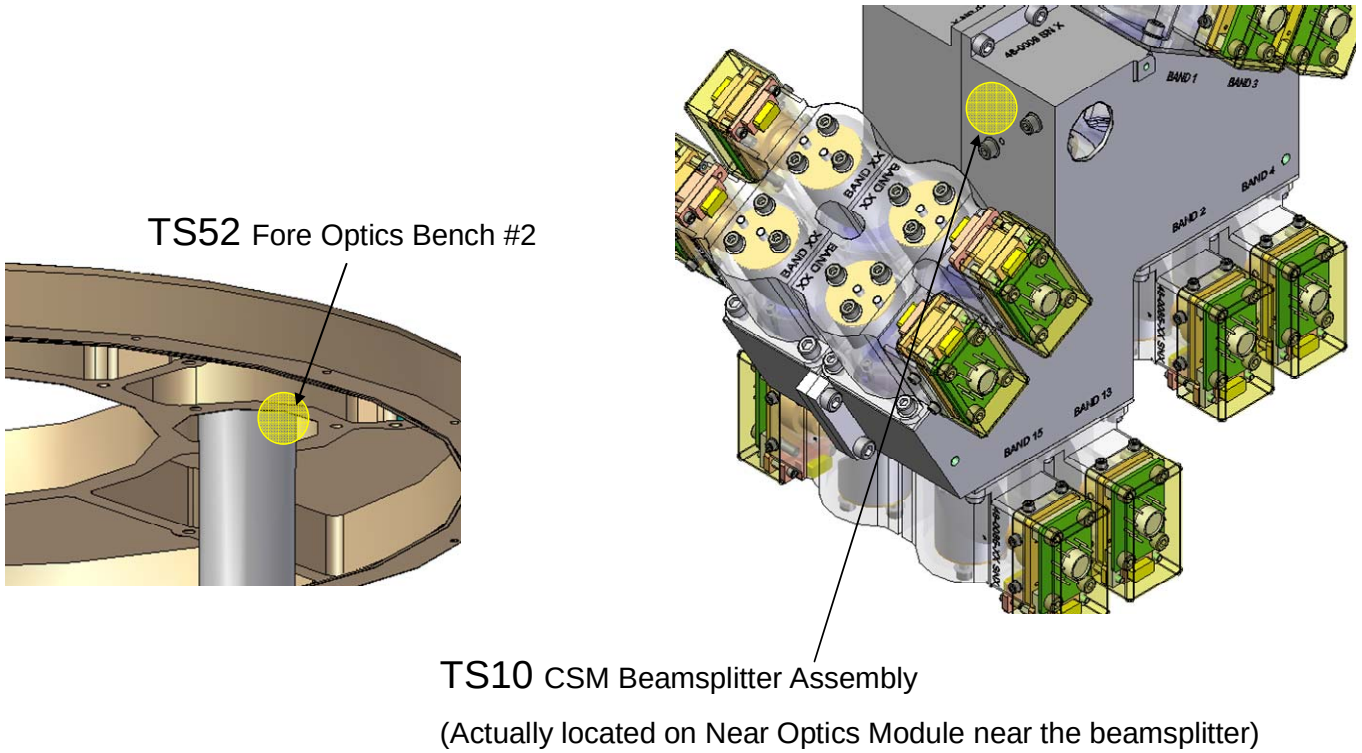


Figure 110 SOFIE PRT locations: instrument beam splitter / fore optics bench

APPENDIX B – SOFIE CABLING PIN OUTS

The following tables list the SOFIE cabling pin out configurations.

Cable Assembly: 48-0352		Signal/Tec 1 (External)	
Connector	**P300**	**Part Number**	**GS83513/04-B16N-429**
Pin 1	(-)12V	Pin 9	(+)12V
Pin 2	AGND	Pin 10	AGND
Pin 3	DET6Sig(+)	Pin 11	DET6Sig(-)
Pin 4	DET6Bias	Pin 12	AGND(Bias)
Pin 5	DET6ThermA	Pin 13	AGND(Therm)
Pin 6	DET6ThermB	Pin 14	TEC(-)
Pin 7	TEC(+)	Pin 15	TEC(-)
Pin 8	TEC(+)		
Connector	**P301**	**Part Number**	**GS83513/04-B16N-429**
Pin 1	-12V	Pin 9	+12V
Pin 2	AGND	Pin 10	AGND
Pin 3	DET5Sig+	Pin 11	DET5Sig(-)
Pin 4	DET5Bias	Pin 12	AGND(Bias)
Pin 5	DET5ThermA	Pin 13	AGND
Pin 6	DET5ThermB	Pin 14	TEC(-)
Pin 7	TEC(+)	Pin 15	TEC(-)
Pin 8	TEC(+)		
Connector	**P302**	**Part Number**	**GS83513/04-B16N-429**
Pin 1	-12V	Pin 9	+12V
Pin 2	AGND	Pin 10	AGND
Pin 3	DET2Sig+	Pin 11	DET2Sig(-)
Pin 4	DET2Bias	Pin 12	AGND(Bias)
Pin 5	DET2ThermA	Pin 13	AGND
Pin 6	DET2ThermB	Pin 14	TEC(-)
Pin 7	TEC(+)	Pin 15	TEC(-)
Pin 8	TEC(+)		
Connector	**P303**	**Part Number**	**GS83513/04-B16N-429**
Pin 1	-12V	Pin 9	+12V
Pin 2	AGND	Pin 10	AGND
Pin 3	DET1Sig+	Pin 11	DET1Sig(-)
Pin 4	DET1Bias	Pin 12	AGND(Bias)
Pin 5	DET1ThermA	Pin 13	AGND
Pin 6	DET1ThermB	Pin 14	TEC(-)
Pin 7	TEC(+)	Pin 15	TEC(-)
Pin 8	TEC(+)		
Connector	**P320**	**Part Number**	**GS83513/04-B16N-429**
Pin 1	-12V	Pin 9	+12V
Pin 2	AGND	Pin 10	AGND

Pin 3	DET8Sig+	Pin 11	DET8Sig(-)
Pin 4	DET8Bias	Pin 12	AGND(Bias)
Pin 5	DET8ThermA	Pin 13	AGND
Pin 6	DET8ThermB	Pin 14	TEC(-)
Pin 7	TEC(+)	Pin 15	TEC(-)
Pin 8	TEC(+)		
Connector	**P321**	**Part Number**	**GS83513/04-B16N-429**
Pin 1	-12V	Pin 9	+12V
Pin 2	AGND	Pin 10	AGND
Pin 3	DET7Sig+	Pin 11	DET7Sig(-)
Pin 4	DET7Bias	Pin 12	AGND(Bias)
Pin 5	DET7ThermA	Pin 13	AGND
Pin 6	DET7ThermB	Pin 14	TEC(-)
Pin 7	TEC(+)	Pin 15	TEC(-)
Pin 8	TEC(+)		
Connector	**P322**	**Part Number**	**GS83513/04-B16N-429**
Pin 1	-12V	Pin 9	+12V
Pin 2	AGND	Pin 10	AGND
Pin 3	DET4Sig+	Pin 11	DET4Sig(-)
Pin 4	DET4Bias	Pin 12	AGND(Bias)
Pin 5	DET4ThermA	Pin 13	AGND
Pin 6	DET4ThermB	Pin 14	TEC(-)
Pin 7	TEC(+)	Pin 15	TEC(-)
Pin 8	TEC(+)		
Connector	**P323**	**Part Number**	**GS83513/04-B16N-429**
Pin 1	-12V	Pin 9	+12V
Pin 2	AGND	Pin 10	AGND
Pin 3	DET3Sig+	Pin 11	DET3Sig(-)
Pin 4	DET3Bias	Pin 12	AGND(Bias)
Pin 5	DET3ThermA	Pin 13	AGND
Pin 6	DET3ThermB	Pin 14	TEC(-)
Pin 7	TEC(+)	Pin 15	TEC(-)
Pin 8	TEC(+)		
Connector	**P400**	**Part Number**	**MS27467T25F35S**
Pin 1	SPARE	Pin 46	TEC(+)
Pin 2	DET8ThermA	Pin 47	SPARE
Pin 3	DET8ThermB	Pin 48	AGND
Pin 4	AGND	Pin 49	AGND
Pin 5	DET7ThermA	Pin 50	AGND
Pin 6	DET7ThermB	Pin 51	AGND
Pin 7	AGND	Pin 52	AGND
Pin 8	DET6ThermA	Pin 53	AGND
Pin 9	DET6Sig(+)	Pin 54	AGND
Pin 10	DET8Sig(+)	Pin 55	AGND
Pin 11	DET8Sig(-)	Pin 56	DET5Bias
Pin 12	DET7Sig(+)	Pin 57	TEC(+)
Pin 13	DET7Sig(-)	Pin 58	TEC(-)

Pin 14	SPARE	Pin 59	(+)12V
Pin 15	DET6ThermB	Pin 60	(-)12V
Pin 16	AGND	Pin 61	(-)12V
Pin 17	DET6Sig(-)	Pin 62	(+)12V
Pin 18	TEC(+)	Pin 63	(+)12V
Pin 19	TEC(+)	Pin 64	(-)12V
Pin 20	TEC(-)	Pin 65	(-)12V
Pin 21	TEC(-)	Pin 66	(+)12V
Pin 22	DET5ThermA	Pin 67	AGND
Pin 23	DET5ThermB	Pin 68	AGND
Pin 24	AGND	Pin 69	TEC(-)
Pin 25	DET6Bias	Pin 70	DET4ThermA
Pin 26	TEC(+)	Pin 71	(+)12V
Pin 27	TEC(+)	Pin 72	(-)12V
Pin 28	TEC(-)	Pin 73	(-)12V
Pin 29	TEC(-)	Pin 74	(+)12V
Pin 30	TEC(+)	Pin 75	DET1ThermA
Pin 31	TEC(+)	Pin 76	(-)12V
Pin 32	TEC(+)	Pin 77	(+)12V
Pin 33	TEC(+)	Pin 78	DET2ThermA
Pin 34	DET5Sig(+)	Pin 79	(+)12V
Pin 35	SPARE	Pin 80	AGND
Pin 36	AGND	Pin 81	AGND
Pin 37	TEC(-)	Pin 82	DET3ThermA
Pin 38	TEC(-)	Pin 83	AGND
Pin 39	DET8Bias	Pin 84	AGND
Pin 40	AGND	Pin 85	AGND
Pin 41	DET7Bias	Pin 86	AGND
Pin 42	AGND	Pin 87	AGND
Pin 43	TEC(-)	Pin 88	AGND
Pin 44	TEC(-)	Pin 89	AGND
Pin 45	DET5Sig(-)	Pin 90	DET2ThermB
Connector	**P400 (cont)**	**Part Number**	**MS27467T25F35S**
Pin 91	(-)12V	Pin 110	DET1Sig(+)
Pin 92	AGND	Pin 111	TEC(-)
Pin 93	DET4ThermB	Pin 112	TEC(-)
Pin 94	DET3ThermB	Pin 113	AGND
Pin 95	DET3Sig(-)	Pin 114	DET4Sig(+)
Pin 96	DET3Sig(+)	Pin 115	TEC(-)
Pin 97	AGND	Pin 116	TEC(-)
Pin 98	DET1Bias	Pin 117	TEC(+)
Pin 99	DET1ThermB	Pin 118	TEC(+)
Pin 100	TEC(+)	Pin 119	DET1Sig(-)
Pin 101	TEC(+)	Pin 120	DET2Sig(-)
Pin 102	AGND	Pin 121	DET2Bias
Pin 103	DET4Sig(-)	Pin 122	TEC(+)
Pin 104	DET4Bias	Pin 123	TEC(+)
Pin 105	AGND	Pin 124	SPARE

Pin 106	DET3Bias	Pin 125	SPARE
Pin 107	AGND	Pin 126	SPARE
Pin 108	TEC(-)	Pin 127	SPARE
Pin 109	TEC(-)	Pin 128	DET2Sig(+)

Table 25 Cable Assembly: 48-0352 Signal/TEC 1 (External)

Cable Assembly: 48-0353		Signal/Tec 2 (External)	
Connector	**P330**	**Part Number**	**GS83513/04-B16N-429**
Pin 1	(-)12V	Pin 9	(+)12V
Pin 2	AGND	Pin 10	AGND
Pin 3	DET14Sig(+)	Pin 11	DET14Sig(-)
Pin 4	DET14Bias	Pin 12	AGND(Bias)
Pin 5	DET14ThermA	Pin 13	AGND(Therm)
Pin 6	DET14ThermB	Pin 14	TEC(-)
Pin 7	TEC(+)	Pin 15	TEC(-)
Pin 8	TEC(+)		
Connector	**P331**	**Part Number**	**GS83513/04-B16N-429**
Pin 1	-12V	Pin 9	+12V
Pin 2	AGND	Pin 10	AGND
Pin 3	DET13Sig+	Pin 11	DET13Sig(-)
Pin 4	DET13Bias	Pin 12	AGND(Bias)
Pin 5	DET13ThermA	Pin 13	AGND
Pin 6	DET13ThermB	Pin 14	TEC(-)
Pin 7	TEC(+)	Pin 15	TEC(-)
Pin 8	TEC(+)		
Connector	**P332**	**Part Number**	**GS83513/04-B16N-429**
Pin 1	-12V	Pin 9	+12V
Pin 2	AGND	Pin 10	AGND
Pin 3	DET10Sig+	Pin 11	DET10Sig(-)
Pin 4	DET10Bias	Pin 12	AGND(Bias)
Pin 5	DET10ThermA	Pin 13	AGND
Pin 6	DET10ThermB	Pin 14	TEC(-)
Pin 7	TEC(+)	Pin 15	TEC(-)
Pin 8	TEC(+)		
Connector	**P333**	**Part Number**	**GS83513/04-B16N-429**
Pin 1	-12V	Pin 9	+12V
Pin 2	AGND	Pin 10	AGND
Pin 3	DET9Sig+	Pin 11	DET9Sig(-)
Pin 4	DET9Bias	Pin 12	AGND(Bias)
Pin 5	DET9ThermA	Pin 13	AGND
Pin 6	DET9ThermB	Pin 14	TEC(-)
Pin 7	TEC(+)	Pin 15	TEC(-)
Pin 8	TEC(+)		
Connector	**P350**	**Part Number**	**GS83513/04-B16N-429**
Pin 1	-12V	Pin 9	+12V
Pin 2	AGND	Pin 10	AGND
Pin 3	DET16Sig+	Pin 11	DET16Sig(-)
Pin 4	DET16Bias	Pin 12	AGND(Bias)
Pin 5	DET16ThermA	Pin 13	AGND
Pin 6	DET16ThermB	Pin 14	TEC(-)
Pin 7	TEC(+)	Pin 15	TEC(-)
Pin 8	TEC(+)		

Connector	**P351**	**Part Number**	**GS83513/04-B16N-429**
Pin 1	-12V	Pin 9	+12V
Pin 2	AGND	Pin 10	AGND
Pin 3	DET15Sig+	Pin 11	DET15Sig(-)
Pin 4	DET15Bias	Pin 12	AGND(Bias)
Pin 5	DET15ThermA	Pin 13	AGND
Pin 6	DET15ThermB	Pin 14	TEC(-)
Pin 7	TEC(+)	Pin 15	TEC(-)
Pin 8	TEC(+)		
Connector	**P352**	**Part Number**	**GS83513/04-B16N-429**
Pin 1	-12V	Pin 9	+12V
Pin 2	AGND	Pin 10	AGND
Pin 3	DET12Sig+	Pin 11	DET12Sig(-)
Pin 4	DET12Bias	Pin 12	AGND(Bias)
Pin 5	DET12ThermA	Pin 13	AGND
Pin 6	DET12ThermB	Pin 14	TEC(-)
Pin 7	TEC(+)	Pin 15	TEC(-)
Pin 8	TEC(+)		
Connector	**P353**	**Part Number**	**GS83513/04-B16N-429**
Pin 1	-12V	Pin 9	+12V
Pin 2	AGND	Pin 10	AGND
Pin 3	DET11Sig+	Pin 11	DET11Sig(-)
Pin 4	DET11Bias	Pin 12	AGND(Bias)
Pin 5	DET11ThermA	Pin 13	AGND
Pin 6	DET11ThermB	Pin 14	TEC(-)
Pin 7	TEC(+)	Pin 15	TEC(-)
Pin 8	TEC(+)		
Connector	**P420**	**Part Number**	**MS27467T25F35SA**
Pin 1	SPARE	Pin 46	TEC(+)
Pin 2	DET9ThermA	Pin 47	SPARE
Pin 3	DET9ThermB	Pin 48	AGND
Pin 4	AGND	Pin 49	AGND
Pin 5	DET10ThermA	Pin 50	AGND
Pin 6	DET10ThermB	Pin 51	AGND
Pin 7	AGND	Pin 52	AGND
Pin 8	DET11ThermA	Pin 53	AGND
Pin 9	DET11Sig(+)	Pin 54	AGND
Pin 10	DET9Sig(+)	Pin 55	AGND
Pin 11	DET9Sig(-)	Pin 56	DET12Bias
Pin 12	DET10Sig(+)	Pin 57	TEC(+)
Pin 13	DET10Sig(-)	Pin 58	TEC(-)
Pin 14	SPARE	Pin 59	(+)12V
Pin 15	DET11ThermB	Pin 60	(-)12V
Pin 16	AGND	Pin 61	(-)12V
Pin 17	DET11Sig(-)	Pin 62	(+)12V
Pin 18	TEC(+)	Pin 63	(+)12V
Pin 19	TEC(+)	Pin 64	(-)12V

Pin 20	TEC(-)	Pin 65	(-)12V
Pin 21	TEC(-)	Pin 66	(+)12V
Pin 22	DET12ThermA	Pin 67	AGND
Pin 23	DET12ThermB	Pin 68	AGND
Pin 24	AGND	Pin 69	TEC(-)
Pin 25	DET11Bias	Pin 70	DET13ThermA
Pin 26	TEC(+)	Pin 71	(+)12V
Pin 27	TEC(+)	Pin 72	(-)12V
Pin 28	TEC(-)	Pin 73	(-)12V
Pin 29	TEC(-)	Pin 74	(+)12V
Pin 30	TEC(+)	Pin 75	DET16ThermA
Pin 31	TEC(+)	Pin 76	(-)12V
Pin 32	TEC(+)	Pin 77	(+)12V
Pin 33	TEC(+)	Pin 78	DET15ThermA
Pin 34	DET12Sig(+)	Pin 79	(+)12V
Pin 35	SPARE	Pin 80	AGND
Pin 36	AGND	Pin 81	AGND
Pin 37	TEC(-)	Pin 82	DET14ThermA
Pin 38	TEC(-)	Pin 83	AGND
Pin 39	DET9Bias	Pin 84	AGND
Pin 40	AGND	Pin 85	AGND
Pin 41	DET10Bias	Pin 86	AGND
Pin 42	AGND	Pin 87	AGND
Pin 43	TEC(-)	Pin 88	AGND
Pin 44	TEC(-)	Pin 89	AGND
Pin 45	DET12Sig(-)	Pin 90	DET15ThermB
Connector	**P420 (cont)**	**Part Number**	**MS27467T25F35SA**
Pin 91	(-)12V	Pin 110	DET16Sig(+)
Pin 92	AGND	Pin 111	TEC(-)
Pin 93	DET13ThermB	Pin 112	TEC(-)
Pin 94	DET14ThermB	Pin 113	AGND
Pin 95	DET14Sig(-)	Pin 114	DET13Sig(+)
Pin 96	DET14Sig(+)	Pin 115	TEC(-)
Pin 97	AGND	Pin 116	TEC(-)
Pin 98	DET16Bias	Pin 117	TEC(+)
Pin 99	DET16ThermB	Pin 118	TEC(+)
Pin 100	TEC(+)	Pin 119	DET16Sig(-)
Pin 101	TEC(+)	Pin 120	DET15Sig(-)
Pin 102	AGND	Pin 121	DET15Bias
Pin 103	DET13Sig(-)	Pin 122	TEC(+)
Pin 104	DET13Bias	Pin 123	TEC(+)
Pin 105	AGND	Pin 124	SPARE
Pin 106	DET14Bias	Pin 125	SPARE
Pin 107	AGND	Pin 126	SPARE
Pin 108	TEC(-)	Pin 127	SPARE
Pin 109	TEC(-)	Pin 128	DET15Sig(+)

Table 26 Cable Assembly: 48-0353 Signal/TEC 2 (External)

Cable Assembly: 48-0354		Data Acquisition (External)	
Connector	**P310**	**Part Number**	**GS83513/04-F16N-429**
Pin 1	TS[19]+ (EXT) Steering Mirror Base	Pin 20	TS[19]- (EXT) Steering Mirror Base
Pin 2	TS[20]+ (EXT) Upper Cable Bulkhead	Pin 21	TS[20]- (EXT) Upper Cable Bulkhead
Pin 3	TS[21]+ (EXT) Sun Sensor PCB	Pin 22	TS[21]- (EXT) Sun Sensor PCB
Pin 4	TS[22]+ (EXT) Aft Optics Bench #1	Pin 23	TS[22]- (EXT) Aft Optics Bench #1
Pin 5	TS[23]+ (EXT) Optics Housing Bands 9&11	Pin 24	TS[23]- (EXT) Optics Housing Bands 9&11
Pin 6	TS[24]+ (EXT) Optics Housing Bands 14&16	Pin 25	TS[24]- (EXT) Optics Housing Bands 14&16
Pin 7	TS[25]+ (EXT) CSM Far Optics Module	Pin 26	TS[25]- (EXT) CSM Far Optics Module
Pin 8	SPARE	Pin 27	SPARE
Pin 9	SPARE	Pin 28	SPARE
Pin 10	SPARE	Pin 29	SPARE
Pin 11	SPARE	Pin 30	TS[3]- (EXT) Steering Mirror Motor Coil
Pin 12	TS[3]+ (EXT) Steering Mirror Motor Coil	Pin 31	TS[4]- (EXT) Pin Puller
Pin 13	TS[4]+ (EXT) Pin Puller	Pin 32	TS[5]- (EXT) Radiator Top
Pin 14	TS[5]+ (EXT) Radiator Top	Pin 33	TS[6]- (EXT) Fore Optics Bench #1
Pin 15	TS[6]+ (EXT) Fore Optics Bench #1	Pin 34	TS[7]- (EXT) Optics Housing Bands 1&3
Pin 16	TS[7]+ (EXT) Optics Housing Bands 1&3	Pin 35	TS[8]- (EXT) Optics Housing Bands 6&8
Pin 17	TS[8]+ (EXT) Optics Housing Bands 6&8	Pin 36	TS[9]- (EXT) CSM Near Optics Module
Pin 18	TS[9]+ (EXT) CSM Near Optics Module	Pin 37	TS[10]- (EXT) CSM Beam Splitter Assembly
Pin 19	TS[10]+ (EXT) CSM Beam Splitter Assembly		
Connector	**P340**	**Part Number**	**GS83513/04-F16N-429**
Pin 1	TS[51]+ (EXT) Aperture Cover Hinge Base Frame	Pin 20	TS[51]- (EXT) Aperture Cover Hinge Base Frame
Pin 2	TS[52]+ (EXT) Fore Optics Bench #2	Pin 21	TS[52]- (EXT) Fore Optics Bench #2
Pin 3	TS[53]+ (EXT) Sun Sensor Module	Pin 22	TS[53]- (EXT) Sun Sensor Module
Pin 4	TS[54]+ (EXT) Steering Mirror Housing Top	Pin 23	TS[54]- (EXT) Steering Mirror Housing Top
Pin 5	TS[55]+ (EXT) Optics Housing Bands 5&7	Pin 24	TS[55]- (EXT) Optics Housing Bands 5&7
Pin 6	TS[56]+ (EXT) Optics Housing Bands 2&4	Pin 25	TS[56]- (EXT) Optics Housing Bands 2&4

Pin 7	TS[57]+ (EXT) Aft Optics Bench #3	Pin 26	TS[57]- (EXT) Aft Optics Bench #3
Pin 8	SPARE	Pin 27	SPARE
Pin 9	SPARE	Pin 28	SPARE
Pin 10	SPARE	Pin 29	SPARE
Pin 11	SPARE	Pin 30	TS[35]- (EXT) Blue Line Electronics Box
Pin 12	TS[35]+ (EXT) Blue Line Electronics Box	Pin 31	TS[36]- (EXT) Mid Optics Housing
Pin 13	TS[36]+ (EXT) Mid Optics Housing	Pin 32	TS[37]- (EXT) Radiator Center
Pin 14	TS[37]+ (EXT) Radiator Center	Pin 33	TS[38]- (EXT) Spare
Pin 15	TS[38]+ (EXT) Spare	Pin 34	TS[39]- (EXT) Optics Housing Bands 10&12
Pin 16	TS[39]+ (EXT) Optics Housing Bands 10&12	Pin 35	TS[40]- (EXT) Optics Housing Bands 13&15
Pin 17	TS[40]+ (EXT) Optics Housing Bands 13&15	Pin 36	TS[41]- (EXT) Aft Optics Bench #2
Pin 18	TS[41]+ (EXT) Aft Optics Bench #2	Pin 37	TS[42]- (EXT) Base Deck Plate
Pin 19	TS[42]+ (EXT) Base Deck Plate		
Connector	**P440**	**Part Number**	**MS27467T21F35S**
Pin 1	SPARE	Pin 28	NC
Pin 2	SPARE	Pin 29	NC
Pin 3	SPARE	Pin 30	TS[10]- (EXT) CSM Beam Splitter Assembly
Pin 4	SPARE	Pin 31	TS[10]+ (EXT) CSM Beam Splitter Assembly
Pin 5	SPARE	Pin 32	TS[7]- (EXT) Optics Housing Bands 1&3
Pin 6	SPARE	Pin 33	TS[7]+ (EXT) Optics Housing Bands 1&3
Pin 7	SPARE	Pin 34	TS[52]- (EXT) Fore Optics Bench #2
Pin 8	NC	Pin 35	TS[52]+ (EXT) Fore Optics Bench #2
Pin 9	NC	Pin 36	TS[36]- (EXT) Mid Optics Housing
Pin 10	NC	Pin 37	TS[36]+ (EXT) Mid Optics Housing
Pin 11	NC	Pin 38	TS[42]- (EXT) Base Deck Plate
Pin 12	NC	Pin 39	TS[42]+ (EXT) Base Deck Plate
Pin 13	NC	Pin 40	NC
Pin 14	NC	Pin 41	TS[56]+ (EXT) Optics Housing Bands 2&4
Pin 15	SPARE	Pin 42	TS[56]- (EXT) Optics Housing Bands 2&4

Pin 16	SPARE	Pin 43	TS[55]+ (EXT) Optics Housing Bands 5&7
Pin 17	SPARE	Pin 44	TS[55]- (EXT) Optics Housing Bands 5&7
Pin 18	SPARE	Pin 45	TS[41]+ (EXT) Aft Optics Bench #2
Pin 19	SPARE	Pin 46	TS[41]- (EXT) Aft Optics Bench #2
Pin 20	SPARE	Pin 47	TS[23]+ (EXT) Optics Housing Bands 9&11
Pin 21	SPARE	Pin 48	TS[23]- (EXT) Optics Housing Bands 9&11
Pin 22	NC	Pin 49	TS[22]+ (EXT) Aft Optics Bench #1
Pin 23	NC	Pin 50	TS[22]- (EXT) Aft Optics Bench #1
Pin 24	NC	Pin 51	NC
Pin 25	NC	Pin 52	TS[21]- (EXT) Sun Sensor PCB
Pin 26	NC	Pin 53	TS[21]+ (EXT) Sun Sensor PCB
Pin 27	NC	Pin 54	TS[9]- (EXT) CSM Near Optics Module
Pin 28	NC	Pin 55	TS[9]+ (EXT) CSM Near Optics Module
Connector	**P440 (cont)**	**Part Number**	**MS27467T21F35S**
Pin 56	TS[53]- (EXT) Sun Sensor Module	Pin 68	TS[8]- (EXT) Optics Housing Bands 6&8
Pin 57	TS[53]+ (EXT) Sun Sensor Module	Pin 69	TS[8]+ (EXT) Optics Housing Bands 6&8
Pin 58	NC	Pin 70	TS[57]- (EXT) Aft Optics Bench #3
Pin 59	TS[38]+ (EXT) SPARE	Pin 71	TS[57]+ (EXT) Aft Optics Bench #3
Pin 60	TS[38]- (EXT) SPARE	Pin 72	SPARE
Pin 61	TS[40]+ (EXT) Optics Housing Bands 13&15	Pin 73	TS[39]+ (EXT) Optics Housing Bands 10&12
Pin 62	TS[40]- (EXT) Optics Housing Bands 13&15	Pin 74	TS[39]- (EXT) Optics Housing Bands 10&12
Pin 63	TS[20]+ (EXT) Upper Cable Bulkhead	Pin 75	TS[24]+ (EXT) Optics Housing Bands 14&16
Pin 64	TS[20]- (EXT) Upper Cable Bulkhead	Pin 76	TS[24]- (EXT) Optics Housing Bands 14&16
Pin 65	TS[25]+ (EXT) CSM Far Optics Module	Pin 77	NC
Pin 66	TS[25]- (EXT) CSM Far Optics Module	Pin 78	NC
Pin 67	NC	Pin 79	NC
Connector	**P700**	**Part Number**	**JF2S2P45AB**

Pin A	TS[3]+ (EXT) Steering Mirror Motor Coil	Pin B	TS[19]+ (EXT) Steering Mirror Base
Pin C	TS[3]- (EXT) Steering Mirror Motor Coil	Pin D	TS[19]- (EXT) Steering Mirror Base
Connector	**P701**	**Part Number**	**JF1S1P45A**
Pin A	TS[4]+ (EXT) Pin Puller	Pin B	TS[4]- (EXT) Pin Puller
Connector	**P702**	**Part Number**	**JF2S2P45AB**
Pin A	TS[5]+ (EXT) Radiator Top	Pin B	TS[37]+ (EXT) Radiator Center
Pin C	TS[5]- (EXT) Radiator Top	Pin D	TS[37]- (EXT) Radiator Center
Connector	**P703**	**Part Number**	**JF1S1P45A**
Pin A	TS[6]+ (EXT) Fore Optics Bench #1	Pin B	TS[6]- (EXT) Fore Optics Bench #1
Connector	**P714**	**Part Number**	**JF1S1P45A**
Pin A	TS[35]+ (EXT) Blue Line Electronics Box	Pin B	TS[35]- (EXT) Blue Line Electronics Box
Connector	**P721**	**Part Number**	**JF1S1P45A**
Pin A	TS[51]+ (EXT) Aperture Cover Hinge Base Frame	Pin B	TS[51]- (EXT) Aperture Cover Hinge Base Frame
Connector	**P723**	**Part Number**	**JF1S1P45A**
Pin A	TS[22]+ (EXT) Aft Optics Bench #1	Pin B	TS[22]- (EXT) Aft Optics Bench #1
Connector	**J711**	**Part Number**	**JF1S1P45A**
Pin A	TS[23]+ (EXT) Optics Housing Bands 9&11	Pin B	TS[23]- (EXT) Optics Housing Bands 9&11
Connector	**J712**	**Part Number**	**JF1S1P45A**
Pin A	TS[24]+ (EXT) Optics Housing Bands 14&16	Pin B	TS[24]- (EXT) Optics Housing Bands 14&16
Connector	**J713**	**Part Number**	**JF1S1P45A**
Pin A	TS[25]+ (EXT) CSM Far Optics Module	Pin B	TS[25]- (EXT) CSM Far Optics Module
Connector	**J715**	**Part Number**	**JF1S1P45A**
Pin A	TS[36]+ (EXT) Mid Optics Housing	Pin B	TS[36]- (EXT) Mid Optics Housing
Connector	**J717**	**Part Number**	**JF1S1P45A**
Pin A	TS[39]+ (EXT) Optics Housing Bands 10&12	Pin B	TS[39]- (EXT) Optics Housing Bands 10&12
Connector	**J718**	**Part Number**	**JF1S1P45A**
Pin A	TS[40]+ (EXT) Optics Housing Bands 13&15	Pin B	TS[40]- (EXT) Optics Housing Bands 13&15
Connector	**J719**	**Part Number**	**JF1S1P45A**
Pin A	TS[41]+ (EXT) Aft Optics Bench #2	Pin B	TS[41]- (EXT) Aft Optics Bench #2
Connector	**J722**	**Part Number**	**JF1S1P45A**
Pin A	TS[52]+ (EXT) Fore Optics	Pin B	TS[52]- (EXT) Fore Optics

	Bench #2		Bench #2
Connector	**J724**	**Part Number**	**JF1S1P45A**
Pin A	TS[55]+ (EXT) Optics Housing Bands 5&7	Pin B	TS[55]- (EXT) Optics Housing Bands 5&7
Connector	**J725**	**Part Number**	**JF1S1P45A**
Pin A	TS[56]+ (EXT) Optics Housing Bands 2&4	Pin B	TS[56]- (EXT) Optics Housing Bands 2&4
Connector	**J726**	**Part Number**	**JF1S1P45A**
Pin A	TS[57]+ (EXT) Aft Optics Bench #3	Pin B	TS[57]- (EXT) Aft Optics Bench #3
Connector	**J728**	**Part Number**	**JF1S1P45A**
Pin A	TS[53]+ (EXT) Sun Sensor Module	Pin B	TS[53]- (EXT) Sun Sensor Module
Connector	**J729**	**Part Number**	**JF1S1P45A**
Pin A	TS[21]+ (EXT) Sun Sensor PCB	Pin B	TS[21]- (EXT) Sun Sensor PCB
Connector	**J730**	**Part Number**	**JF1S1P45A**
Pin A	TS[42]+ (EXT) Base Deck Plate	Pin B	TS[42]- (EXT) Base Deck Plate

Table 27 Cable Assembly: 48-0354 Data Acquisition (External)

Cable Assembly: 48-0355		Chopper (External)	
Connector	**P360**	**Part Number**	**GS83513/04-C16N-429**
Pin 1	CHOP_SENSE_R +	Pin 12	CHOP_SENSE_R -
Pin 2	CHOP_SENSE_R +	Pin 13	CHOP_SENSE_R -
Pin 3	SPARE	Pin 14	SPARE
Pin 4	CHOP_DRV_R +	Pin 15	CHOP_DRV_R -
Pin 5	CHOP_DRV_R +	Pin 16	CHOP_DRV_R -
Pin 6	SPARE	Pin 17	CHOP_DRV_L -
Pin 7	CHOP_DRV_L +	Pin 18	CHOP_DRV_L -
Pin 8	CHOP_DRV_L +	Pin 19	SPARE
Pin 9	SPARE	Pin 20	CHOP_SENSE_L +
Pin 10	CHOP_SENSE_L -	Pin 21	CHOP_SENSE_L +
Pin 11	CHOP_SENSE_L -		
Connector	**P450**	**Part Number**	**MS27467T13F35S**
Pin 1	CHOP_SENSE_R +	Pin 12	CHOP_DRV_L +
Pin 2	CGND	Pin 13	CGND
Pin 3	CHOP_DRV_R +	Pin 14	CHOP_SENSE_R +
Pin 4	CHOP_DRV_R +	Pin 15	CHOP_SENSE_R -
Pin 5	CGND	Pin 16	CHOP_DRV_R -
Pin 6	CHOP_SENSE_L +	Pin 17	CHOP_DRV_R -
Pin 7	CHOP_SENSE_L -	Pin 18	SPARE
Pin 8	CHOP_SENSE_L -	Pin 19	CHOP_DRV_L -
Pin 9	CHOP_SENSE_L +	Pin 20	CHOP_DRV_L -
Pin 10	CGND	Pin 21	CHOP_SENSE_R -
Pin 11	CHOP_DRV_L +	Pin 22	NC

Table 28 Cable Assembly: 48-0355 Chopper (External)

Cable Assembly: 48-0356		Sun Sensor (External)	
Connector	**P370**	**Part Number**	**GS83513/04-E16N-429**
Pin 1	MONUARTIN_RX+	Pin 17	MONUARTIN_RX-
Pin 2	UARTINA_RX+	Pin 18	UARTINA_RX-
Pin 3	UARTINB_RX+	Pin 19	UARTINB_RX-
Pin 4	UARTOUTA_TX+	Pin 20	UARTOUTA_TX-
Pin 5	UARTOUTB_TX+	Pin 21	UARTOUTB_TX-
Pin 6	20HZSYNCA_TX+	Pin 22	20HZSYNCA_TX-
Pin 7	20HZSYNCB_TX+	Pin 23	20HZSYNCB_TX-
Pin 8	MONUARTOUT_TX+	Pin 24	MONUARTOUT_TX-
Pin 9	SPARE1A+	Pin 25	SPARE1A-
Pin 10	SPARE2A+	Pin 26	SPARE2A-
Pin 11	RFPGA_S1	Pin 27	DGND
Pin 12	SUNSENSOR_5V	Pin 28	DGND
Pin 13	SUNSENSOR_5V	Pin 29	DGND
Pin 14	SUNSENSOR_5V	Pin 30	DGND
Pin 15	SUNSENSOR_5V	Pin 31	DGND
Pin 16	SUNSENSOR_5V		
Connector	**P380**	**Part Number**	**GS83513/04-A16N-429**
Pin 1	SSGUARTOUTA_TX+	Pin 6	SSGUARTOUTB_TX+
Pin 2	SSGUARTOUTA_TX-	Pin 7	SSGUARTOUTB_TX-
Pin 3	SSGUARTINA_RX+	Pin 8	SSGUARTINB_RX+
Pin 4	SSGUARTINA_RX-	Pin 9	SSGUARTINB_RX-
Pin 5	SPARE		
Connector	**P410**	**Part Number**	**MS27467T15F35SA**
Pin 1	SSGND1	Pin 20	UARTOUTA_TX- >> UARTINA_RX-
Pin 2	SSPWR1	Pin 21	UARTINA_RX+ >> UARTOUTA_TX+
Pin 3	SSPWR2	Pin 22	UARTINA_RX- >> UARTOUTA_TX-
Pin 4	SSGND2	Pin 23	UARTOUTB_TX+ >> UARTINB_RX+
Pin 5	SSGND3	Pin 24	UARTOUTB_TX- >> UARTINB_RX-
Pin 6	SSPWR3	Pin 25	UARTINB_RX+ >> UARTOUTB_TX+
Pin 7	SSPWR4	Pin 26	UARTINB_RX- >> UARTOUTB_TX-
Pin 8	SSGND4	Pin 27	SSGUARTINA_RX+
Pin 9	SSGND5	Pin 28	SSGUARTINA_RX-
Pin 10	SSPWR5	Pin 29	SSGUARTOUTA_TX+
Pin 11	NC	Pin 30	SSGUARTOUTA_TX-
Pin 12	NC	Pin 31	SSGUARTINB_RX+
Pin 13	NC	Pin 32	SSGUARTINB_RX-
Pin 14	NC	Pin 33	SSGUARTOUTB_TX+
Pin 15	20HZSYNCA_TX+ >> 20HZSYNCA_RX+	Pin 34	SSGUARTOUTB_TX-
Pin 16	20HZSYNCA_TX- >> 20HZSYNCA_RX-	Pin 35	SPARE
Pin 17	20HZSYNCB_TX+ >> 20HZSYNCB_RX+	Pin 36	NC

Pin 18	20HZSYNCB_TX- >> 20HZSYNCB_RX-	Pin 37	NC
Pin 19	UARTOUTA_TX+ >> UARTINA_RX+		

Table 29 Cable Assembly: 48-0356 Sun Sensor (External)

Cable Assembly: 48-0357		Release	
Connector	**P373**	**Part Number**	**GS83513/04-D16N-429**
Pin 1	APTPP1A+	Pin 14	APTPP1A-
Pin 2	APTPP1B+	Pin 15	APTPP1B-
Pin 3	APTPP2A+	Pin 16	APTPP2A-
Pin 4	APTPP2B+	Pin 17	APTPP2B-
Pin 5	SPARE	Pin 18	SPARE
Pin 6	SPARE	Pin 19	SPARE
Pin 7	SPARE	Pin 20	SPARE
Pin 8	SPARE	Pin 21	SPARE
Pin 9	SPARE	Pin 22	SPARE
Pin 10	SPARE	Pin 23	SPARE
Pin 11	SPARE	Pin 24	SPARE
Pin 12	SPARE	Pin 25	DGND
Pin 13	MIRROR_APTOPEN		
Connector	**P480**	**Part Number**	**JF2P2S45AB**
Pin A	APTPP1A-	Pin C	APTPP1A+
Pin B	APTPP2A-	Pin D	APTPP2A+
Connector	**P481**	**Part Number**	**JF2P2S45AB**
Pin A	APTPP1B-	Pin C	APTPP1B+
Pin B	APTPP2B-	Pin D	APTPP2B+
Connector	**P482**	**Part Number**	**JF1P1S45A**
Pin A	AGND	Pin B	APTOPEN_H

Table 30 Cable Assembly: 48-0357 Release Mechanism

Cable Assembly: 48-0358		Position (Blue Line Package)	
Connector	**P381**	**Part Number**	**GS83513/04-B16N-429**
Pin 1	NC	Pin 9	422_Tx_2MHzLO
Pin 2	422_Tx_2MHzHI	Pin 10	+12V_I
Pin 3	+12V_I	Pin 11	-12V_I
Pin 4	-12V_I	Pin 12	AGND
Pin 5	AGND	Pin 13	POSITION_1(+)
Pin 6	POSITION_1(-)	Pin 14	AGND
Pin 7	AGND	Pin 15	POSITION_2(+)
Pin 8	POSITION_2(-)		
Connector	**P460**	**Part Number**	**311P407-1P-B-12**
Pin 1	+12 VDC	Pin 9	SPARE
Pin 2	-12 VDC	Pin 10	2 MHZ LOW
Pin 3	ANALOG RETURN	Pin 11	SIG OUT 2
Pin 4	SPARE	Pin 12	SIG OUT 2 RTN
Pin 5	2 MHZ HI	Pin 13	SPARE
Pin 6	SIG OUT 1	Pin 14	FPS REF RTN
Pin 7	SIG OUT 1 RTN	Pin 15	FPS REF
Pin 8	SPARE		

Table 31 Cable Assembly: 48-0358 Position (Blue Line Package)

Cable Assembly: 48-0359		Motor (External)	
Connector	**P390**	**Part Number**	**GS83513/04-C16N-429**
Pin 1	SPARE	Pin 12	Motor 1 Power/3 Return
Pin 2	SPARE	Pin 13	Motor 1 Power/3 Return
Pin 3	SPARE	Pin 14	Motor 1 Return/3 Power
Pin 4	SPARE	Pin 15	Motor 1 Return/3 Power
Pin 5	SPARE	Pin 16	SPARE
Pin 6	SPARE	Pin 17	SPARE
Pin 7	SPARE	Pin 18	SPARE
Pin 8	Motor 2 Power/4 Return	Pin 19	SPARE
Pin 9	Motor 2 Power/4 Return	Pin 20	SPARE
Pin 10	Motor 2 Return/4 Power	Pin 21	SPARE
Pin 11	Motor 2 Return/4 Power		
Connector	**P470**	**Part Number**	**MS27467T13F35SA**
Pin 1	NC	Pin 12	Motor 2 Return/4 Power
Pin 2	Motor 2 Power/4 Return	Pin 13	Motor 2 Power/4 Return
Pin 3	Motor 2 Return/4 Power	Pin 14	NC
Pin 4	SHIELD	Pin 15	NC
Pin 5	Motor 1 Return/3 Power	Pin 16	NC
Pin 6	Motor 1 Power/3 Return	Pin 17	SHIELD
Pin 7	NC	Pin 18	NC
Pin 8	NC	Pin 19	SHIELD
Pin 9	Motor 1 Power/3 Return	Pin 20	NC
Pin 10	Motor 1 Return/3 Power	Pin 21	NC
Pin 11	SHIELD	Pin 22	NC

Table 32 Cable Assembly: 48-0359 Motor (External)

Cable Assembly: 48-0360		Survival Heaters (External)	
Connector	**P110**	**Part Number**	**MS27467T13F98P**
Pin A	SPARE	Pin F	SOFIE Instrument External Thermistor B - P
Pin B	SOFIE Instrument Survival Heater PRI PWR	Pin G	SOFIE Instrument Survival Heater SEC RTN
Pin C	SOFIE Instrument Survival Heater PRI RTN	Pin H	SOFIE Instrument Survival Heater SEC PWR
Pin D	SOFIE Instrument External Thermistor A - P	Pin J	SOFIE Instrument External Thermistor A - M
Pin E	SPARE	Pin K	SOFIE Instrument External Thermistor B - M
Connector	**P430**	**Part Number**	**MS27467T13F98S**
Pin A	SPARE	Pin F	SPARE
Pin B	SOFIE Instrument Survival Heater PRI PWR	Pin G	SOFIE Instrument Survival Heater SEC RTN
Pin C	SOFIE Instrument Survival Heater PRI RTN	Pin H	SOFIE Instrument Survival Heater SEC PWR
Pin D	SOFIE Instrument External Thermistor A - P	Pin J	SOFIE Instrument External Thermistor A - M
Pin E	SPARE	Pin K	SPARE
Connector	**P431**	**Part Number**	**JF2S2P45AB**
Pin A	SOFIE Instrument Survival Heater PRI PWR	Pin C	SOFIE Instrument Survival Heater PRI RTN
Pin B	SOFIE Instrument Survival Heater SEC PWR	Pin D	SOFIE Instrument Survival Heater SEC RTN
Connector	**P432**	**Part Number**	**JF2S45**
Pin A	SOFIE Instrument External Thermistor B - P	Pin B	SOFIE Instrument External Thermistor B - M

Table 33 Cable Assembly: 48-0360 Survival Heaters (External)

Cable Assembly: 48-0361		Cover Drain Wire (External)	
Connector	**P800**	**Part Number**	**SPC3718**
Pin 1	Instrument		
Connector	**P801**	**Part Number**	**SPC3718**
Pin 1	Cover		

Table 34 Cable Assembly: 48-0361 Cover Drain Wire (External)

Cable Assembly: 48-0362		Signal/Tec 1 (Internal)	
Connector	**J400**	**Part Number**	**MS27505E25F35P**
Pin 1	SPARE	Pin 46	TEC(+)
Pin 2	DET8ThermA	Pin 47	SPARE
Pin 3	DET8ThermB	Pin 48	AGND
Pin 4	AGND	Pin 49	AGND
Pin 5	DET7ThermA	Pin 50	AGND
Pin 6	DET7ThermB	Pin 51	AGND
Pin 7	AGND	Pin 52	AGND
Pin 8	DET6ThermA	Pin 53	AGND
Pin 9	DET6Sig(+)	Pin 54	AGND
Pin 10	DET8Sig(+)	Pin 55	AGND
Pin 11	DET8Sig(-)	Pin 56	DET5Bias
Pin 12	DET7Sig(+)	Pin 57	TEC(+)
Pin 13	DET7Sig(-)	Pin 58	TEC(-)
Pin 14	SPARE	Pin 59	(+)12V
Pin 15	DET6ThermB	Pin 60	(-)12V
Pin 16	AGND	Pin 61	(-)12V
Pin 17	DET6Sig(-)	Pin 62	(+)12V
Pin 18	TEC(+)	Pin 63	(+)12V
Pin 19	TEC(+)	Pin 64	(-)12V
Pin 20	TEC(-)	Pin 65	(-)12V
Pin 21	TEC(-)	Pin 66	(+)12V
Pin 22	DET5ThermA	Pin 67	AGND
Pin 23	DET5ThermB	Pin 68	AGND
Pin 24	AGND	Pin 69	TEC(-)
Pin 25	DET6Bias	Pin 70	DET4ThermA
Pin 26	TEC(+)	Pin 71	(+)12V
Pin 27	TEC(+)	Pin 72	(-)12V
Pin 28	TEC(-)	Pin 73	(-)12V
Pin 29	TEC(-)	Pin 74	(+)12V
Pin 30	TEC(+)	Pin 75	DET1ThermA
Pin 31	TEC(+)	Pin 76	(-)12V
Pin 32	TEC(+)	Pin 77	(+)12V
Pin 33	TEC(+)	Pin 78	DET2ThermA
Pin 34	DET5Sig(+)	Pin 79	(+)12V
Pin 35	SPARE	Pin 80	AGND
Pin 36	AGND	Pin 81	AGND
Pin 37	TEC(-)	Pin 82	DET3ThermA
Pin 38	TEC(-)	Pin 83	AGND
Pin 39	DET8Bias	Pin 84	AGND
Pin 40	AGND	Pin 85	AGND
Pin 41	DET7Bias	Pin 86	AGND
Pin 42	AGND	Pin 87	AGND
Pin 43	TEC(-)	Pin 88	AGND
Pin 44	TEC(-)	Pin 89	AGND
Pin 45	DET5Sig(-)	Pin 90	DET2ThermB

Connector	J400 (cont)	Part Number	MS27505E25F35P
Pin 91	(-)12V	Pin 110	DET1Sig(+)
Pin 92	AGND	Pin 111	TEC(-)
Pin 93	DET4ThermB	Pin 112	TEC(-)
Pin 94	DET3ThermB	Pin 113	AGND
Pin 95	DET3Sig(-)	Pin 114	DET4Sig(+)
Pin 96	DET3Sig(+)	Pin 115	TEC(-)
Pin 97	AGND	Pin 116	TEC(-)
Pin 98	DET1Bias	Pin 117	TEC(+)
Pin 99	DET1ThermB	Pin 118	TEC(+)
Pin 100	TEC(+)	Pin 119	DET1Sig(-)
Pin 101	TEC(+)	Pin 120	DET2Sig(-)
Pin 102	AGND	Pin 121	DET2Bias
Pin 103	DET4Sig(-)	Pin 122	TEC(+)
Pin 104	DET4Bias	Pin 123	TEC(+)
Pin 105	AGND	Pin 124	SPARE
Pin 106	DET3Bias	Pin 125	SPARE
Pin 107	AGND	Pin 126	SPARE
Pin 108	TEC(-)	Pin 127	SPARE
Pin 109	TEC(-)	Pin 128	DET2Sig(+)
Connector	**P501**	**Part Number**	**GS83513/03-B16N-429**
Pin 1	(-)12V	Pin 9	(+)12V
Pin 2	AGND	Pin 10	AGND
Pin 3	Det Sig(+)	Pin 11	Det Sig(-)
Pin 4	Det Bias	Pin 12	AGND
Pin 5	THERMA	Pin 13	AGND
Pin 6	THERMB	Pin 14	TEC GND
Pin 7	TEC(+)	Pin 15	TEC GND
Pin 8	TEC(+)		
Connector	**P502**	**Part Number**	**GS83513/03-B16N-429**
Pin 1	(-)12V	Pin 9	(+)12V
Pin 2	AGND	Pin 10	AGND
Pin 3	Det Sig(+)	Pin 11	Det Sig(-)
Pin 4	Det Bias	Pin 12	AGND
Pin 5	THERMA	Pin 13	AGND
Pin 6	THERMB	Pin 14	TEC GND
Pin 7	TEC(+)	Pin 15	TEC GND
Pin 8	TEC(+)		
Connector	**P503**	**Part Number**	**GS83513/03-B16N-429**
Pin 1	(-)12V	Pin 9	(+)12V
Pin 2	AGND	Pin 10	AGND
Pin 3	Det Sig(+)	Pin 11	Det Sig(-)
Pin 4	Det Bias	Pin 12	AGND
Pin 5	THERMA	Pin 13	AGND
Pin 6	THERMB	Pin 14	TEC GND
Pin 7	TEC(+)	Pin 15	TEC GND
Pin 8	TEC(+)		

Connector	P504	Part Number	GS83513/03-B16N-429
Pin 1	(-)12V	Pin 9	(+)12V
Pin 2	AGND	Pin 10	AGND
Pin 3	Det Sig(+)	Pin 11	Det Sig(-)
Pin 4	Det Bias	Pin 12	AGND
Pin 5	THERMA	Pin 13	AGND
Pin 6	THERMB	Pin 14	TEC GND
Pin 7	TEC(+)	Pin 15	TEC GND
Pin 8	TEC(+)		
Connector	**P505**	**Part Number**	**GS83513/03-B16N-429**
Pin 1	(-)12V	Pin 9	(+)12V
Pin 2	AGND	Pin 10	AGND
Pin 3	Det Sig(+)	Pin 11	Det Sig(-)
Pin 4	Det Bias	Pin 12	AGND
Pin 5	THERMA	Pin 13	AGND
Pin 6	THERMB	Pin 14	TEC GND
Pin 7	TEC(+)	Pin 15	TEC GND
Pin 8	TEC(+)		
Connector	**P506**	**Part Number**	**GS83513/03-B16N-429**
Pin 1	(-)12V	Pin 9	(+)12V
Pin 2	AGND	Pin 10	AGND
Pin 3	Det Sig(+)	Pin 11	Det Sig(-)
Pin 4	Det Bias	Pin 12	AGND
Pin 5	THERMA	Pin 13	AGND
Pin 6	THERMB	Pin 14	TEC GND
Pin 7	TEC(+)	Pin 15	TEC GND
Pin 8	TEC(+)		
Connector	**P507**	**Part Number**	**GS83513/03-B16N-429**
Pin 1	(-)12V	Pin 9	(+)12V
Pin 2	AGND	Pin 10	AGND
Pin 3	Det Sig(+)	Pin 11	Det Sig(-)
Pin 4	Det Bias	Pin 12	AGND
Pin 5	THERMA	Pin 13	AGND
Pin 6	THERMB	Pin 14	TEC GND
Pin 7	TEC(+)	Pin 15	TEC GND
Pin 8	TEC(+)		
Connector	**P508**	**Part Number**	**GS83513/03-B16N-429**
Pin 1	(-)12V	Pin 9	(+)12V
Pin 2	AGND	Pin 10	AGND
Pin 3	Det Sig(+)	Pin 11	Det Sig(-)
Pin 4	Det Bias	Pin 12	AGND
Pin 5	THERMA	Pin 13	AGND
Pin 6	THERMB	Pin 14	TEC GND
Pin 7	TEC(+)	Pin 15	TEC GND
Pin 8	TEC(+)		

Table 35 Cable Assembly: 48-0362 Signal/TEC 1 (Internal)

Cable Assembly: 48-0363		Signal/Tec 2 (Internal)	
Connector	**J420**	**Part Number**	**MS27505E25F35PA**
Pin 1	SPARE	Pin 46	TEC(+)
Pin 2	DET9ThermA	Pin 47	SPARE
Pin 3	DET9ThermB	Pin 48	AGND
Pin 4	AGND	Pin 49	AGND
Pin 5	DET10ThermA	Pin 50	AGND
Pin 6	DET10ThermB	Pin 51	AGND
Pin 7	AGND	Pin 52	AGND
Pin 8	DET11ThermA	Pin 53	AGND
Pin 9	DET11Sig(+)	Pin 54	AGND
Pin 10	DET9Sig(+)	Pin 55	AGND
Pin 11	DET9Sig(-)	Pin 56	DET12Bias
Pin 12	DET10Sig(+)	Pin 57	TEC(+)
Pin 13	DET10Sig(-)	Pin 58	TEC(-)
Pin 14	SPARE	Pin 59	(+)12V
Pin 15	DET11ThermB	Pin 60	(-)12V
Pin 16	AGND	Pin 61	(-)12V
Pin 17	DET11Sig(-)	Pin 62	(+)12V
Pin 18	TEC(+)	Pin 63	(+)12V
Pin 19	TEC(+)	Pin 64	(-)12V
Pin 20	TEC(-)	Pin 65	(-)12V
Pin 21	TEC(-)	Pin 66	(+)12V
Pin 22	DET12ThermA	Pin 67	AGND
Pin 23	DET12ThermB	Pin 68	AGND
Pin 24	AGND	Pin 69	TEC(-)
Pin 25	DET11Bias	Pin 70	DET13ThermA
Pin 26	TEC(+)	Pin 71	(+)12V
Pin 27	TEC(+)	Pin 72	(-)12V
Pin 28	TEC(-)	Pin 73	(-)12V
Pin 29	TEC(-)	Pin 74	(+)12V
Pin 30	TEC(+)	Pin 75	DET16ThermA
Pin 31	TEC(+)	Pin 76	(-)12V
Pin 32	TEC(+)	Pin 77	(+)12V
Pin 33	TEC(+)	Pin 78	DET15ThermA
Pin 34	DET12Sig(+)	Pin 79	(+)12V
Pin 35	SPARE	Pin 80	AGND
Pin 36	AGND	Pin 81	AGND
Pin 37	TEC(-)	Pin 82	DET14ThermA
Pin 38	TEC(-)	Pin 83	AGND
Pin 39	DET9Bias	Pin 84	AGND
Pin 40	AGND	Pin 85	AGND
Pin 41	DET10Bias	Pin 86	AGND
Pin 42	AGND	Pin 87	AGND
Pin 43	TEC(-)	Pin 88	AGND
Pin 44	TEC(-)	Pin 89	AGND
Pin 45	DET12Sig(-)	Pin 90	DET15ThermB

Connector	J420 (cont)	Part Number	MS27505E25F35PA
Pin 91	(-)12V	Pin 110	DET16Sig(+)
Pin 92	AGND	Pin 111	TEC(-)
Pin 93	DET13ThermB	Pin 112	TEC(-)
Pin 94	DET14ThermB	Pin 113	AGND
Pin 95	DET14Sig(-)	Pin 114	DET13Sig(+)
Pin 96	DET14Sig(+)	Pin 115	TEC(-)
Pin 97	AGND	Pin 116	TEC(-)
Pin 98	DET16Bias	Pin 117	TEC(+)
Pin 99	DET16ThermB	Pin 118	TEC(+)
Pin 100	TEC(+)	Pin 119	DET16Sig(-)
Pin 101	TEC(+)	Pin 120	DET15Sig(-)
Pin 102	AGND	Pin 121	DET15Bias
Pin 103	DET13Sig(-)	Pin 122	TEC(+)
Pin 104	DET13Bias	Pin 123	TEC(+)
Pin 105	AGND	Pin 124	SPARE
Pin 106	DET14Bias	Pin 125	SPARE
Pin 107	AGND	Pin 126	SPARE
Pin 108	TEC(-)	Pin 127	SPARE
Pin 109	TEC(-)	Pin 128	DET15Sig(+)
Connector	**P509**	**Part Number**	**GS83513/03-B16N-429**
Pin 1	(-)12V	Pin 9	(+)12V
Pin 2	AGND	Pin 10	AGND
Pin 3	Det Sig(+)	Pin 11	Det Sig(-)
Pin 4	Det Bias	Pin 12	AGND
Pin 5	THERMA	Pin 13	AGND
Pin 6	THERMB	Pin 14	TEC GND
Pin 7	TEC(+)	Pin 15	TEC GND
Pin 8	TEC(+)		
Connector	**P510**	**Part Number**	**GS83513/03-B16N-429**
Pin 1	(-)12V	Pin 9	(+)12V
Pin 2	AGND	Pin 10	AGND
Pin 3	Det Sig(+)	Pin 11	Det Sig(-)
Pin 4	Det Bias	Pin 12	AGND
Pin 5	THERMA	Pin 13	AGND
Pin 6	THERMB	Pin 14	TEC GND
Pin 7	TEC(+)	Pin 15	TEC GND
Pin 8	TEC(+)		
Connector	**P511**	**Part Number**	**GS83513/03-B16N-429**
Pin 1	(-)12V	Pin 9	(+)12V
Pin 2	AGND	Pin 10	AGND
Pin 3	Det Sig(+)	Pin 11	Det Sig(-)
Pin 4	Det Bias	Pin 12	AGND
Pin 5	THERMA	Pin 13	AGND
Pin 6	THERMB	Pin 14	TEC GND
Pin 7	TEC(+)	Pin 15	TEC GND
Pin 8	TEC(+)		

Connector	**P512**	**Part Number**	**GS83513/03-B16N-429**
Pin 1	(-)12V	Pin 9	(+)12V
Pin 2	AGND	Pin 10	AGND
Pin 3	Det Sig(+)	Pin 11	Det Sig(-)
Pin 4	Det Bias	Pin 12	AGND
Pin 5	THERMA	Pin 13	AGND
Pin 6	THERMB	Pin 14	TEC GND
Pin 7	TEC(+)	Pin 15	TEC GND
Pin 8	TEC(+)		
Connector	**P513**	**Part Number**	**GS83513/03-B16N-429**
Pin 1	(-)12V	Pin 9	(+)12V
Pin 2	AGND	Pin 10	AGND
Pin 3	Det Sig(+)	Pin 11	Det Sig(-)
Pin 4	Det Bias	Pin 12	AGND
Pin 5	THERMA	Pin 13	AGND
Pin 6	THERMB	Pin 14	TEC GND
Pin 7	TEC(+)	Pin 15	TEC GND
Pin 8	TEC(+)		
Connector	**P514**	**Part Number**	**GS83513/03-B16N-429**
Pin 1	(-)12V	Pin 9	(+)12V
Pin 2	AGND	Pin 10	AGND
Pin 3	Det Sig(+)	Pin 11	Det Sig(-)
Pin 4	Det Bias	Pin 12	AGND
Pin 5	THERMA	Pin 13	AGND
Pin 6	THERMB	Pin 14	TEC GND
Pin 7	TEC(+)	Pin 15	TEC GND
Pin 8	TEC(+)		
Connector	**P515**	**Part Number**	**GS83513/03-B16N-429**
Pin 1	(-)12V	Pin 9	(+)12V
Pin 2	AGND	Pin 10	AGND
Pin 3	Det Sig(+)	Pin 11	Det Sig(-)
Pin 4	Det Bias	Pin 12	AGND
Pin 5	THERMA	Pin 13	AGND
Pin 6	THERMB	Pin 14	TEC GND
Pin 7	TEC(+)	Pin 15	TEC GND
Pin 8	TEC(+)		
Connector	**P516**	**Part Number**	**GS83513/03-B16N-429**
Pin 1	(-)12V	Pin 9	(+)12V
Pin 2	AGND	Pin 10	AGND
Pin 3	Det Sig(+)	Pin 11	Det Sig(-)
Pin 4	Det Bias	Pin 12	AGND
Pin 5	THERMA	Pin 13	AGND
Pin 6	THERMB	Pin 14	TEC GND
Pin 7	TEC(+)	Pin 15	TEC GND
Pin 8	TEC(+)		

Table 36 Cable Assembly: 48-0363 Signal/TEC 2 (Internal)

Cable Assembly: 48-0364		Data Acquisition (Internal)	
Connector	**J440**	**Part Number**	**MS27505E21F35P**
Pin 1	SPARE	Pin 28	NC
Pin 2	SPARE	Pin 29	NC
Pin 3	SPARE	Pin 30	TS[10]- (EXT) CSM Beam Splitter Assembly
Pin 4	SPARE	Pin 31	TS[10]+ (EXT) CSM Beam Splitter Assembly
Pin 5	SPARE	Pin 32	TS[7]- (EXT) Optics Housing Bands 1&3
Pin 6	SPARE	Pin 33	TS[7]+ (EXT) Optics Housing Bands 1&3
Pin 7	SPARE	Pin 34	TS[52]- (EXT) Fore Optics Bench #2
Pin 8	NC	Pin 35	TS[52]+ (EXT) Fore Optics Bench #2
Pin 9	NC	Pin 36	TS[36]- (EXT) Mid Optics Housing
Pin 10	NC	Pin 37	TS[36]+ (EXT) Mid Optics Housing
Pin 11	NC	Pin 38	TS[42]- (EXT) Base Deck Plate
Pin 12	NC	Pin 39	TS[42]+ (EXT) Base Deck Plate
Pin 13	NC	Pin 40	NC
Pin 14	NC	Pin 41	TS[56]+ (EXT) Optics Housing Bands 2&4
Pin 15	SPARE	Pin 42	TS[56]- (EXT) Optics Housing Bands 2&4
Pin 16	SPARE	Pin 43	TS[55]+ (EXT) Optics Housing Bands 5&7
Pin 17	SPARE	Pin 44	TS[55]- (EXT) Optics Housing Bands 5&7
Pin 18	SPARE	Pin 45	TS[41]+ (EXT) Aft Optics Bench #2
Pin 19	SPARE	Pin 46	TS[41]- (EXT) Aft Optics Bench #2
Pin 20	SPARE	Pin 47	TS[23]+ (EXT) Optics Housing Bands 9&11
Pin 21	SPARE	Pin 48	TS[23]- (EXT) Optics Housing Bands 9&11
Pin 22	NC	Pin 49	TS[22]+ (EXT) Aft Optics Bench #1
Pin 23	NC	Pin 50	TS[22]- (EXT) Aft Optics Bench #1
Pin 24	NC	Pin 51	NC
Pin 25	NC	Pin 52	TS[21]- (EXT) Sun Sensor PCB
Pin 26	NC	Pin 53	TS[21]+ (EXT) Sun Sensor PCB

Pin 27	NC	Pin 54	TS[9]- (EXT) CSM Near Optics Module
Pin 28	NC	Pin 55	TS[9]+ (EXT) CSM Near Optics Module
Connector	**P440 (cont)**	**Part Number**	**MS27505E21F35P**
Pin 56	TS[53]- (EXT) Sun Sensor Module	Pin 68	TS[8]- (EXT) Optics Housing Bands 6&8
Pin 57	TS[53]+ (EXT) Sun Sensor Module	Pin 69	TS[8]+ (EXT) Optics Housing Bands 6&8
Pin 58	NC	Pin 70	TS[57]- (EXT) Aft Optics Bench #3
Pin 59	TS[38]+ (EXT) SPARE	Pin 71	TS[57]+ (EXT) Aft Optics Bench #3
Pin 60	TS[38]- (EXT) SPARE	Pin 72	SPARE
Pin 61	TS[40]+ (EXT) Optics Housing Bands 13&15	Pin 73	TS[39]+ (EXT) Optics Housing Bands 10&12
Pin 62	TS[40]- (EXT) Optics Housing Bands 13&15	Pin 74	TS[39]- (EXT) Optics Housing Bands 10&12
Pin 63	TS[20]+ (EXT) Upper Cable Bulkhead	Pin 75	TS[24]+ (EXT) Optics Housing Bands 14&16
Pin 64	TS[20]- (EXT) Upper Cable Bulkhead	Pin 76	TS[24]- (EXT) Optics Housing Bands 14&16
Pin 65	TS[25]+ (EXT) CSM Far Optics Module	Pin 77	NC
Pin 66	TS[25]- (EXT) CSM Far Optics Module	Pin 78	NC
Pin 67	NC	Pin 79	NC
Connector	**J704**	**Part Number**	**JF1S1P45A**
Pin A	TS[7]+ (EXT) Optics Housing Bands 1&3	Pin B	TS[7]- (EXT) Optics Housing Bands 1&3
Connector	**J705**	**Part Number**	**JF1S1P45A**
Pin A	TS[8]+ (EXT) Optics Housing Bands 6&8	Pin B	TS[8]- (EXT) Optics Housing Bands 6&8
Connector	**J706**	**Part Number**	**JF1S1P45A**
Pin A	TS[9]+ (EXT) CSM Near Optics Module	Pin B	TS[9]- (EXT) CSM Near Optics Module
Connector	**J707**	**Part Number**	**JF1S1P45A**
Pin A	TS[10]+ (EXT) CSM Beam Splitter Assembly	Pin B	TS[10]- (EXT) CSM Beam Splitter Assembly
Connector	**J708**	**Part Number**	**JF1S1P45A**
Pin A	TS[20]+ (EXT) Upper Cable Bulkhead	Pin B	TS[20]- (EXT) Upper Cable Bulkhead
Connector	**J710**	**Part Number**	**JF1S1P45A**
Pin A	TS[22]+ (EXT) Aft Optics Bench #1	Pin B	TS[22]- (EXT) Aft Optics Bench #1
Connector	**J711**	**Part Number**	**JF1S1P45A**

Pin A	TS[23]+ (EXT) Optics Housing Bands 9&11	Pin B	TS[23]- (EXT) Optics Housing Bands 9&11
Connector	**J712**	**Part Number**	**JF1S1P45A**
Pin A	TS[24]+ (EXT) Optics Housing Bands 14&16	Pin B	TS[24]- (EXT) Optics Housing Bands 14&16
Connector	**J713**	**Part Number**	**JF1S1P45A**
Pin A	TS[25]+ (EXT) CSM Far Optics Module	Pin B	TS[25]- (EXT) CSM Far Optics Module
Connector	**J715**	**Part Number**	**JF1S1P45A**
Pin A	TS[36]+ (EXT) Mid Optics Housing	Pin B	TS[36]- (EXT) Mid Optics Housing
Connector	**J717**	**Part Number**	**JF1S1P45A**
Pin A	TS[39]+ (EXT) Optics Housing Bands 10&12	Pin B	TS[39]- (EXT) Optics Housing Bands 10&12
Connector	**J718**	**Part Number**	**JF1S1P45A**
Pin A	TS[40]+ (EXT) Optics Housing Bands 13&15	Pin B	TS[40]- (EXT) Optics Housing Bands 13&15
Connector	**J719**	**Part Number**	**JF1S1P45A**
Pin A	TS[41]+ (EXT) Aft Optics Bench #2	Pin B	TS[41]- (EXT) Aft Optics Bench #2
Connector	**J722**	**Part Number**	**JF1S1P45A**
Pin A	TS[52]+ (EXT) Fore Optics Bench #2	Pin B	TS[52]- (EXT) Fore Optics Bench #2
Connector	**J724**	**Part Number**	**JF1S1P45A**
Pin A	TS[55]+ (EXT) Optics Housing Bands 5&7	Pin B	TS[55]- (EXT) Optics Housing Bands 5&7
Connector	**J725**	**Part Number**	**JF1S1P45A**
Pin A	TS[56]+ (EXT) Optics Housing Bands 2&4	Pin B	TS[56]- (EXT) Optics Housing Bands 2&4
Connector	**J726**	**Part Number**	**JF1S1P45A**
Pin A	TS[57]+ (EXT) Aft Optics Bench #3	Pin B	TS[57]- (EXT) Aft Optics Bench #3
Connector	**J728**	**Part Number**	**JF1S1P45A**
Pin A	TS[53]+ (EXT) Sun Sensor Module	Pin B	TS[53]- (EXT) Sun Sensor Module
Connector	**J729**	**Part Number**	**JF1S1P45A**
Pin A	TS[21]+ (EXT) Sun Sensor PCB	Pin B	TS[21]- (EXT) Sun Sensor PCB
Connector	**J730**	**Part Number**	**JF1S1P45A**
Pin A	TS[42]+ (EXT) Base Deck Plate	Pin B	TS[42]- (EXT) Base Deck Plate

Table 37 Cable Assembly: 48-0364 Data Acquisition (Internal)

Cable Assembly: 48-0365		Chopper (Internal)	
Connector	**J450**	**Part Number**	**MS27505E13F35P**
Pin 1	CHOP_SENSE_R +	Pin 12	CHOP_DRV_L +
Pin 2	CGND	Pin 13	CGND
Pin 3	CHOP_DRV_R +	Pin 14	CHOP_SENSE_R +
Pin 4	CHOP_DRV_R +	Pin 15	CHOP_SENSE_R -
Pin 5	CGND	Pin 16	CHOP_DRV_R -
Pin 6	CHOP_SENSE_L +	Pin 17	CHOP_DRV_R -
Pin 7	CHOP_SENSE_L -	Pin 18	SPARE
Pin 8	CHOP_SENSE_L -	Pin 19	CHOP_DRV_L -
Pin 9	CHOP_SENSE_L +	Pin 20	CHOP_DRV_L -
Pin 10	CGND	Pin 21	CHOP_SENSE_R -
Pin 11	CHOP_DRV_L +	Pin 22	NC
Connector	**P620**	**Part Number**	**GS83513/03-C16N-429**
Pin 1	CHOP_SENSE_R +	Pin 12	CHOP_SENSE_R -
Pin 2	CHOP_SENSE_R +	Pin 13	CHOP_SENSE_R -
Pin 3	SPARE	Pin 14	SPARE
Pin 4	CHOP_DRV_R +	Pin 15	CHOP_DRV_R -
Pin 5	CHOP_DRV_R +	Pin 16	CHOP_DRV_R -
Pin 6	SPARE	Pin 17	CHOP_DRV_L -
Pin 7	CHOP_DRV_L +	Pin 18	CHOP_DRV_L -
Pin 8	CHOP_DRV_L +	Pin 19	SPARE
Pin 9	SPARE	Pin 20	CHOP_SENSE_L +
Pin 10	CHOP_SENSE_L -	Pin 21	CHOP_SENSE_L +
Pin 11	CHOP_SENSE_L -		

Table 38 Cable Assembly: 48-0365 Chopper (Internal)

Cable Assembly: 48-0366		Sun Sensor (Internal)	
Connector	**J410**	**Part Number**	**MS27505E15F35PA**
Pin 1	SSGND1	Pin 20	UARTOUTA_TX- >> UARTINA_RX-
Pin 2	SSPWR1	Pin 21	UARTINA_RX+ >> UARTOUTA_TX+
Pin 3	SSPWR2	Pin 22	UARTINA_RX- >> UARTOUTA_TX-
Pin 4	SSGND2	Pin 23	UARTOUTB_TX+ >> UARTINB_RX+
Pin 5	SSGND3	Pin 24	UARTOUTB_TX- >> UARTINB_RX-
Pin 6	SSPWR3	Pin 25	UARTINB_RX+ >> UARTOUTB_TX+
Pin 7	SSPWR4	Pin 26	UARTINB_RX- >> UARTOUTB_TX-
Pin 8	SSGND4	Pin 27	SSGUARTINA_RX+
Pin 9	SSGND5	Pin 28	SSGUARTINA_RX-
Pin 10	SSPWR5	Pin 29	SSGUARTOUTA_TX+
Pin 11	NC	Pin 30	SSGUARTOUTA_TX-
Pin 12	NC	Pin 31	SSGUARTINB_RX+
Pin 13	NC	Pin 32	SSGUARTINB_RX-
Pin 14	NC	Pin 33	SSGUARTOUTB_TX+
Pin 15	20HZSYNCA_TX+ >> 20HZSYNCA_RX+	Pin 34	SSGUARTOUTB_TX-
Pin 16	20HZSYNCA_TX- >> 20HZSYNCA_RX-	Pin 35	SPARE
Pin 17	20HZSYNCB_TX+ >> 20HZSYNCB_RX+	Pin 36	NC
Pin 18	20HZSYNCB_TX- >> 20HZSYNCB_RX-	Pin 37	NC
Pin 19	UARTOUTA_TX+ >> UARTINA_RX+		
Connector	**P610**	**Part Number**	**GS83513/03-F16N-429**
Pin 1	SSPWR1 (+5V)	Pin 20	SSGND1 (DGND)
Pin 2	SSPWR2 (+5V)	Pin 21	SSGND2 (DGND)
Pin 3	SSPWR3 (+5V)	Pin 22	SSGND3 (DGND)
Pin 4	SSPWR4 (+5VA)	Pin 23	SSGND4 (AGND)
Pin 5	SSPWR5 (+5VA)	Pin 24	SSGND5 (AGND)
Pin 6	SSGUARTINB_RX(-)	Pin 25	SSGUARTINB_RX+
Pin 7	UARTINB_RX-	Pin 26	UARTINB_RX+
Pin 8	20HZSYNCB_RX+	Pin 27	20HZSYNCB_RX-
Pin 9	MONUARTIN_RX+	Pin 28	MONUARTIN_RX-
Pin 10	SSGUARTINA_RX-	Pin 29	SSGUARTINA_RX+
Pin 11	UARTINA_RX+	Pin 30	UARTINA_RX-
Pin 12	20HZSYNCA_RX+	Pin 31	20HZSYNCA_RX-
Pin 13	MONUARTOUT_TX+	Pin 32	MONUARTOUT_TX-
Pin 14	SSGUARTOUTB_TX-	Pin 33	SSGUARTOUTB_TX+
Pin 15	UARTOUTB_TX-	Pin 34	UARTOUTB_TX+
Pin 16	SSGUARTOUTA_TX+	Pin 35	SSGUARTOUTA_TX-
Pin 17	UARTOUTA_TX-	Pin 36	UARTOUTA_TX+
Pin 18	SPARE	Pin 37	SSTEMPRTN
Pin 19	SSTEMPPWR		
Connector	**P709**	**Part**	**JF1S1P45A**

	Number		
Pin A	TS[21]+ (EXT) Sun Sensor PCB	Pin B	TS[21]- (EXT) Sun Sensor PCB

Table 39 Cable Assembly: 48-0366 Sun Sensor (Internal)

Cable Assembly: 48-0367		Motor (Internal)	
Connector	**J470**	**Part Number**	**MS27505E13F35PA**
Pin 1	NC	Pin 12	Motor 2 Return/4 Power
Pin 2	Motor 2 Power/4 Return	Pin 13	Motor 2 Power/4 Return
Pin 3	Motor 2 Return/4 Power	Pin 14	NC
Pin 4	SHIELD	Pin 15	NC
Pin 5	Motor 1 Return/3 Power	Pin 16	NC
Pin 6	Motor 1 Power/3 Return	Pin 17	SHIELD
Pin 7	NC	Pin 18	NC
Pin 8	NC	Pin 19	SHIELD
Pin 9	Motor 1 Power/3 Return	Pin 20	NC
Pin 10	Motor 1 Return/3 Power	Pin 21	NC
Pin 11	SHIELD	Pin 22	NC
Connector	**P630**	**Part Number**	**GS83513/03-D11N-429**
Pin 1	NC	Pin 14	Motor 1 Return/3 Power
Pin 2	NC	Pin 15	Motor 1 Return/3 Power
Pin 3	NC	Pin 16	Motor 1 Power/ 3 Return
Pin 4	TS[3]- (EXT) Steering Mirror Motor Coil	Pin 17	Motor 1 Power/ 3 Return
Pin 5	NC	Pin 18	NC
Pin 6	TS[3]+ (EXT) Steering Mirror Motor Coil	Pin 19	NC
Pin 7	NC	Pin 20	NC
Pin 8	TS[19]+ (EXT) Steering Mirror Base	Pin 21	NC
Pin 9	NC	Pin 22	Motor 2 Power/4 Return
Pin 10	TS[19]- (EXT) Steering Mirror Base	Pin 23	Motor 2 Power/4 Return
Pin 11	NC	Pin 24	Motor 2 Return/ 4 Power
Pin 12	NC	Pin 25	Motor 2 Return/ 4 Power
Pin 13	NC		
Connector	**J700**	**Part Number**	**JF2P2S45AB**
Pin A	TS[3]+ (EXT) Steering Mirror Motor Coil	Pin C	TS[3]- (EXT) Steering Mirror Motor Coil
Pin B	TS[19]+ (EXT) Steering Mirror Base	Pin D	TS[19]- (EXT) Steering Mirror Base

Table 40 Cable Assembly: 48-0367 Motor (Internal)

Cable Assembly: 48-0368		Survival Heaters (Internal)	
Connector	**J430**	**Part Number**	**MS27505E13F98P**
Pin A	SPARE	Pin F	SPARE
Pin B	SOFIE Instrument Survival Heater PRI PWR	Pin G	SOFIE Instrument Survival Heater SEC RTN
Pin C	SOFIE Instrument Survival Heater PRI RTN	Pin H	SOFIE Instrument Survival Heater SEC PWR
Pin D	SOFIE Instrument External Thermistor A - P	Pin J	SOFIE Instrument External Thermistor A - M
Pin E	SPARE	Pin K	SPARE
Connector	**P600**	**Part Number**	**JF2S2P45AB**
Pin A	SOFIE Instrument Survival Heater PRI PWR	Pin C	SOFIE Instrument Survival Heater PRI RTN
Pin B	SOFIE Instrument Survival Heater SEC PWR	Pin D	SOFIE Instrument Survival Heater SEC RTN
Connector	**P601**	**Part Number**	**JF2S45**
Pin A	SOFIE Instrument External Thermistor A - P	Pin B	SOFIE Instrument External Thermistor A - M

Table 41 Cable Assembly: 48-0368 Survival Heaters (Internal)